

# SH7216 Group

# Using the Compare Match Timer

R01AN0429EJ0100 Rev. 1.00 Jan. 11, 2011

## **Summary**

This application note describes an example to use interrupts by the SH7216 Compare Match Timer.

## **Target Device**

SH7216 MCU

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#### 1. Introduction

### 1.1 Specifications

Uses the SH7216 Compare Match Timer interrupts to blink an LED.

This application uses the Compare Match Timer as a 10-ms periodic timer, and generates a compare match interrupt when the compare match flag is set to 1. Every time when the number of compare match interrupts reaches 50, the SH7216 reverses the general-purpose I/O ports output value within the interrupt processing, and blinks the LED which is connected to the general-purpose I/O ports in 500-ms period.

#### 1.2 Modules Used

- Compare Match Timer (CMT)
- Interrupt Controller (INTC)

## 1.3 Applicable Conditions

MCU SH7216

Operating Frequency Internal clock: 200 MHz

Bus clock: 50 MHz

Peripheral clock: 50 MHz

Integrated Development Renesas Electronics Corporation

Environment High-performance Embedded Workshop Ver.4.07.00 C Compiler Renesas Electronics SuperH RISC engine Family

C/C++ compiler package Ver.9.03 Release 00

Compiler Options Default setting in the High-performance Embedded Workshop

(-cpu=sh2afpu -fpu=single -debug -gbr=auto -global\_volatile=0 -opt\_range=all -infinite\_loop=0 -del\_vacant\_loop=0 -struct\_alloc=1)

## 1.4 Related Application Note

For more information, refer to the following application note:

• SH7216 Group Example of Initialization

## 2. Applications

#### 2.1 Overview of Modules

#### 2.1.1 Compare Match Timer

Compare Match Timer (CMT) counts values in a constant interval by the Compare match counter (CMCNT). When the Count start bit in the Compare match timer start register (CMSTR) is set to 1, the CMCNT starts counting up. When the CMCNT value matches the Compare match constant register (CMCOR) value, the CMCNT is cleared to 0, and the Compare match flag (CMF) in the Compare match timer control/status register (CMCSR) is set to 1. A compare match interrupt (CMI) occurs when the Compare match interrupt enable bit (CMIE) in the CMCSR is set to 1 at the same time. Then, the CMCNT starts counting up from 0 again.

Table 1 lists the specifications of the CMT. Figure 1 shows its block diagram. For more information, refer to the Compare Match Timer (CMT) chapter in the SH7214 Group, SH7216 Group User's Hardware Manual.

#### **Table 1 CMT Specifications**

Item	Description
Number of channels available	2
Counting	16-bit counter (only up-counter)
Pin function	None
Clock source	Pφ/8, Pφ/32, Pφ/128, Pφ/512 (Pφ: peripheral clock)
How to activate	Activated by the software
Compare match occur condition	A compare match occurs at the last state (CMCNT value is updated to H'0000) when the CMCNT and CMCOR match
Interrupt request	Compare match interrupt (CMI)

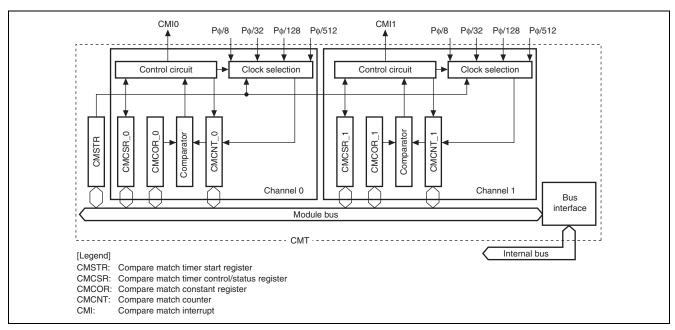


Figure 1 CMT Block Diagram

#### 2.1.2 Interrupt Controller

The Interrupt Controller (INTC) detects the priority of interrupt sources, and controls interrupt requests to the CPU. INTC has registers to set interrupt priorities, and it handles interrupt requests according to the priority which is set to the INTC register by user.

Figure 2 shows the INTC block diagram. For more information, refer to the Interrupt Controller (INTC) chapter in the SH7214 Group, SH7216 Group User's Hardware Manual.

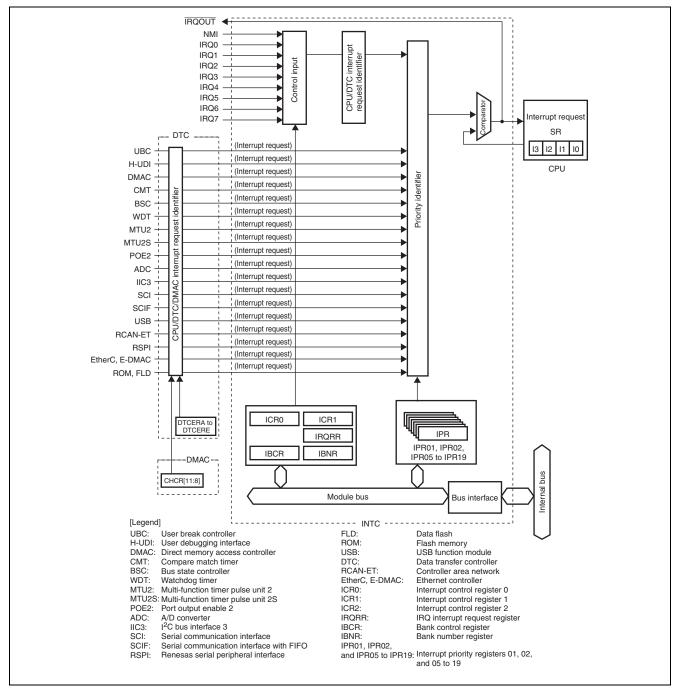


Figure 2 INTC Block Diagram

#### 2.2 Configuration Procedure

This section describes how to configure the CMT (channel 0) periodic count operation.

Figure 3 shows the flow chart for configuring the CMT periodic counter. For more information on register settings, refer to the SH7214 Group, SH7216 Group User's Hardware Manual.

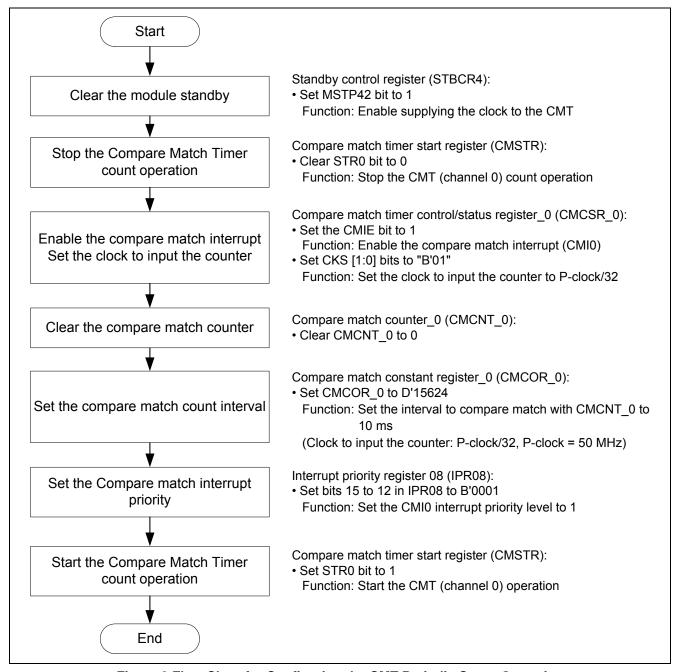
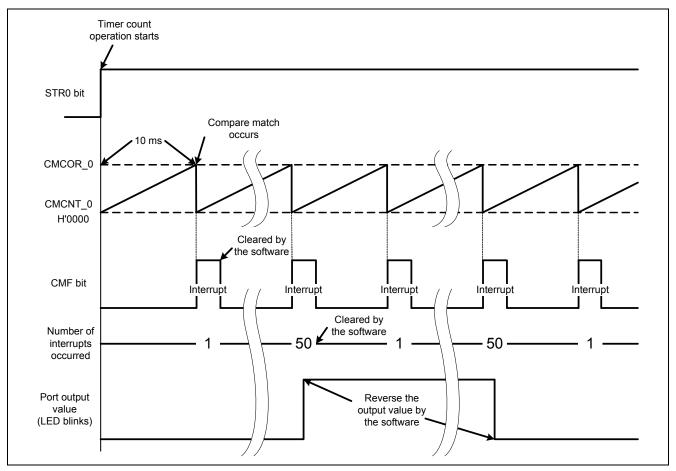


Figure 3 Flow Chart for Configuring the CMT Periodic Count Operation

### 2.3 Sample Program Operation

The sample program uses the CMT (channel 0) interrupt (CMT0). Every time when the number of times of CMI0 reaches 50, the sample program reverses the general-purpose I/O ports (PE) output value, and blinks the LED which is connected to the PE.

Figure 4 shows the operation timing of the sample program.



**Figure 4 Sample Program Operation Timing** 

## 2.4 Sample Program Procedure

Table 2 lists the register settings for the CMT (channel 0). Table 3 lists the register settings for the INTC. Figure 5 and Figure 6 show sample program flow charts.

Table 2 CMT (channel 0) Register Setting

Register Name	Address	Setting	Description
Standby control register 4 (STBCR4)	H'FFFE 040C	H'F7	MSTP42 = "0":     CMT is operating
Compare match timer start register (CMSTR)	H'FFFE C000	H'0000	STR0 = "0":     Stops the count operation
		H'0001	• STR0 = "1": Starts the count operation
Compare match timer control/status register_0 (CMCSR_0)	H'FFFE C002	H'0041	<ul> <li>CMIE = "1": Enables the compare match interrupt</li> <li>CKS [1:0] = "B'01": Clock to input the counter = Pφ/32</li> </ul>
Compare match counter_0 (CMCNT_0)	H'FFFE C004	H'0000	Clears the timer counter
Compare match constant register_0 (CMCOR_0)	H'FFFE C006	D'15624	Compare match interval: 10 ms Note: When the clock to input the counter = $P\phi/32$ , and $P\phi = 50$ MHz

### **Table 3 INTC Register Setting**

Register Name	Address	Setting	Description
Interrupt priority register 08	H'FFFE 0C04	H'1000	CMT0 interrupt priority level = 1
(IPR08)			

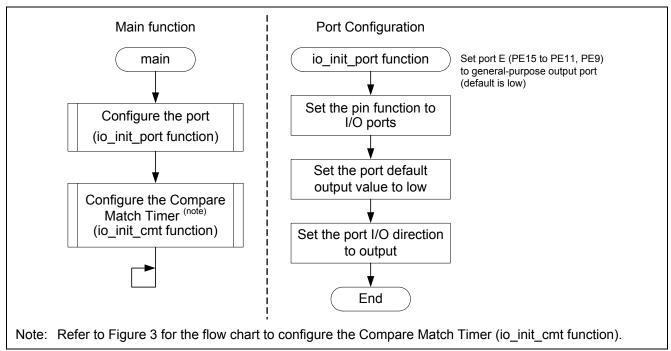


Figure 5 Main Function and Port Configuration (io\_init\_port function) Flow Chart

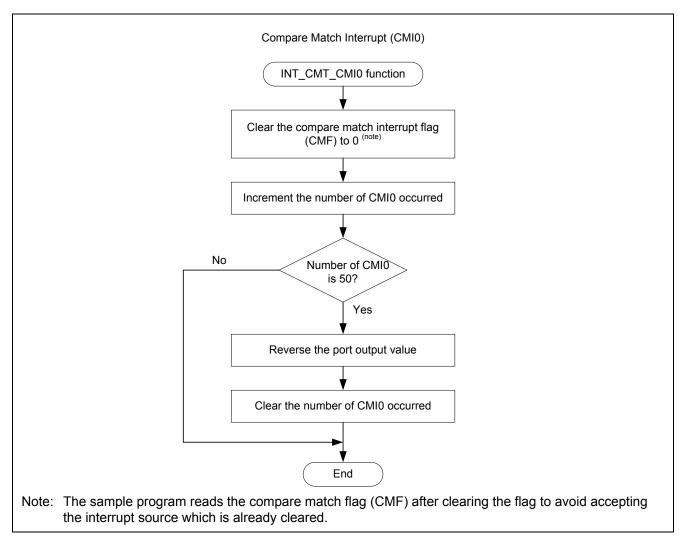


Figure 6 INT\_CMT\_CMI0 Flow Chart

#### 3. Sample Program Listing

## 3.1 Sample Program Listing "main.c" (1/3)

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13
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28
29
    **************************
    /*""FILE COMMENT""******** Technical reference data *****************************
      System Name : SH7216 Sample Program
31
      File Name : main.c
32
       Abstract : Using the Compare Match Timer
33
       Version
                 : 1.00.00
35
                  : SH7216
       Device
36
       Tool-Chain : High-performance Embedded Workshop (Ver. 4.07.00).
37
                 : C/C++ compiler package for the SuperH RISC engine family
38
                                           (Ver.9.03 Release00).
    * OS
                 : None
39
40
       H/W Platform: ROK572167 (CPU board)
41
       Description :
    *******************************
42
       History : Oct.21,2010 Ver.1.00.00
43
    44
45
    #include "iodefine.h"
46
```

### 3.2 Sample Program Listing "main.c" (2/3)

```
47
   /* ==== Prototype declaration ==== */
  void main(void);
49
  void io_init_port(void);
50
  void io_init_cmt(void);
51
  52
53
   * ID
   * Outline : Sample program main
54
56
   * Include
57
   *_____
58
   * Declaration : void main(void);
   * Description : Sample program main
60
61
   *-----
          : void
62
   * Argument
   * Return Value : void
64
65
   67
68
  void main(void)
69
70
   /* ==== Configures the port ==== */
71
   io_init_port();
72
   /* ==== Configures the Compare Match Timer ==== */
73
   io_init_cmt();
74
75
   while(1){
76
77
78
  79
   * ID :
80
   * Outline : Port Configuration
82
          : "iodefine.h"
83
   *-----
   * Declaration : void io_init_port(void);
86
   *-----
87
   * Description : Configures port E (PE15 to PE11, PE9).
   * Argument
89
          : void
   *_____
90
   * Return Value : void
91
93
   * Note : None
   94
95
  void io_init_port(void)
96
```

### 3.3 Sample Program Listing "main.c" (3/3)

```
97
      /* ---- Sets the pin function ---- */
      PFC.PECRL4.WORD = 0...

PFC.PECRL3.BIT.PE11MD = 0;
      PFC.PECRL4.WORD = 0x0000; /* PE15 to 12: I/O ports */
                              /* PE11: I/O ports */
99
                               /* PE9: I/O ports */
     PFC.PECRL3.BIT.PE9MD = 0;
100
101
     /* ---- Sets the default data ---- */
     PE.DR.WORD = 0x0000; /* PE15 to PE11, PE9: Default value is low */
103
     /* ---- Sets the I/O direction ---- */
     PFC.PEIORL.WORD |= 0xfa00; /* PE15 to PE11, PE9: Output */
104
105
106
     107
     * ID :
108
109
     * Outline
                : CMT configuration
     *-----
110
     * Include
                : "iodefine.h"
111
112
     *-----
113
     * Declaration : void io_init_cmt(void);
114
     * Description : Sets CMT channel 0 as a 10-ms periodic timer.
115
116
117
     * Argument
                : void
118
119
     * Return Value : void
120
121
     * Note
                 : None
     122
123    void io_init_cmt(void)
124 {
125
      /* ---- Module standby clear ---- */
                               /* Supplies the clock to the CMT */
126
     STB.CR4.BIT.\_CMT = 0;
127
128
     /* ---- Stops the count operation ---- */
129
     CMT.CMSTR.BIT.STR0 = 0;
130
     /* ---- Enables interrupts/sets the clock to input the counter ---- */
     CMT0.CMCSR.WORD = 0x0041; /* Enables CMI0, the clock to input the counter is */
131
                            /* P-clock/32 */
132
133
     /* ---- Clears the counter ---- */
134
      CMT0.CMCNT = 0 \times 0000;
135
      /* ---- Sets the count operation interval ---- */
136
      CMTO.CMCOR = 15625 - 1; /* 10 ms (P-clock/32, P-clock = 50 MHz) */
137
      /* ---- Sets the interrupt priority level---- */
138
139
     INTC.IPR08.BIT._CMT0 = 1;  /* CMI0 priority = 1 */
140
141
      /* ---- Starts the count operation ---- */
142
      CMT.CMSTR.BIT.STR0 = 1;
143
   }
144
145 /* End of File */
```

### 3.4 Sample Program Listing "intprg.c" (1/2)

```
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28
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    *****************************
29
    30
31
       System Name : SH7216 Sample Program
32
       File Name : intprg.c
33
       Abstract : Interrupt Functions
34
      Version : 1.00.00
35
                 : SH7216
      Tool-Chain : High-performance Embedded Workshop (Ver.4.07.00).
36
37
                  : C/C++ compiler package for the SuperH RISC engine family
38
                                           (Ver.9.03 Release00).
39
       OS
                 : None
40
       H/W Platform: ROK572167 (CPU board)
41
      Description :
    *************************
42
                 : Oct.21,2010 Ver.1.00.00
43
      History
    44
45
    #include <machine.h>
46
    #include "vect.h"
47
    #include "iodefine.h"
48
49
    /* ==== CMI0 occur counter ==== */
50
   int cmi0_count = 0;
51
```

### 3.5 Sample Program Listing "intprg.c" (2/2)

```
52
    #pragma section IntPRG
53
   // 4 Illegal code
54
   void INT_Illegal_code(void){/* sleep(); */}
55
   (omitted)
   // 140 CMT CMI0
326
    327
328
    * Outline
329
             : Compare match interrupt (CMIO).
330
    *-----
             : "vect.h" and "iodefine.h"
    *-----
332
    * Declaration : void INT_CMT_CMIO(void);
333
334
    *-----
335
    * Description : Counts the number of CMIO occurred. Every time when the number
336
             : reaches 50, it reverses port E (PE15 to PE11, PE9) output data
337
             : and changes the LED display pattern.
338
339
    * Argument
             : void
340
341
    * Return Value : void
343
              : None
    344
345
   void INT_CMT_CMI0(void)
346 {
                         /* Clears the compare match flag (CMF) */
347
    CMT0.CMCSR.BIT.CMF = 0;
                         /* Dummy read the CMF */
348
    CMT0.CMCSR.BIT.CMF;
349
    cmi0_count++;
350
                         /* Increments the number of CMIO occurred */
351
352
    /* ==== LED blinking ==== */
    if(cmi0_count == 50){
                         /* Number of CMIO is 50? */
     354
355
356
357
   }
   (omitted)
592
   /* End of File */
```

#### 4. References

#### • Software Manual

SH-2A/SH2A-FPU Software Manual Rev. 3.00

The latest version of the software manual can be downloaded from the Renesas Electronics website.

#### • Hardware Manual

SH7214 Group, Group User's Hardware Manual Rev. 2.00

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### Description

Rev.	Date	Page	Summary
1.00	Jan.11.11	_	First edition issued

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#### 1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

— The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

### 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
- 3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

The reserved addresses are provided for the possible future expansion of functions. Do not access
these addresses; the correct operation of LSI is not guaranteed if they are accessed.

#### 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
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