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SH7145 Group

LED Control by Periodic Counting Operation of the Compare Match Timer

Introduction

An interrupt is generated at a specific period by using the channel 0 of the CMT (compare-match timer). LEDs are connected to the general port (port C) to flash alternately on and off every time an interrupt occurs.

Target Device

SH7145F

Contents

1. Specifications

An interrupt is generated at a specific period by using the channel 0 of the SH7145's CMT(compare-match timer). LEDs are connected to the general port (port C) to flash alternately on and off every time an interrupt occurs. The GL3PR8 manufactured by Sharp Corporation is used as LEDs.

Figure 1 shows the connections between the SH7145F and LEDs. Table 1 summarizes the LED specifications.

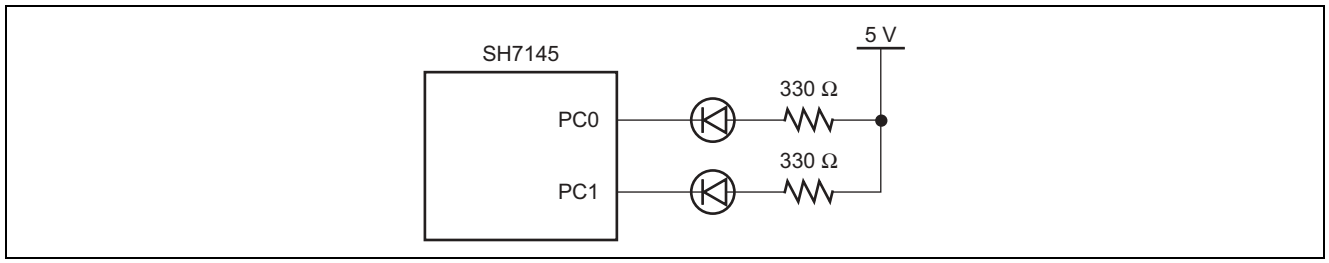


Figure 1 Connections between SH7145F and LEDs

Table 1 LED (GL3PR8) Absolute Maximum Ratings

Model	Emitting Color	Material	Permissible Power Dissipation P (mW)	Forward Current I_F (mA)	Peak Forward Current I_{FM}* (mA)	Derating Factor (mA/°C)		Reverse Voltage V_R (V)
						DC	Pulse	
GL3PR8	Red	GaP	23	10	50	0.13	0.67	5

Note: Duty cycle = 1/10, Pulse width = 0.1 ms

2. Description of Functions

In this sample task, two LEDs are controlled by the compare match timer (CMT) and the general port (port C). Figure 2 shows the function block diagram.

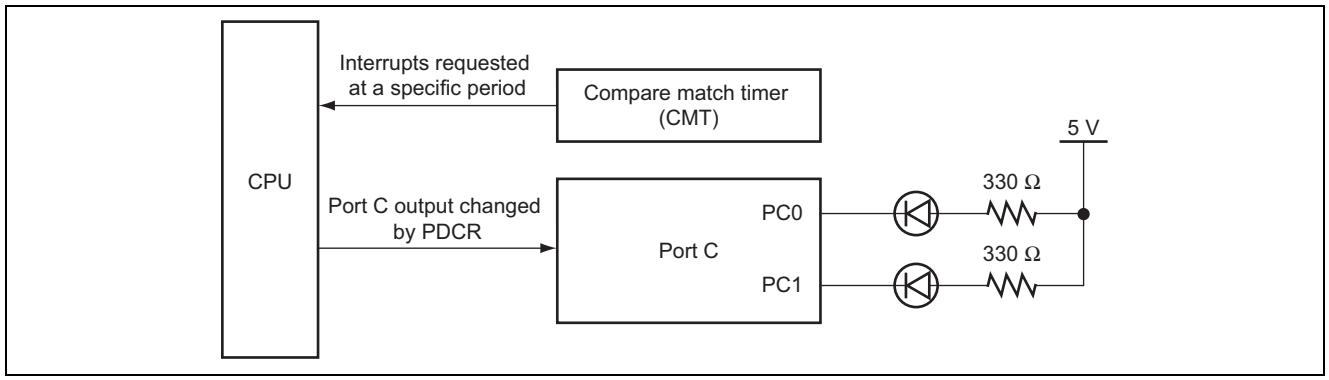


Figure 2 Function Block Diagram

2.1 Compare Match Timer (CMT)

The CMT generates an interrupt at a given period. Figure 3 shows a block diagram of the CMT module channel 0 (ch0). Its functions are described below.

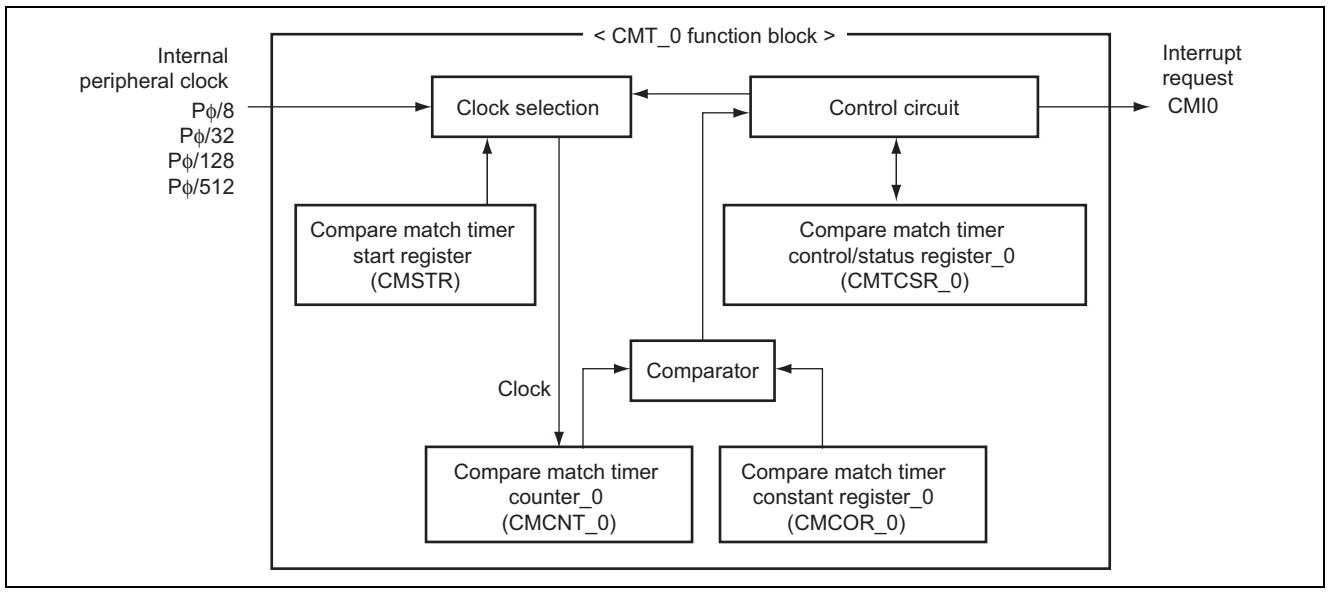


Figure 3 CMT Channel 0 Block Diagram

- The CMT has a 16-bit counter and can generate interrupts at a specified period.
- A clock generated by dividing the internal peripheral clock Pϕ can be selected as a CMT clock. The CMT increments based on the selected clock.
- The compare match timer start register (CMSTR) starts or stops counting.
- The compare match timer control/status register (CMCSR_0) indicates a compare match occurrence, enables the interrupt, and selects the clock for counting.
- The compare match timer counter (CMCNT_0) is an up-counter to generate an interrupt request on a compare match between the CMCNT_0 and CMCOR_0 registers.
- The compare match timer constant register (CMCOR_0) sets the period to generate a compare match.

2.2 General Port (Port C)

In this sample task, LEDs are connected to a general port (port C). The PC0 and PC1 of port C are used to control the LEDs. Figure 4 shows a block diagram of port C. The function of port C is summarized below.

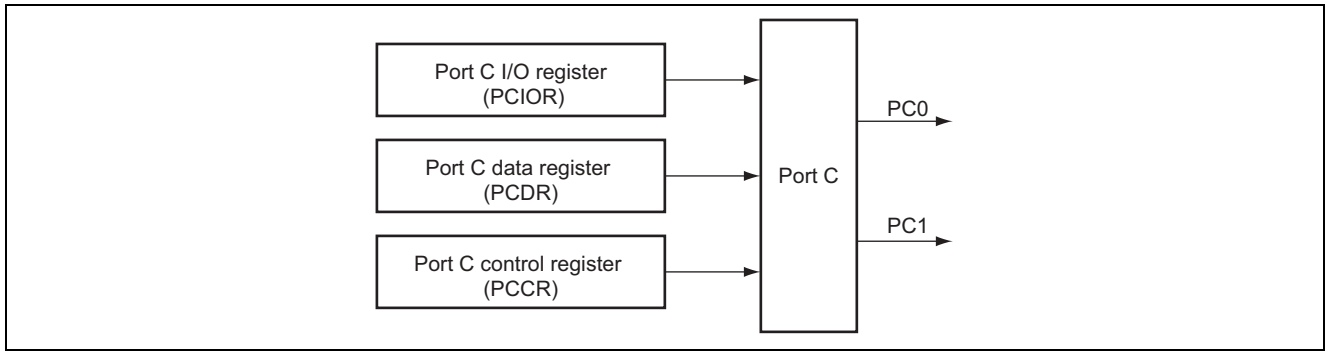


Figure 4 Port C Block Diagram

- Port C is a 16-bit general I/O port.
- The port C control register (PCCR) selects the function of multiplexed pins.
- The port C I/O register (PCIOR) selects the input or output direction of the pins. The PCIOR is valid only when the pins of the port C function as general I/O pins; it is invalid otherwise.
- The port C data register (PCDR) stores the data of port C. If port C functions as a general output, data written to PCDR is output directly from the corresponding pin. If the port C functions as a general input, the pin status can be read directly by reading the PCDR.

3. Principles of Operation

Figure 5 shows the CMT interrupt and port C output change in this sample task.

Table 2 shows the software and hardware processing performed in the operation shown in figure 5.

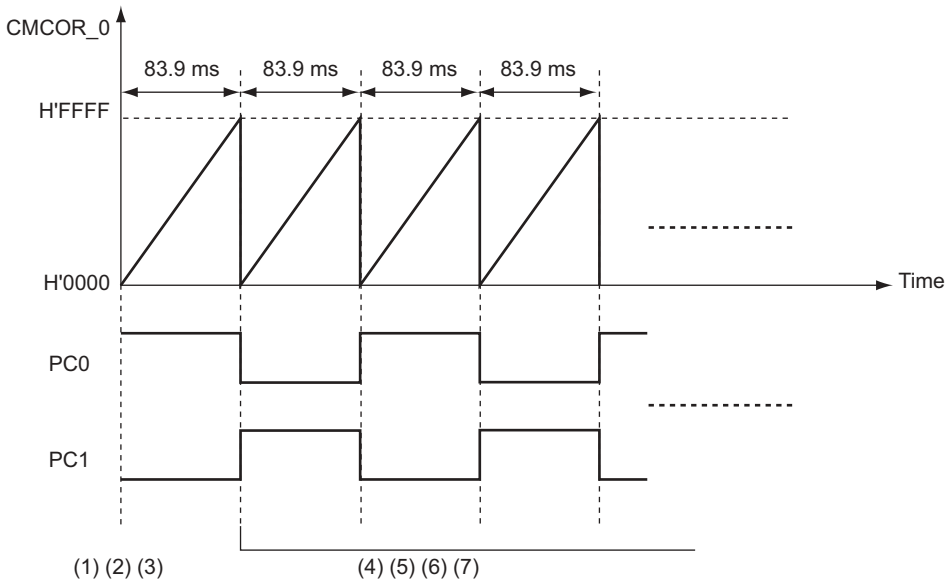


Figure 5 CMT Interrupt and Port Outputs

Table 2 Software and Hardware Processing

No.	Software Processing	Hardware Processing
(1)	Set the levels of output from PC0 and PC1 in PCDR.	—
(2)	Set the interrupt period in CMCOR_0.	—
(3)	Set the STR0 bit in CMSTR to 1.	Start counting by CMT_0.
(4)	—	Set the CMF flag (a compare match interrupt occurs).
(5)	Clear the CMF flag.	Start counting by CMT_0.
(6)	Set PCDR to invert the output levels on PC0 and PC1.	—
(7)	Repeat steps (4) to (6) above.	Repeat steps (4) to (6) above.

4. Description of Software

4.1 Modules

Table 3 shows the modules used in this sample task.

Table 3 Description of Modules

Module Name	Label Name	Function
Main routine	main	Initializes the CMT0 and port C, and starts counting.
CMT0 interrupt routine	cmt_int	Inverts the port C outputs.

4.2 Internal Registers

Tables 4 and 5 describe the internal registers used in this sample task. The setting values in these tables are the values used in this sample task and not the initial values.

Table 4 Description of Internal Registers (1)

Register Name	Bit	Bit Name	Setting Value	Function
MSTCR2				Module standby control register 2
	12	MSTP12	0	CMT standby control bit When MSTP12 = 0, the CMT's standby state is cancelled.
CMSTR			H'01	Compare match timer start register
	15 to 2	—	0	Reserved bits
	1	STR1	0	Count start 1 When STR1 = 0, the CMCNT_1 stops counting.
	0	STR0	1	Count start 0 When STR0 = 1, the CMCNT_0 starts counting.
CMCSR_0				Compare match timer control/status register_0
	15 to 8	—	0	Reserved bits
	7	CMF	*	Compare match flag When CMF = 1, the CMCNT matches the CMCOR.
	6	CMIE	1	Compare match interrupt enable Enables or disables the compare match interrupt. When CMIE = 1, the compare match interrupt is enabled.
	5 to 2	—	0	Reserved bits
	1, 0	CKS1 CKS0	0 1	CMCNT_0 input clock selection In this sample task, Pϕ/32 is selected.
CMCNT_0			—	Compare match timer counter_0 Up-counter to generate interrupt requests.
CMCOR_0			H'FFFF	Compare match timer constant register Sets the period of compare match with CMCNT_0.

Note: * This bit can only be cleared to 0. This bit is automatically set to 1 by hardware.

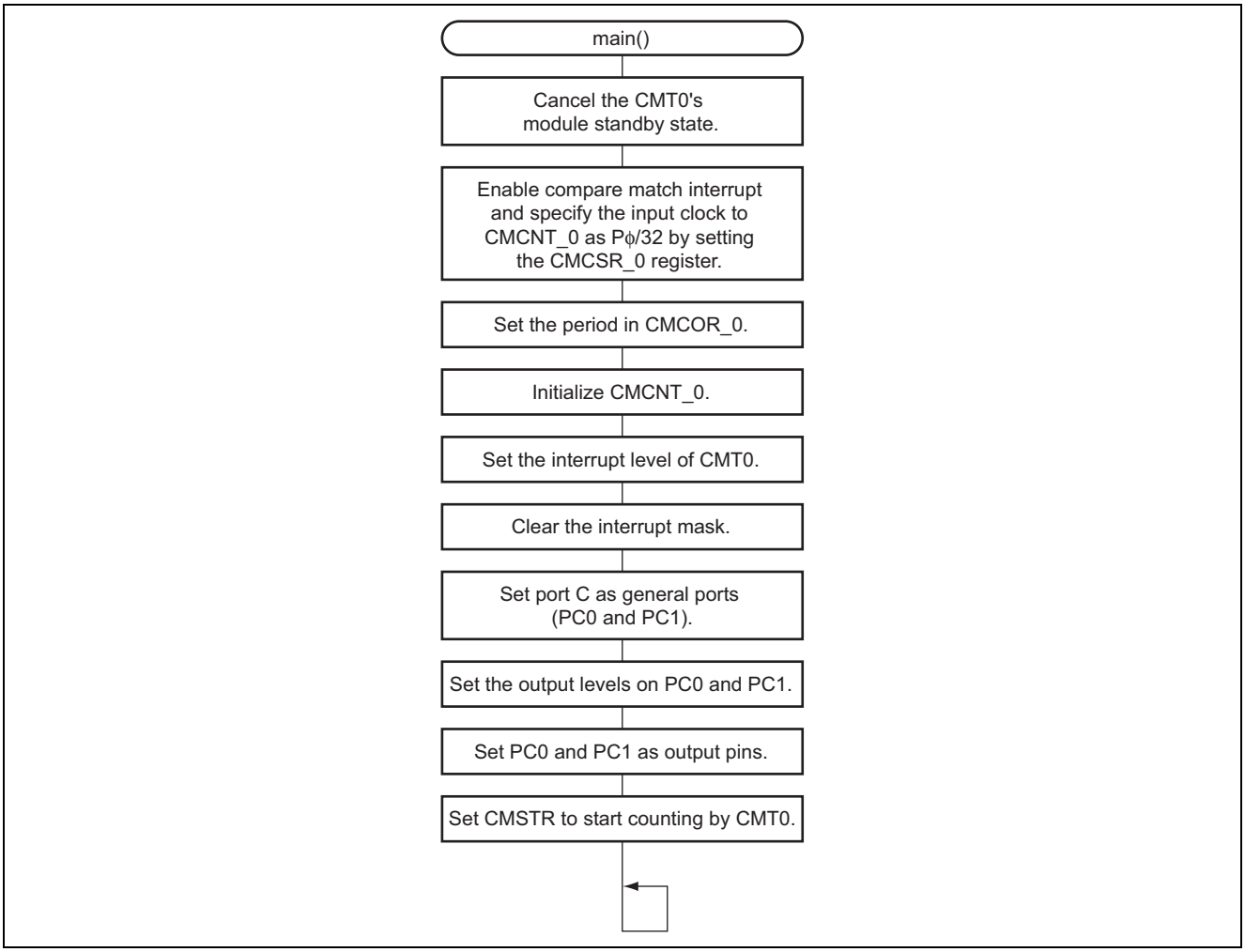
Table 5 Description of Internal Registers (2)

Register Name	Bit	Bit Name	Setting Value	Function
IPRG			H'00F0	Interrupt priority register G Sets the priorities of interrupt sources.
	7 to 4	IPR7	1	Set the priority of the CMT0 interrupt (0 to 15).
		IPR6	1	
		IPR5	1	
		IPR4	1	
PCCR			H'00	Port C control register Sets port C pin functions.
	1	PC1MD	0	When PC1MD = 0, the corresponding pin functions as a general port.
	0	PC0MD	0	When PC0MD = 0, the corresponding pin functions as a general port.
PCIOR			H'03	Port C I/O register Sets the port C input or output.
	1	PC1IOR	1	When PC1IOR = 1, PC1 functions as an output.
	0	PC0IOR	1	When PC0IOR = 1, PC0 functions as an output.
PCDR				Port C data register
	1	PC1DR	*	When PC1 functions as a general output pin, the value of PC1DR is output.
	0	PC0DR	*	When PC0 functions as a general output pin, the value of PC0DR is output.

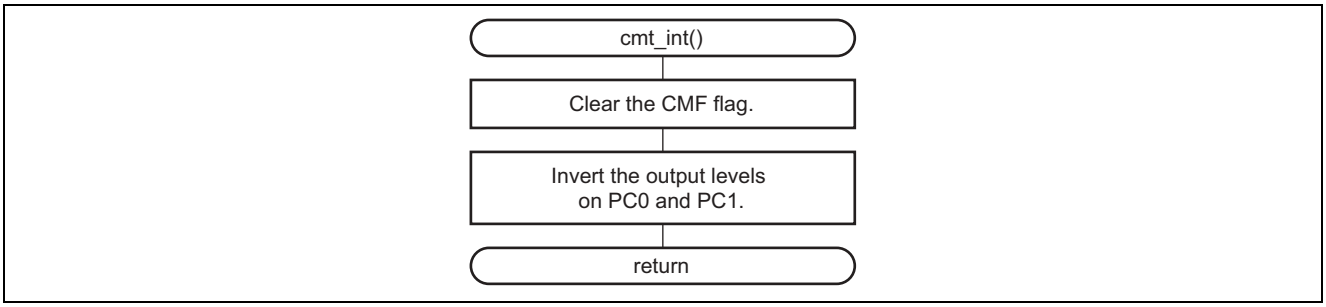
Note: * The values of these bits are changed by software every time a compare match interrupt occurs.

5. Flowchart

5.1 Main Routine



5.2 Compare Match Interrupt Routine



6. Program Listing

```
/************************************************************************************************/
/* SH7145F Application Note                                                                     */
/*                                                                                              */
/* Function                                                                                     */
/*   :CMT0                                                                                      */
/*                                                                                              */
/* External input clock       :12.5MHz                                                          */
/* Internal CPU clock         :50MHz                                                            */
/* Internal peripheral clock  :25MHz                                                            */
/*                                                                                              */
/* Written      : 2003/10     Rev.1.0                                                           */
/************************************************************************************************/

#include "iodefine.h"
#include <machine.h>

/*------------ Function Definition ---------------------------------------------------------*/
void main(void);

void cmt_int(void);
void dummy_f(void);

/************************************************************************************************/
/*  main Program                                                                                */
/************************************************************************************************/
void main( void )
{
   P_STBY.MSTCR2.BIT.MSTP12 = 0;             /* disable CMT0 standby mode                      */

   P_CMT.CMCSR_0.WORD = 0x0041;              /* initialize CMCSR_0                             */
           // [15-8]  = 0
           // [7]CMF  = 0
           // [6]CMIE = 1   CMT0 interrupt enable
           // [5-2]   = 0
           // [1]CKS1 = 0
           // [0]CKS0 = 1   count clock P phi/32
   P_CMT.CMCOR_0 = 0xFFFF;                   /* set CMCOR_0                                    */
   P_CMT.CMCNT_0 = 0;                        /* initialize CMCNT_0                             */

   P_INTC.IPRG.BIT.CMT0 = 0xF;               /* interruption level of CMT0                     */
   set_imask(0);

   P_PORTC.PCCR.WORD &= 0xFFFC;              /* set function PC0,PC1                           */
   P_PORTC.PCDR.WORD = 0x0001;               /* PC0 -> H,PC1 -> L                              */
   P_PORTC.PCIOR.WORD |= 0x0003;             /* portC output                                   */

   P_CMT.CMSTR.BIT.STR = 1;                  /* count start                                    */

   while(1);                                 /* LOOP                                           */
}
```

```
/************************************************************************************************/
/*  Interruption Program                                                                        */
/************************************************************************************************/
#pragma interrupt(cmt_int)
void cmt_int(void)
{
   P_CMT.CMCSR_0.BIT.CMF = 0;               /* CMF clear                                       */

   P_PORTC.PCDR.WORD = ~P_PORTC.PCDR.WORD;  /* output reversal                                 */
}

#pragma interrupt(dummy_f)
void dummy_f(void)
{
                                            /* Other Interrupt                                 */
}
```

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Sep.16.04	—	First edition issued

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