RX63N Group, RX631 Group

Application Example of Exclusive Operation of Two Motors by One Set of Complementary PWM Outputs

R01AN1068EJ0101
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Abstract

This application note describes an example of exclusive operation of two motors by one set of three-phase complementary pulse width modulation (PWM) outputs using multi-function timer pulse unit 2 (MTU).

Products

- RX63N Group, 177- and 176-pin versions, ROM capacity: 768 KB to 2 MB
- RX63N Group, 145- and 144-pin versions, ROM capacity: 768 KB to 2 MB
- RX63N Group, 100-pin version, ROM capacity: 768 KB to 2 MB
- RX631 Group, 177- and 176-pin versions, ROM capacity: 256 KB to 2 MB
- RX631 Group, 145- and 144-pin versions, ROM capacity: 256 KB to 2 MB
- RX631 Group, 100-pin version, ROM capacity: 256 KB to 2 MB

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

Using the MTU's complementary PWM mode 3, three-phase complementary PWM waveforms and a toggle waveform synchronized with the PWM cycle are output. A dead time is specified for the complementary PWM outputs to ensure a non-overlapping relationship between the positive-phase and negative-phase pulses.

After a reset is canceled, complementary PWM waveforms are output on PWM output pin group 0 (PC5, PC4, PB3, PB1, PC2, and PC3). When a switch input is detected, the waveforms are output on PWM output pin group 1 (PB7, PB6, PE2, PE1, PE3, and PE4) takes place. Thereafter, the waveforms are output alternately from PWM output pin group 0 and group 1 each time a switch input is detected.

- PWM cycle: 200 μs
- PWM duty: Changes each PWM cycle (initial value: 50%)
- PWM active level: Low level
- Dead time: 4 μs

Table 1.1 lists the peripheral functions used and their applications, and figure 1.1 is a block diagram.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	Application
MTU2a channel 3 (MTU3)	Complementary PWM output and PWM cycle toggle output
MTU2a channel 4 (MTU4)	Complementary PWM output
MPC	Complementary PWM output pin switching

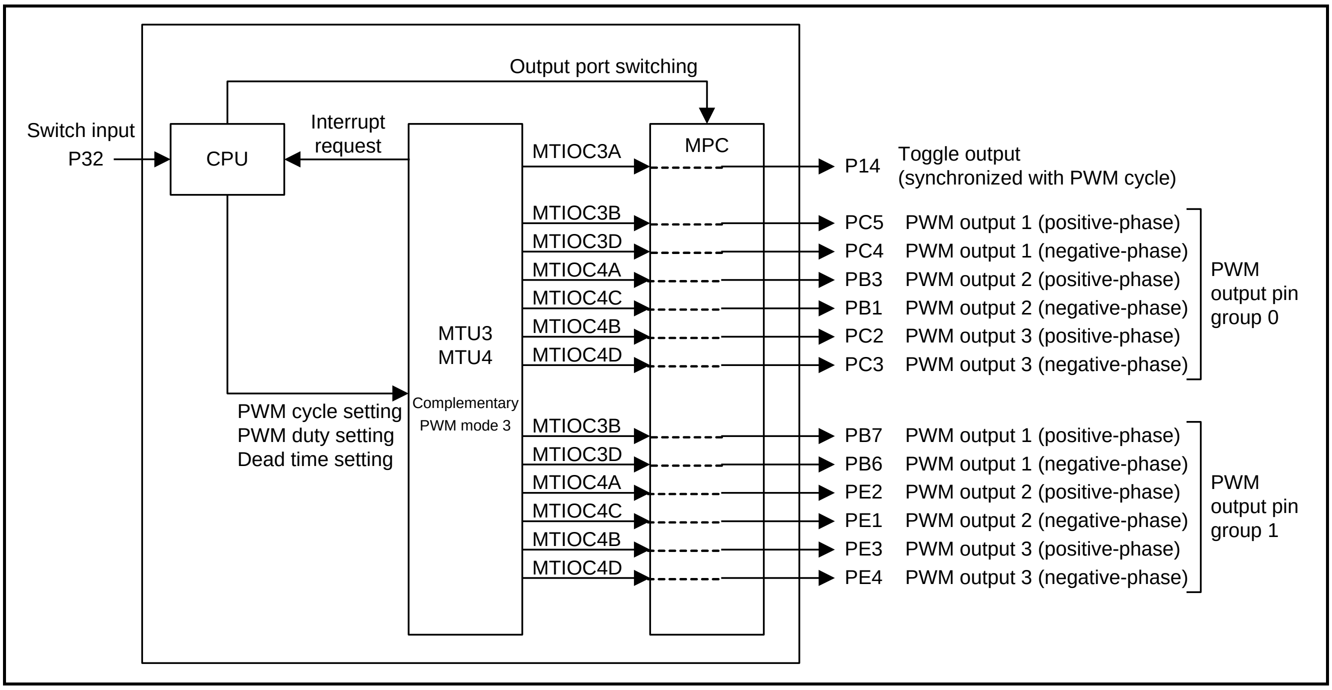

Figure 1.1 Block Diagram

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
Microcontroller used	R5F563NBDDFC (RX63N Group)
Operating frequency	Main clock: 12 MHz PLL: 192 MHz (main clock divided by 1 and multiplied by 16) System clock (ICLK): 96 MHz (PLL divided by 2) Peripheral module clock B (PCLKB): 48 MHz (PLL divided by 4)
Operating voltage	3.3 V
Integrated development environment	Renesas Electronics Corporation High-performance Embedded Workshop Version 4.09.01
C compiler	Renesas Electronics Corporation C/C++ Compiler Package for RX Family V.1.02 Release 01
	Compiler options -cpu=rx600 -output=obj="$(CONFIGDIR)\$(FILELEAF).obj" -debug -nologo (The integrated development environment default settings are used.)
iodefine.h version	Version 1.80
Endian order	Little endian
Operating mode	Single-chip mode
Processor mode	Supervisor mode
Sample code version	Version 1.01
Board used	Renesas Starter Kit for RX63N (product No.: R0K50563NC010BR)

3. Reference Application Note

For additional information associated with this document, refer to the following application note.

- RX63N Group, RX631 Group: Initial Setting, (R01AN1245EJ)

The initial setting function described in the above application note is used by the sample code in this application note.

The latest version can be obtained from the Renesas Electronics Web site. If a newer version is available, replace the the current version with the newest version.

4. Hardware

4.1 Hardware Configuration

Figure 4.1 shows a connection example.

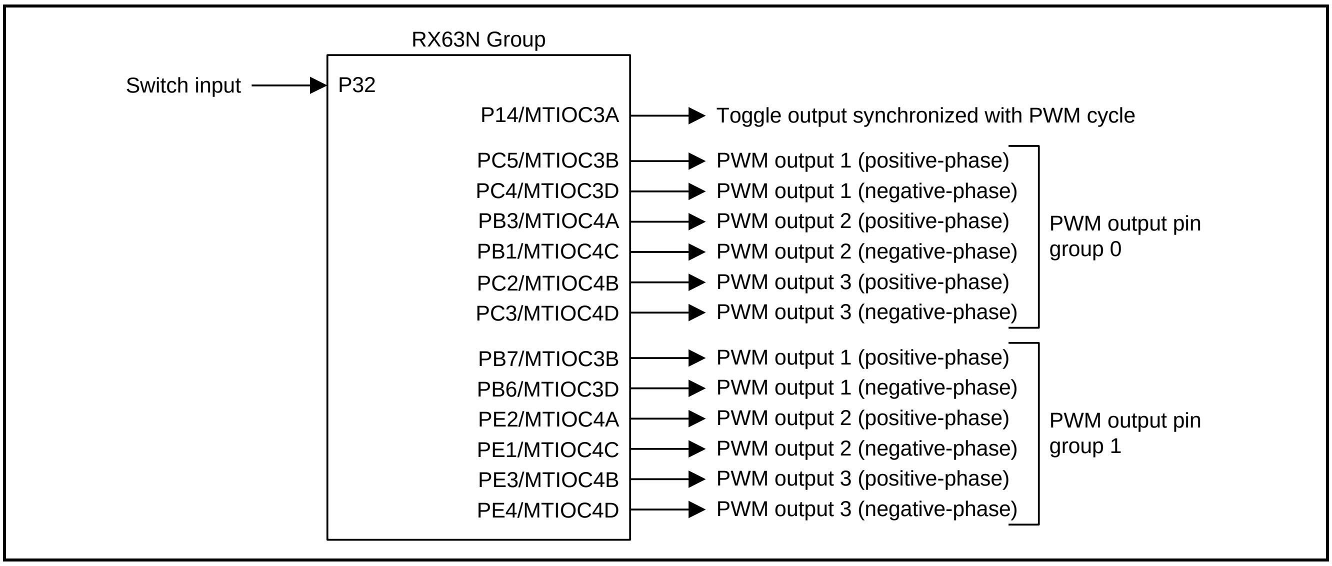

Figure 4.1 Connection Example

4.2 Pins Used

Table 4.1 lists the pins used and their functions.

Table 4.1 Pins Used and Their Functions

Pin Name	I/O	Function
P32	Input	Switch input for changing PWM output pin group
P14/MTIOC3A	Output	PWM cycle toggle output
PC5/MTIOC3B	Output	PWM output 1 (positive-phase) PWM output pin group 0
PC4/MTIOC3D	Output	PWM output 1 (negative-phase) PWM output pin group 0
PB3/MTIOC4A	Output	PWM output 2 (positive-phase) PWM output pin group 0
PB1/MTIOC4C	Output	PWM output 2 (negative-phase) PWM output pin group 0
PC2/MTIOC4B	Output	PWM output 3 (positive-phase) PWM output pin group 0
PC3/MTIOC4D	Output	PWM output 3 (negative-phase) PWM output pin group 0
PB7/MTIOC3B	Output	PWM output 1 (positive-phase) PWM output pin group 1
PB6/MTIOC3D	Output	PWM output 1 (negative-phase) PWM output pin group 1
PE2/MTIOC4A	Output	PWM output 2 (positive-phase) PWM output pin group 1
PE1/MTIOC4C	Output	PWM output 2 (negative-phase) PWM output pin group 1
PE3/MTIOC4B	Output	PWM output 3 (positive-phase) PWM output pin group 1
PE4/MTIOC4D	Output	PWM output 3 (negative-phase) PWM output pin group 1

5. Software

After the initial settings, a toggle waveform synchronized with the PWM cycle, and three-phase complementary PWM waveforms on PWM output pin group 0, are output.

When a switch input is detected, the complementary PWM waveform output destination is switched between PWM output pin group 0 and group 1 alternately. The carrier cycle of the PWM output is 200 µs. This interrupt every 200 µs is used to generate 5 ms of switch input read cycle, and an input is determined when the switch input level matches three times in succession.

The peripheral function settings used are listed below.

MTU (MTU3 and MTU4)

- Counter clock: PCLKB/4 rising edge
- Operation mode: Complementary PWM mode 3 (transfer at crest and trough)
- Dead time: 4 µs
- Carrier cycle (PWM cycle): 200 µs (carrier frequency: 5 kHz)
- TDDR register: Sets offset value of MTU4.TCNT and MTU3.TCNT (dead time)
  (setting value: 48 = 4 µs / counter clock cycle)
- TCDR register: Sets MTU4.TCNT upper limit value (1/2 of carrier cycle)
  (setting value: 1200 = 100 µs / counter clock cycle)
- TCBR register: Operates as buffer register of TCDR register
- MTU3.TGRA register: Sets MTU3.TCNT upper limit value (1/2 of carrier cycle + dead time)
  (setting value: 1248 = 1200 + 48)
- MTU3.TGRB register: Sets duty of PWM output 1 (initial value: 50%)
  (setting value: 600 = 1200 / 2)
- MTU3.TGRC register: Operates as buffer register of MTU3.TGRA register
- MTU3.TGRD register: Operates as buffer register of MTU3.TGRB register
- MTU4.TGRA register: Sets duty of PWM output 2 (initial value: 50%)
  (setting value: 600 = 1200 / 2)
- MTU4.TGRB register: Sets duty of PWM output 3 (initial value: 50%)
  (setting value: 600 = 1200 / 2)
- MTU4.TGRC register: Operates as buffer register of MTU4.TGRA register
- MTU4.TGRD register: Operates as buffer register of MTU4.TGRB register
- Positive-phase output levels: Initial output: High
  Active level: Low
  Compare match output (up counter): Low
  Compare match output (down counter): High
- Negative-phase output levels: Initial output: High
  Active level: Low
  Compare match output (up counter): High
  Compare match output (down counter): Low
- PWM sync output: Toggle output enabled
- PWM output pin 1: MTIOC3B and MTIOC3D pin output enabled
- PWM output pin 2: MTIOC4A and MTIOC4C pin output enabled
- PWM output pin 3: MTIOC4B and MTIOC4D pin output enabled
- Counter clearing: Clearing TCNT disabled
- Interrupt: Use TGR interrupt request A (MTU3.TGIA3)

5.1 Operation

(1) Initial Settings

After the initial settings, a toggle waveform synchronized with the PWM cycle, and three-phase complementary PWM waveforms on PWM output pin group 0, are output.

(2) TGIA3 Interrupt Handler

The interrupt handler for TGIA3, which is generated every 200 µs, increments (+1) the switch read cycle counter for measuring 5 ms intervals, and changes the PWM output duty.

(3) Switch Input Determination

When the switch input level, which is read every 5 ms, matches three times consecutively, the switch input determination flag is set to 1.

(4) PWM Output Pin Group Switching

When the switch input determination flag is set to 1, PWM output pin group 0 is set as general input ports and group 1 is set as PWM output pins. The output of PWM output pin group 0 becomes high-impedance, and complementary PWM waveforms are output on group 1.

Figure 5.1 is a timing chart.

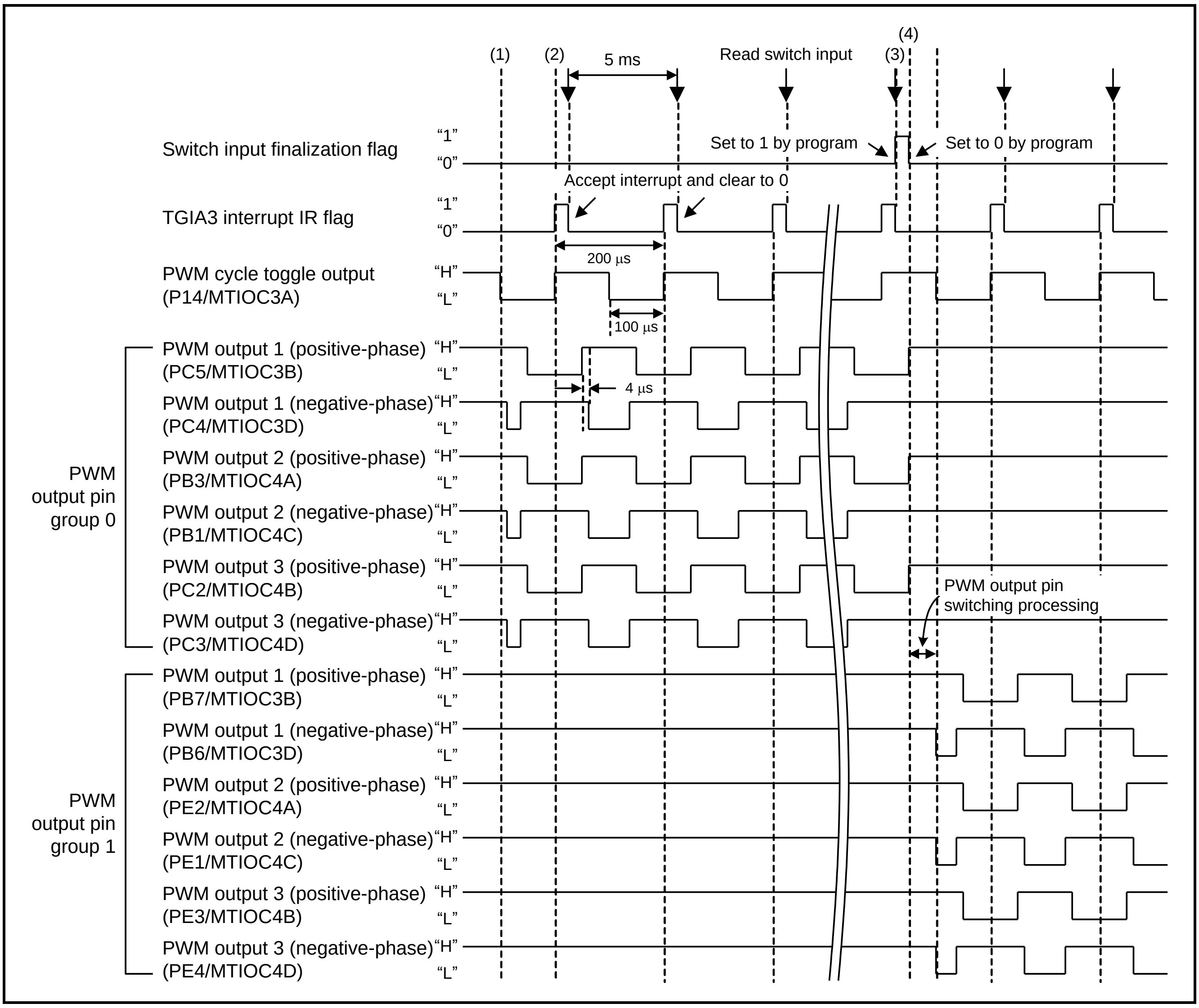

Figure 5.1 Timing Chart

5.2 File Composition

Table 5.1 lists the files used in the sample code. Files generated by the integrated development environment are not included in this table.

Table 5.1 Files Used in the Sample Code

File Name	Outline	Remarks
main.c	Main processing	
r_init_stop_module.c	Stop processing for peripheral functions that are active after a reset	
r_init_stop_module.h	r_init_stop_module.c header file	
r_init_non_existent_port.c	Nonexistent port initialization	
r_init_non_existent_port.h	r_init_non_existent_port.c header file	
r_init_clock.c	Clock initialization	
r_init_clock.h	r_init_clock.c header file	

5.3 Option-Setting Memory

Table 5.2 lists the option-setting memory configured in the sample code. When necessary, set a value suited to the user system.

Table 5.2 Option-Setting Memory Configured in the Sample Code

Symbol	Address	Setting Value	Contents
OFS0	FFFF FF8Fh to FFFF FF8Ch	FFFF FFFFh	IWDT is stopped after a reset. WDT is stopped after a reset.
OFS1	FFFF FF8Bh to FFFF FF88h	FFFF FFFFh	Voltage monitor 0 reset is disabled after a reset. HOCO oscillation is disabled after a reset.
MDES	FFFF FF83h to FFFF FF80h	FFFF FFFFh	Little endian

5.4 Constants

Table 5.3 lists the constants used in the sample code.

Table 5.3 Constants Used in the Sample Code

Constant Name	Setting Value	Contents
SW_NUM	3	Switch match determination count
SW_CYCLE	25	Switch read cycle: 5 ms = PWM cycle (200 µs) × 25
LOW	0	Low level
HIGH	1	High level
PWM_GROUP_0	0	PWM output pin group 0
PWM_GROUP_1	1	PWM output pin group 1
PWM_DEAD_TIME	48	Dead time: 4 µs = MTU counter clock cycle (1/12 MHz) × 48
PWM_CYCLE	1200	1/2 of carrier cycle: 100 µs = MTU counter clock cycle (1/12 MHz) × 1200
PWM_MAX	(PWM_CYCLE + PWM_DEAD_TIME)	MTU3.TCNT upper limit value: 104 µs
PWM_DUTY_50	(PWM_CYCLE / 2)	PWM duty setting value: 50%
PWM_DUTY_ADD	0	PWM duty setting value state: Add
PWM_DUTY_SUB	1	PWM duty setting value state: Subtract

5.5 Variables

Table 5.4 lists the global variables.

Table 5.4 Global Variables

Type	Variable Name	Contents	Function Used
unsigned char	sw_cycle_cnt	Switch read cycle counter for measuring 5 ms intervals	main Excep_MTU3_TGIA3
unsigned char	sw_match_cnt	Switch match counter	sw_input_check
unsigned char	sw_level_last	Switch previous level	sw_input_check
unsigned char	sw_level_fix	Switch determination level	sw_input_check
unsigned char	sw_fix_flag	Switch input determination flag 0: Not determined 1: Determined (switch input falling edge detected)	main sw_input_check
unsigned char	pwm_pin	PWM output pin	pwm_pin_change
unsigned char	pwm_duty_state	PWM duty setting value state	Excep_MTU3_TGIA3
unsigned short	pwm_1_duty	PWM output 1 duty setting value	Excep_MTU3_TGIA3
unsigned short	pwm_2_duty	PWM output 2 duty setting value	Excep_MTU3_TGIA3
unsigned short	pwm_3_duty	PWM output 3 duty setting value	Excep_MTU3_TGIA3

5.6 Functions

Table 5.5 lists the functions used in the sample code.

Table 5.5 Functions Used in the Sample Code

Function Name	Outline
main	Main processing
port_init	Port initialization
R_INIT_StopModule	Stop processing for active peripheral functions after a reset
R_INIT_NonExistentPort	Nonexistent port initialization
R_INIT_Clock	Clock initialization
peripheral_init	Peripheral function initialization
mtu_init	MTU initialization
pwm_pin_change	PWM output pin switching
pwm_pin_group_0	PWM output pin group 0 settings
pwm_pin_group_1	PWM output pin group 1 settings
sw_input_check	Switch input determination
Excep_MTU3_TGIA3	MTU3.TGIA3 interrupt handler

5.7 Function Specifications

The following tables list the sample code function specifications.

main	
Outline	Main processing
Header	None
Declaration	void main(void)
Description	After initialization, determine the input level of the switch input for changing PWM output pin group every 5 ms. When the switch input determination flag is set to 1, change the PWM output pins.
Arguments	None
Return Value	None

port_init	
Outline	Port initialization
Header	None
Declaration	void port_init(void)
Description	Initialize the ports.
Arguments	None
Return Value	None

R_INIT_StopModule	
Outline	Stop processing for active peripheral functions after a reset
Header	r_init_stop_module.h
Declaration	void R_INIT_StopModule(void)
Description	Configure the setting to enter the module stop-state.
Arguments	None
Return Value	None
Remarks	Transition to the module-stop state is not performed in the sample code. Refer to the application note RX63N Group, RX631 Group: Initial Setting, Rev. 1.00, for details of this function.

R_INIT_NonExistentPort	
Outline	Nonexistent port initialization
Header	r_init_non_existent_port.h
Declaration	void R_INIT_NonExistentPort(void)
Description	Initialize port direction registers for ports that do not exist in products with less than 176 pins.
Arguments	None
Return Value	None
Remarks	The number of pins in the sample code is set for the 176-pin package (PIN_SIZE=176). After this function is called, when writing in byte units to the PDR registers that have nonexistent ports, set the bits corresponding to nonexistent ports as follows: set the I/O select bits to 1 and set the output data store bits to 0. Refer to the application note RX63N Group, RX631 Group: Initial Setting, Rev. 1.00, for details of this function.

R_INIT_Clock	
Outline	Clock initialization
Header	r_init_clock.h
Declaration	void R_INIT_Clock(void)
Description	Initialize the clock.
Arguments	None
Return Value	None
Remarks	The sample code selects processing which uses PLL as the system clock without using the sub-clock. Refer to the application note RX63N Group, RX631 Group: Initial Setting, Rev. 1.00, for details of this function.

peripheral_init	
Outline	Peripheral function initialization
Header	None
Declaration	void peripheral_init(void)
Description	Initialize the peripheral functions used by the sample code.
Arguments	None
Return Value	None

mtu_init	
Outline	MTU initialization
Header	None
Declaration	void mtu_init(void)
Description	Initialize the MTU (MTU3 and MTU4).
Arguments	None
Return Value	None

pwm_pin_change	
Outline	PWM output pin switching
Header	None
Declaration	void pwm_pin_change(void)
Description	Switch alternately between PWM output pin group 0 and group 1.
Arguments	None
Return Value	None

pwm_pin_group_0	
Outline	PWM output pin group 0 settings
Header	None
Declaration	void pwm_pin_group_0(void)
Description	Change the PWM output pins from group 1 to group 0.
Arguments	None
Return Value	None

pwm_pin_group_1	
Outline	PWM output pin group 1 settings
Header	None
Declaration	void pwm_pin_group_1(void)
Description	Change the PWM output pins from group 0 to group 1.
Arguments	None
Return Value	None

sw_input_check	
Outline	Switch input determination
Header	None
Declaration	void sw_input_check(void)
Description	Determine the switch input level. Compare the current level to the previous level, and determine the input level when the levels match three times consecutively. When the determination level is changed from high to low, set the switch input determination flag to 1.
Arguments	None
Return Value	None

Excep_MTU3_TGIA3	
Outline	MTU3.TGIA3 interrupt handler
Header	None
Declaration	void Excep_MTU3_TGIA3(void)
Description	Change the duty of the PWM output, and update the switch read cycle counter for measuring 5 ms intervals.
Arguments	None
Return Value	None

5.8 Flowcharts

5.8.1 Main Processing

Figure 5.2 is a flowchart of the main processing routine.

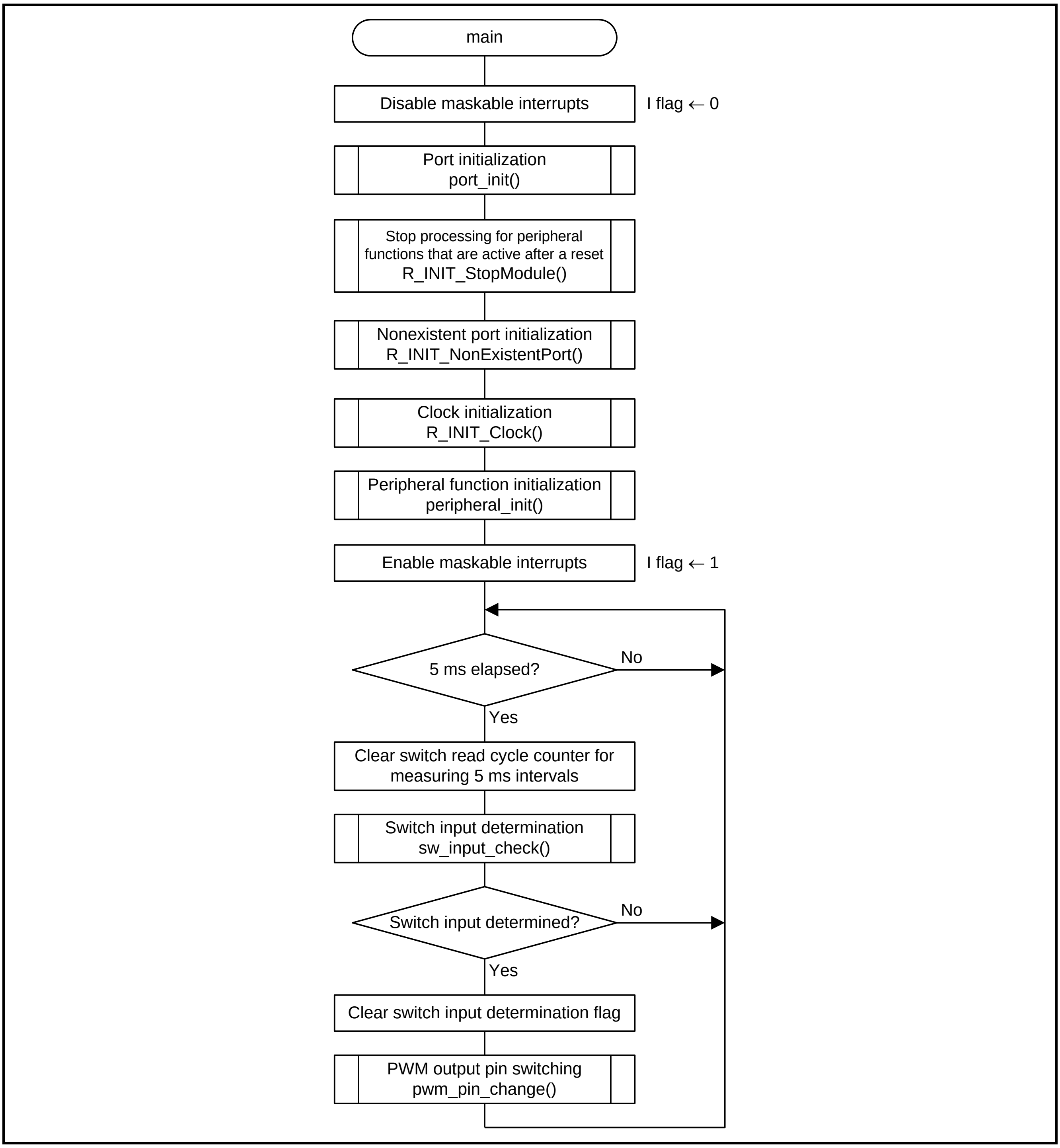

Figure 5.2 Main Processing

5.8.2 Port Initialization

Figure 5.3 is a flowchart of the port initialization routine.

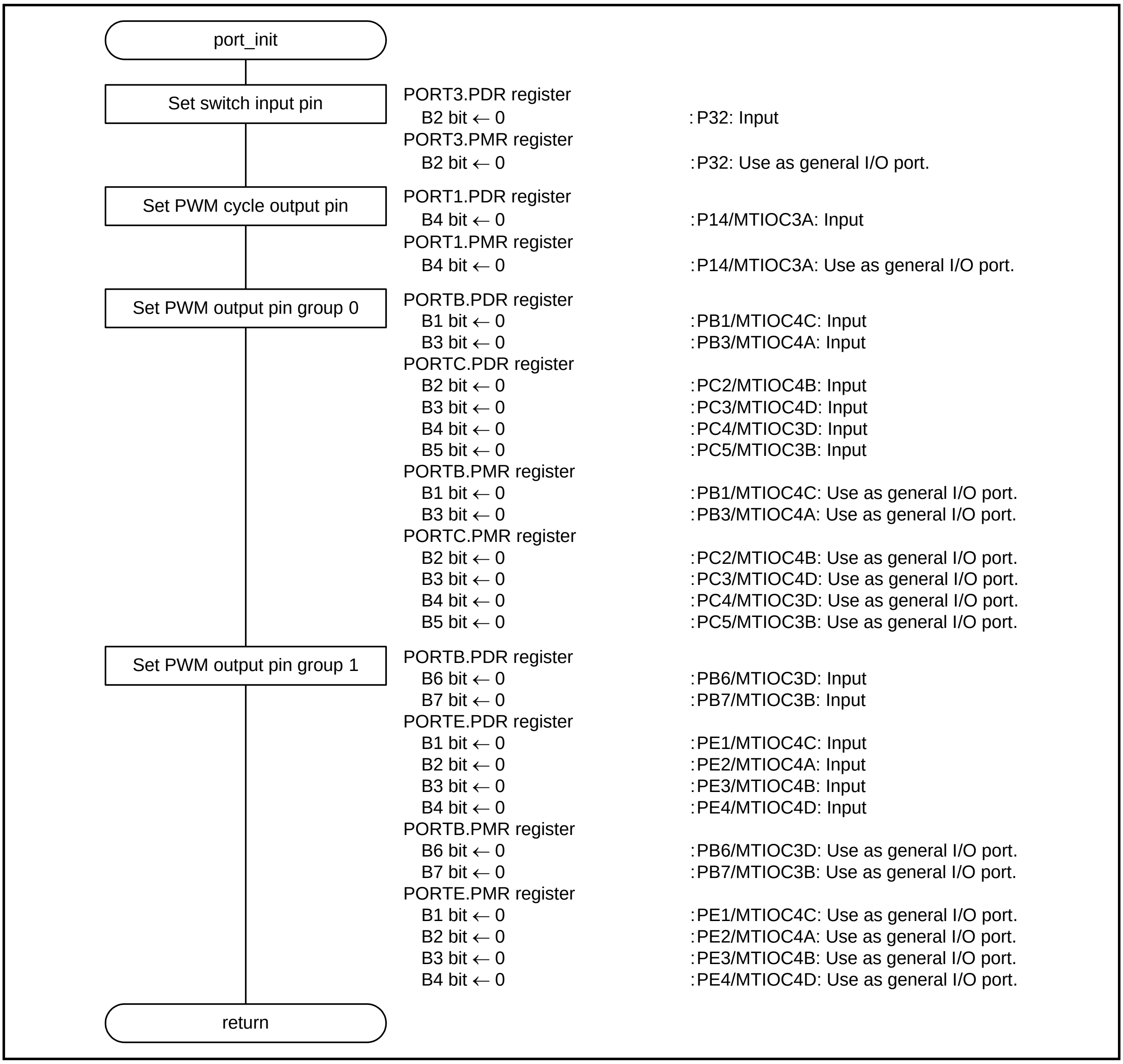

Figure 5.3 Port Initialization

5.8.3 Peripheral Function Initialization

Figure 5.4 is a flowchart of the peripheral function initialization routine.

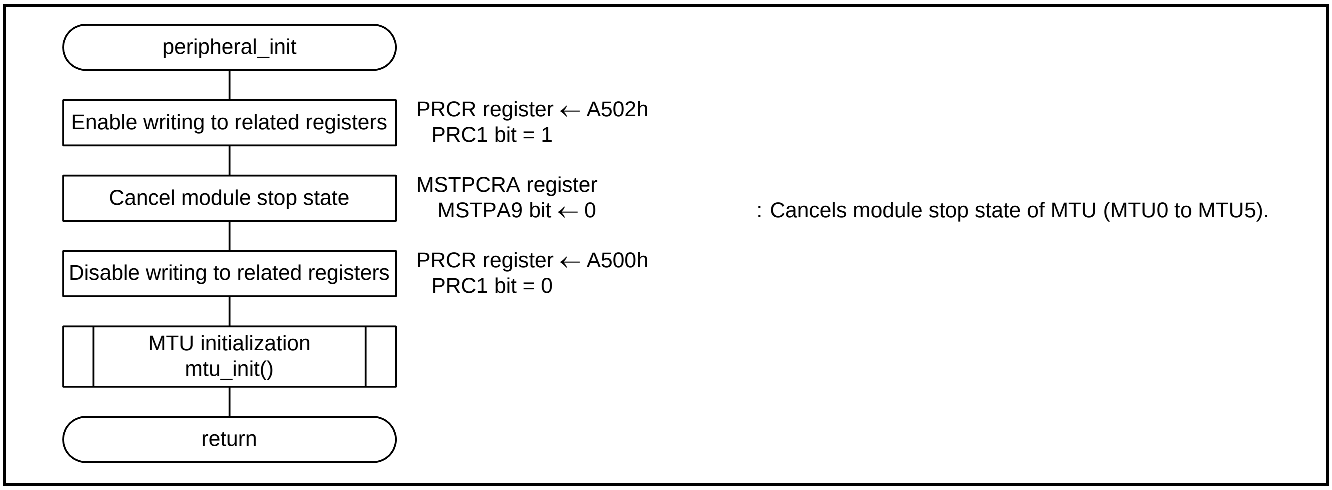

Figure 5.4 Peripheral Function Initialization

5.8.4 MTU Initialization

Figures 5.5 and 5.6 are a flowchart of the MTU initialization routine.

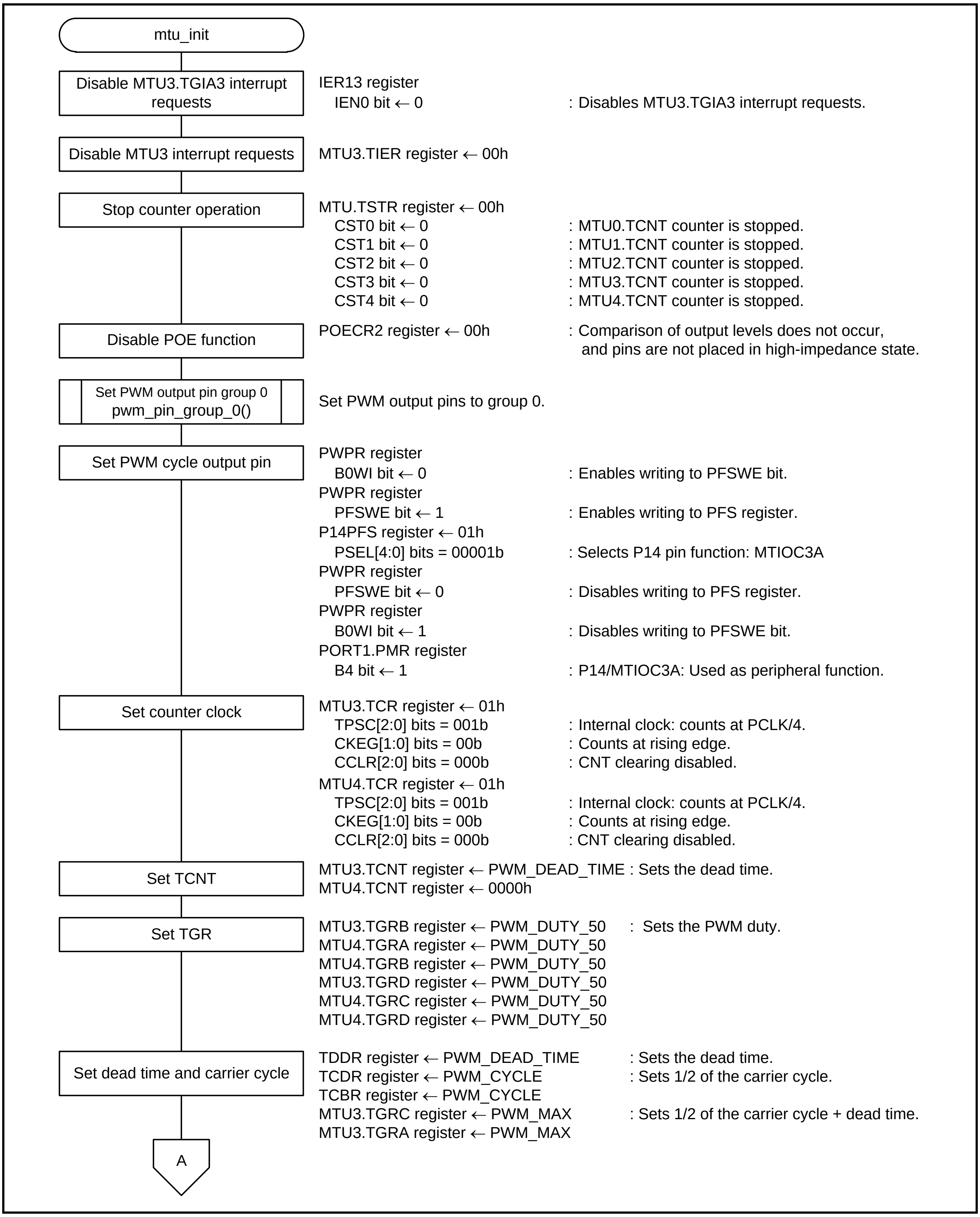

Figure 5.5 MTU Initialization (1/2)

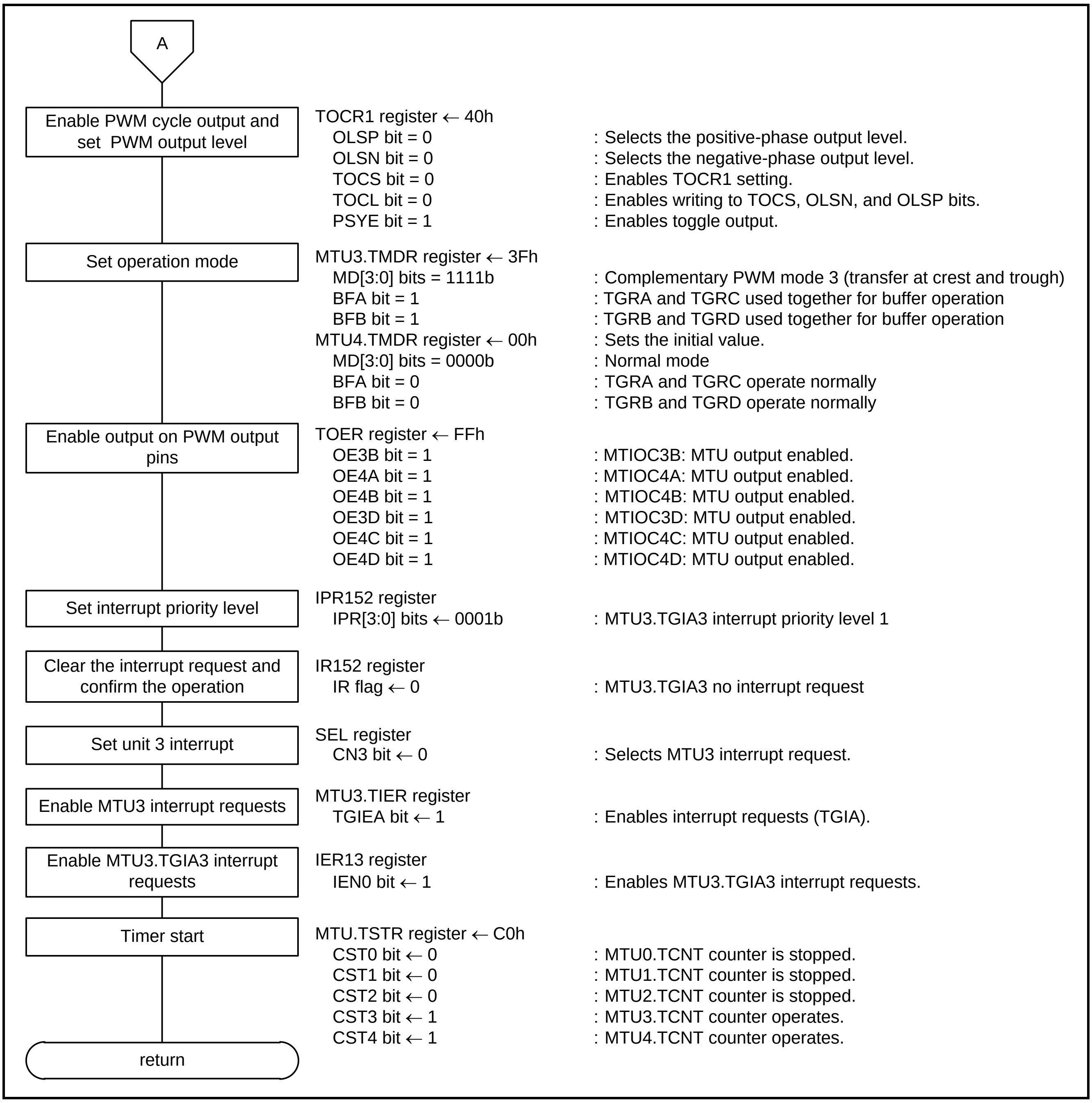

Figure 5.6 MTU Initialization (2/2)

5.8.5 PWM Output Pin Switching

Figure 5.7 is a flowchart of the PWM output pin switching routine.

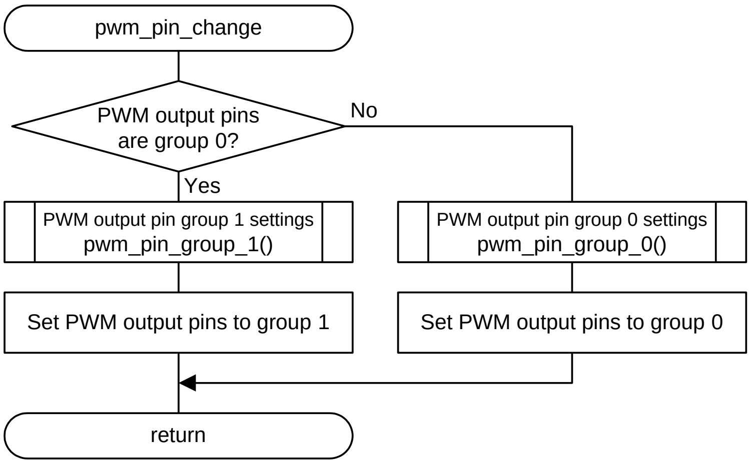

Figure 5.7 PWM Output Pin Switching

5.8.6 PWM Output Pin Group 0 Settings

Figure 5.8 is a flowchart of the PWM output pin group 0 settings routine.

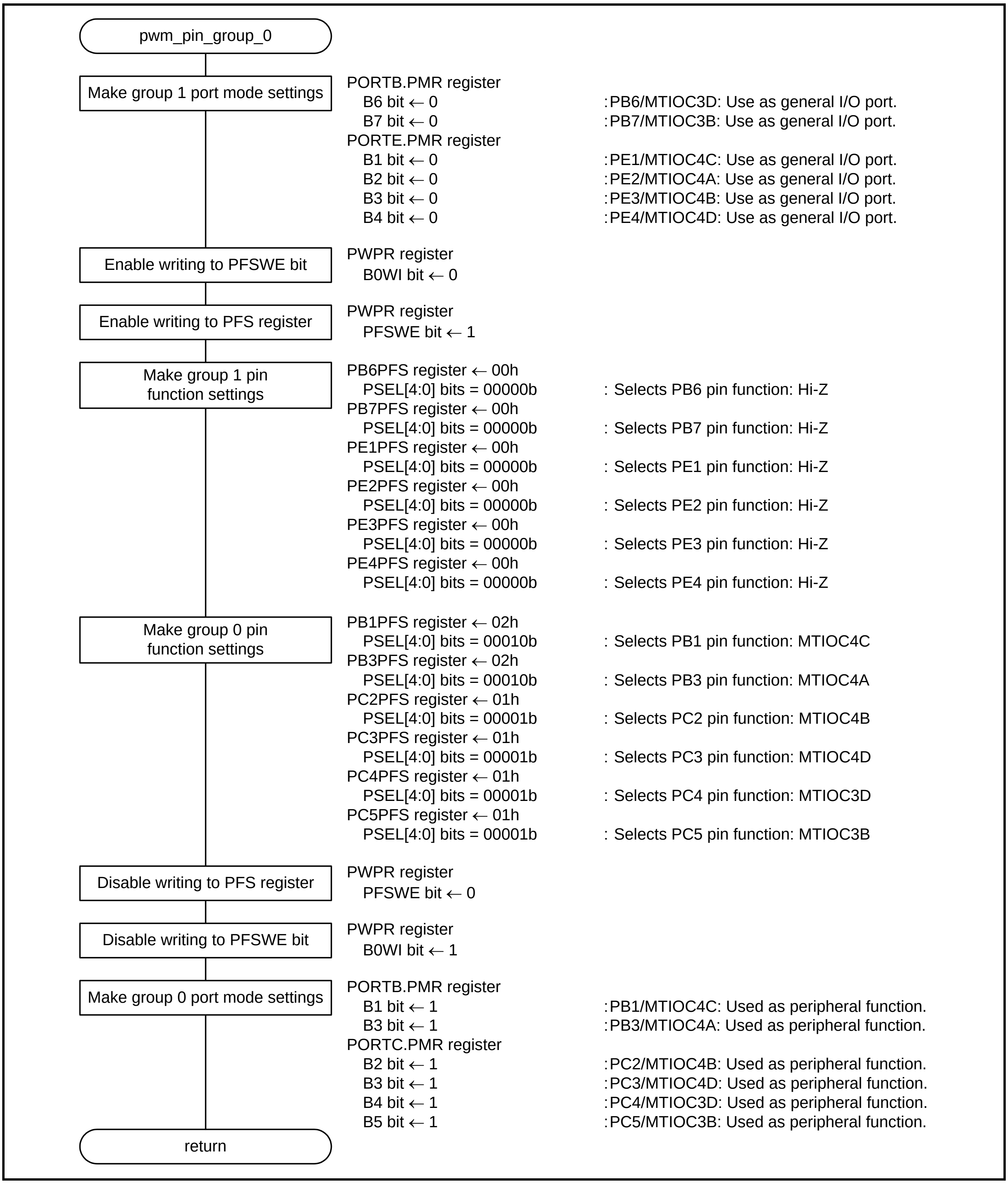

Figure 5.8 PWM Output Pin Group 0 Settings

5.8.7 PWM Output Pin Group 1 Settings

Figure 5.9 is a flowchart of the PWM output pin group 1 settings routine.

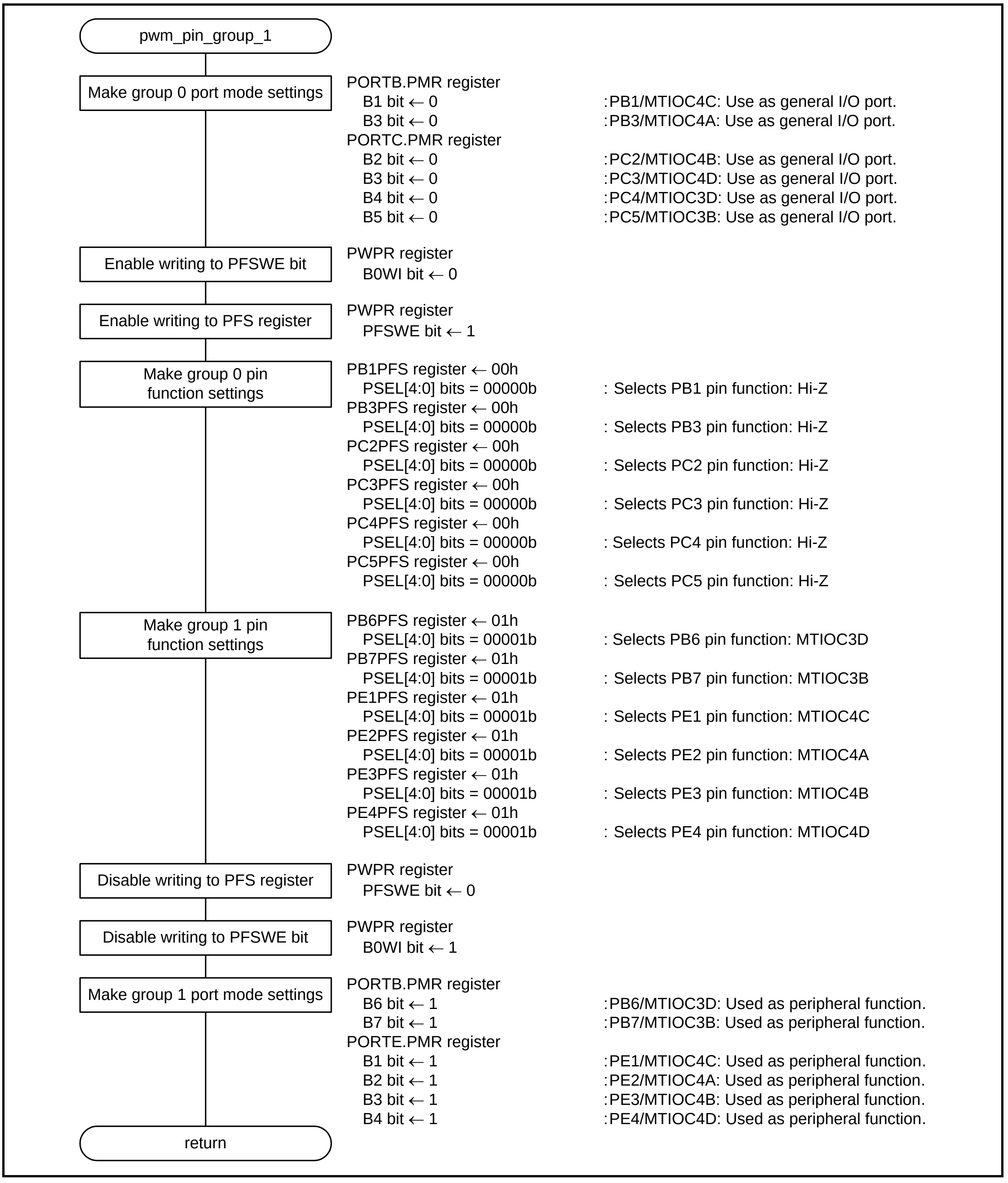

Figure 5.9 PWM Output Pin Group 1 Settings

5.8.8 Switch Input Determination

Figure 5.10 is a flowchart of the switch input determination routine.

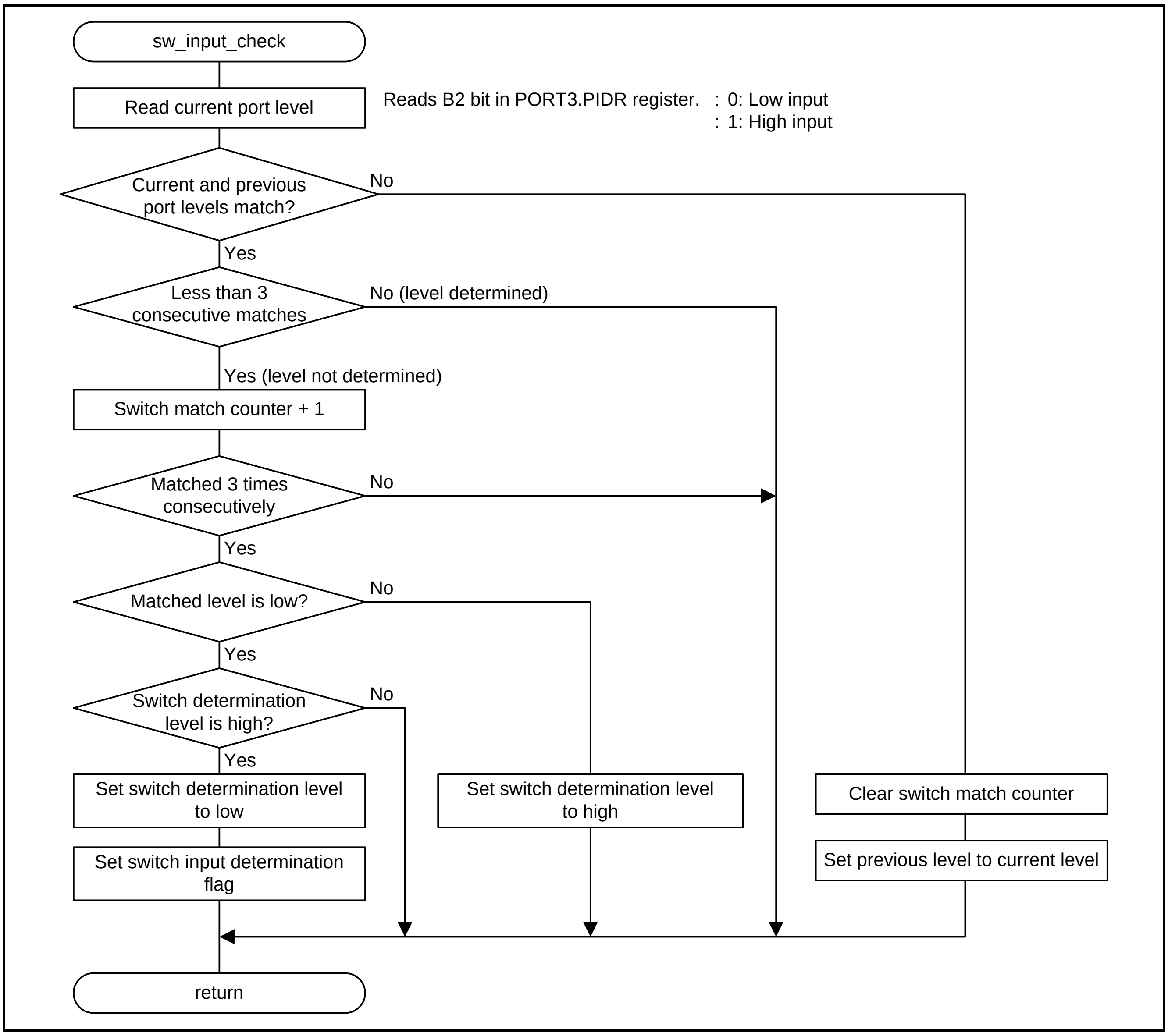

Figure 5.10 Switch Input Determination

5.8.9 MTU3.TGIA3 Interrupt Handler

Figure 5.11 is a flowchart of the MTU3.TGIA3 interrupt handler.

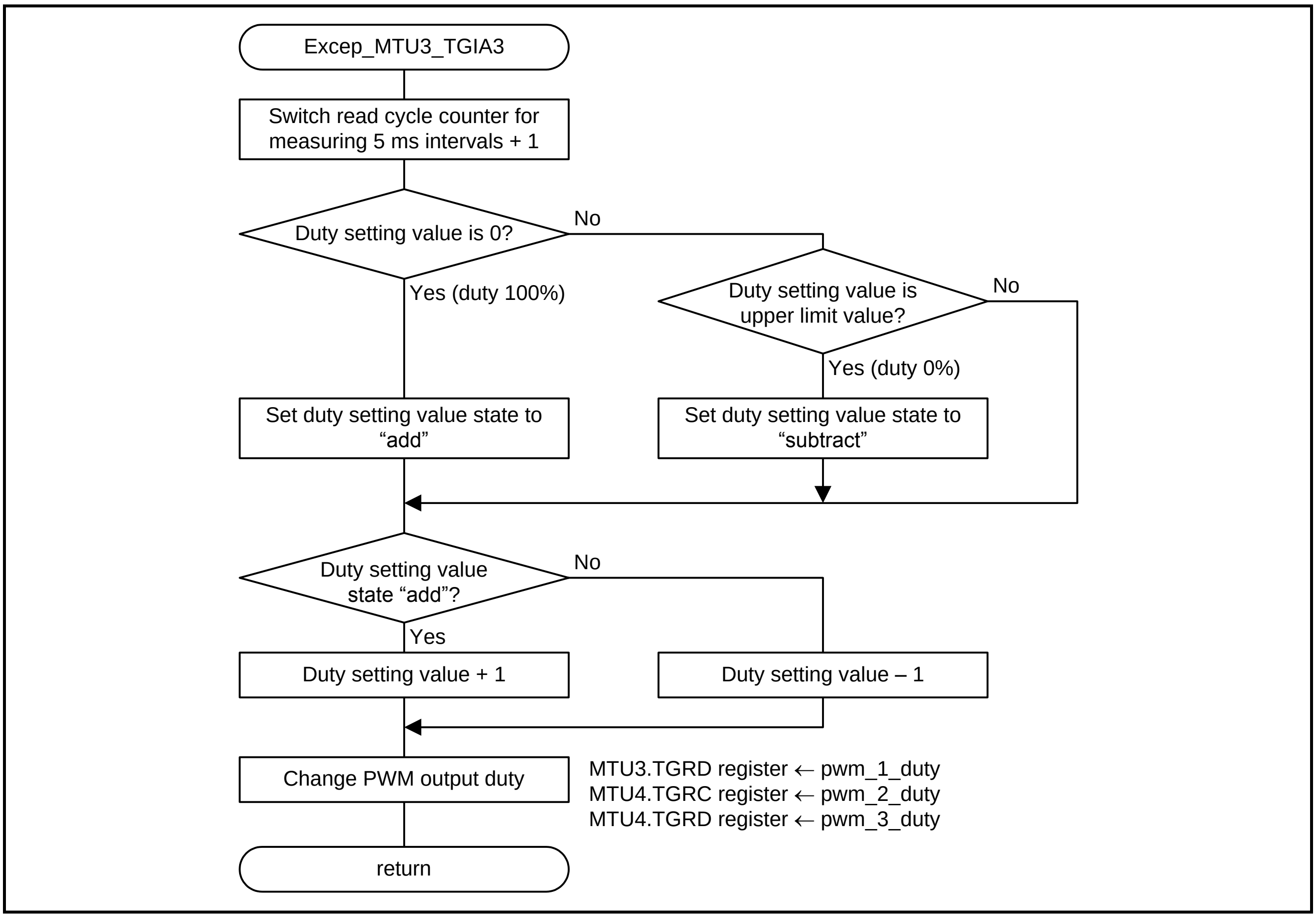

Figure 5.11 MTU3.TGIA3 Interrupt Handler

6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

User's Manual: Hardware

RX63N Group, RX631 Group User's Manual: Hardware Rev.1.80 (R01UH0041EJ)
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

User's Manual: Development Tools

RX Family C/C++ Compiler Package V.1.01 User's Manual Rev.1.00 (R20UT0570EJ)
The latest version can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website

http://www.renesas.com

Inquiries

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REVISION HISTORY	RX63N Group, RX631 Group Application Note Application Example of Exclusive Operation of Two Motors by One Set of Complementary PWM Outputs

Rev.	Date	Description	
		Page	**Summary**
1.00	**Apr. 05, 2013**	**—**	First edition issued
1.01	**Nov. 06, 2015**	**17**	Figure 5.5 is corrected.
		18	Figure 5.6 is corrected.
		Program	A setting method of a TSTR register was corrected.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   ¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

RENESAS

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