RX63N Group and RX631 Group

Differences by Pin Count in MPC Pin Functions

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Abstract

The RX63N Group and RX631 Group are offered in a variety of packages with different pin counts. This application note provides reference information on the variations in pin functions selectable by the multifunction pin controller (MPC) for different pin counts.

Products

RX63N Group and RX631 Group

Contents

1. Points to Consider Regarding Variations in Pin Functions According to RX63N Group and RX631 Group Package (Pin Count)

The pin functions selectable by the MPC differ according to the pin counts of the various RX63N Group and RX631 Group packages. This must be considered when switching microcontroller products within the RX63N Group and RX631 Group. For details, see section 4., Differences, and RX63N Group and RX631 Group User's Manual: Hardware.

2. Differences

2.1 Function Differences by Pin Count

Table 2.1.1 lists function differences by pin count.

Table 2.1.1 Function Differences by Pin Count (1/2)

O: Selectable —: Pin function eliminated (setting prohibited) (Blank): Pin eliminated

		Pin Function	MPC Setting	Pin Count				
				177/176-Pin	145/144-Pin	100-Pin	64-Pin	48-Pin
Port 1	P12	MTIC5U	00001b	O	—	—		
	P15	SCK3	01011b	O	O	O	—	—
		USB1_ DPUPE	10001b	O	—	—	—	—
	P16	RXD3 SMISO3 SSCL3	01011b	O	O	O	—	—
	P17	ADTRG#	01001b	O	O	O	—	—
		TXD3 SMOSI3 SSDA3	01011b	O	O	O	—	—
		USB1_ VBUS	10001b	O	—	—	—	—
Port 2	P20	SDA1	01111b	O	O	—		
	P21	SCL1	01111b	O	O	—		
	P26	CTS3# RTS3# SS3#	01011b	O	O	O	—	—
		USB0_VBUSEN	10011b	—	—	—	O	O
Port 5	P54	CTS2# RTS2# SS2#	01011b	O	O	O	—	
		ET_LINKSTA	10001b	O	O	O	—	
		EDACK0	11000b	O	O	O	—	
	P55	ET_EXOUT	10001b	O	O	O	—	
		EDREQ0	11000b	O	O	O	—	
Port A	PA0	ET_TX_EN	10001b	O	O	O	—	
		RMII_TXD_EN	10010b	O	O	O	—	
	PA1	ET_WOL	10001b	O	O	O	—	—
	PA3	ET_MDIO	10001b	O	O	O	—	—
	PA4	ET_MDC	10001b	O	O	O	—	—
	PA6	ET_EXOUT	10001b	O	O	O	—	—
Port B	PB0	RXD4 SMISO4 SSCL4	01010b	O	O	—	—	—
		ET_ERXD1	10001b	O	O	O	—	—
		RMII_RXD1	10010b	O	O	O	—	—
	PB1	TXD4 SMOSI4 SSDA4	01010b	O	O	—	—	—
		ET_ERXD0	10001b	O	O	O	—	—
		RMII_RXD0	10010b	O	O	O	—	—
	PB2	CTS4# RTS4# SS4#	01010b	O	O	—		
	PB3	SCK4	01010b	O	O	—	—	—
		ET_RX_ER	10001b	O	O	O	—	—
		RMII_RX_ER	10010b	O	O	O	—	—
	PB5	ET_ETXD0	10001b	O	O	O	—	—
		RMII_TXD0	10010b	O	O	O	—	—
	PB6	ET_ETXD1	10001b	O	O	O	—	
		RMII_TXD1	10010b	O	O	O	—	
	PB7	ET_CRS	10001b	O	O	O	—	
		RMII_CRS_DV	10010b	O	O	O	—	

Table 2.1.2 Function Differences by Pin Count (2/2)

O: Selectable —: Pin function eliminated (setting prohibited) (Blank): Pin eliminated

		Pin Function	MPC Setting	Pin Count				
				177/176-Pin	145/144-Pin	100-Pin	64-Pin	48-Pin
Port C	PC0	SCL3	01111b	O	O	—		
	PC1	SDA3	01111b	O	O	—		
	PC2	ET_RX_DV	10001b	O	O	O	—	
	PC3	ET_TX_ER	10001b	O	O	O	—	
	PC4	TIOCC6	00011b	O	O	—	—	—
		TCLKE	00100b	O	O	—	—	—
		ET_TX_CLK	10001b	O	O	O	—	—
		USB0_DPRPD	10011b	—	—	—	O	O
	PC5	TIOCD6	00011b	O	O	—	—	—
		TCLKF	00100b	O	O	—	—	—
		ET_ETXD2	10001b	O	O	O	—	—
		USB0_ID	10011b	—	—	—	O	O
	PC6	TIOCA6	00011b	O	O	—	—	—
		ET_ETXD3	10001b	O	O	O	—	—
		USB0_EXICEN	10011b	—	—	—	O	O
	PC7	TIOCB6	00011b	O	O	—	—	—
		ET_COL	10001b	O	O	O	—	—
Port D	PD0	TIOCA7	00011b	O	O	—		
	PD1	TIOCB7	00011b	O	O	—		
		TCLKG	00100b	O	O	—		
		MOSIC	01101b	O	O	—		
	PD2	TIOCA8	00011b	O	O	—		
		MISOC	01101b	O	O	—		
	PD3	TIOCB8	00011b	O	O	—		
		TCLKH	00100b	O	O	—		
		RSPCKC	01101b	O	O	—		
	PD4	SSLC0	01101b	O	O	—		
	PD5	SSLC1	01101b	O	O	—		
	PD6	SSLC2	01101b	O	O	—		
	PD7	SSLC3	01101b	O	O	—		
Port E	PE0	TIOCC9	00011b	O	O	—	—	
	PE1	TIOCD9	00011b	O	O	—	—	—
	PE2	TIOCA9	00011b	O	O	—	—	—
	PE3	TIOCB9	00011b	O	O	—	—	—
		ET_ERXD3	10001b	O	O	O	—	—
	PE4	TIOCA10	00011b	O	O	—	—	—
		ET_ERXD2	10001b	O	O	O	—	—
	PE5	TIOCB10	00011b	O	O	—	—	
		ET_RX_CLK	10001b	O	O	O	—	
		REF50CK	10010b	O	O	O	—	
	PE6	TIOCA11	00011b	O	O	—		
	PE7	TIOCB11	00011b	O	O	—		

2.2 Difference in Pin Functions of Ports by Pin Count

Tables 2.2.1 to 2.2.16 list the differences in the pin functions selectable by the MPC for each port according to the pin count.

Table 2.2.1 Port 0

—: Setting prohibited —: Pin function eliminated (setting prohibited) : Pin eliminated

Port	Pin Count	Setting Value of Bits PSEL4 to PSEL0																				
		00000b	00001b	00010b	00011b	00100b	00101b	00110b	00111b	01000b	01001b	01010b	01011b	01100b	01101b	01110b	01111b	10000b	10001b	10010b	10011b	11000b
P00	177/176-Pin	Hi-Z	—	—	—	—	TMRI0	—	—	—	—	TXD6 SMOSI6 SSDA6	—	—	—	—	—	—	—	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P01	177/176-Pin	Hi-Z	—	—	—	—	TMCI0	—	—	—	—	RXD6 SMISO6 SSCL6	—	—	—	—	—	—	—	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P02	177/176-Pin	Hi-Z	—	—	—	—	TMCI1	—	—	—	—	SCK6	—	—	—	—	—	—	—	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P03	177/176-Pin	—																				
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P04	177/176-Pin																					
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P05	177/176-Pin	—																				
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P06	177/176-Pin																					
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P07	177/176-Pin	Hi-Z	—	—	—	—	—	—	—	—	ADTRG0#	—	—	—	—	—	—	—	—	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					

Table 2.2.2 Port 1

—: Setting prohibited — : Pin function eliminated (setting prohibited) : Pin eliminated

Port	Pin Count	Setting Value of Bits PSEL4 to PSEL0																					
		00000b	00001b	00010b	00011b	00100b	00101b	00110b	00111b	01000b	01001b	01010b	01011b	01100b	01101b	01110b	01111b	10000b	10001b	10010b	10011b	11000b
P10	177/176-Pin	Hi-Z	MTIC5W	—	—	—	TMRI3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	145/144-Pin																						
	100-Pin																						
	64-Pin																						
	48-Pin																						
P11	177/176-Pin	Hi-Z	MTIC5V	—	—	—	TMCI3	—	—	—	—	SCK2	—	—	—	—	—	—	—	—	—	—	—
	145/144-Pin																						
	100-Pin																						
	64-Pin																						
	48-Pin																						
P12	177/176-Pin	Hi-Z	MTIC5U	—	—	—	TMCI1	—	—	—	—	RXD2 SMISO2 SSCL2	—	—	—	—	SCL0 [FM+]	—	—	—	—	—
	145/144-Pin		—																				
	100-Pin																						
	64-Pin																						
	48-Pin																						
P13	177/176-Pin	Hi-Z	MTIOC0B	—	TIOCA5	—	TMO3	PO13	—	—	ADTRG#	TXD2 SMOSI2 SSDA2	—	—	—	—	SDA0 [FM+]	—	—	—	—	—
	145/144-Pin																						
	100-Pin																						
	64-Pin																						
	48-Pin																						
P14	177/176-Pin	Hi-Z	MTIOC3A	MTCLKA	TIOCB5	TCLKA	TMRI2	PO15	—	—	—	—	CTS1# RTS1# SS1#	—	—	—	—	CTX1	USB0_ DPUPE	USB0_ OVRCURA	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P15	177/176-Pin	Hi-Z	MTIOC0B	MTCLKB	TIOCB2	TCLKB	TMCI2	PO13	—	—	—	RXD1 SMISO1 SSCL1	SCK3	—	—	—	—	CRX1-DS	USB1_ DPUPE	—	—	—
	145/144-Pin												—						—			
	100-Pin																					
	64-Pin																					
	48-Pin																					
P16	177/176-Pin	Hi-Z	MTIOC3C	MTIOC3D	TIOCB1	TCLKC	TMO2	PO14	RTCOUT	—	ADTRG0#	TXD1 SMOSI1 SSDA1	RXD3 SMISO3 SSCL3	—	MOSIA	—	SCL2-DS	IERXD	USB0_ VBUS	USB0_ VBUSEN	USB0_ OVRCURB	—
	145/144-Pin												—									
	100-Pin																					
	64-Pin																					
	48-Pin																					
P17	177/176-Pin	Hi-Z	MTIOC3A	MTIOC3B	TIOCB0	TCLKD	TMO1	PO15	POE8#	—	ADTRG#	SCK1	TXD3 SMOSI3 SSDA3	—	MISOA	—	SDA2-DS	IETXD	USB1_ VBUS	—	—	—
	145/144-Pin																		—			
	100-Pin																					
	64-Pin										—		—									
	48-Pin																					

Table 2.2.3 Port 2

—: Setting prohibited —: Pin function eliminated (setting prohibited) : Pin eliminated

Port	Pin Count	Setting Value of Bits PSEL4 to PSEL0																				
		00000b	00001b	00010b	00011b	00100b	00101b	00110b	00111b	01000b	01001b	01010b	01011b	01100b	01101b	01110b	01111b	10000b	10001b	10010b	10011b	11000b
P20	177/176-Pin	Hi-Z	MTIOC1A	—	TIOCB3	—	TMRI0	PO0	—	—	—	TXD0 SMOSI0 SSDA0	—	—	—	—	SDA1	—	—	—	USB0_ID	—
	145/144-Pin																					
	100-Pin																—					
	64-Pin																					
	48-Pin																					
P21	177/176-Pin	Hi-Z	MTIOC1B	—	TIOCA3	—	TMCI0	PO1	—	—	—	RXD0 SMISO0 SSCL0	—	—	—	—	SCL1	—	—	—	USB0_ EXICEN	—
	145/144-Pin																					
	100-Pin																—					
	64-Pin																					
	48-Pin																					
P22	177/176-Pin	Hi-Z	MTIOC3B	MTCLKC	TIOCC3	—	TMO0	PO2	—	—	—	SCK0	—	—	—	—	—	—	—	—	USB0_ DRPD	EDREQ0
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P23	177/176-Pin	Hi-Z	MTIOC3D	MTCLKD	TIOCD3	—	—	PO3	—	—	—	TXD3 SMOSI3 SSDA3	CTS0# RTS0# SS0#	—	—	—	—	—	—	—	USB0_ DPUPE	EDACK0
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P24	177/176-Pin	Hi-Z	MTIOC4A	MTCLKA	TIOCB4	—	TMRI1	PO4	—	—	—	SCK3	—	—	—	—	—	—	—	—	USB0_ VBUSEN	EDREQ1
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P25	177/176-Pin	Hi-Z	MTIOC4C	MTCLKB	TIOCA4	—	—	PO5	—	—	ADTRG0#	RXD3 SMISO3 SSCL3	—	—	—	—	—	—	—	—	USB0_ DPRPD	EDACK1
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P26	177/176-Pin	Hi-Z	MTIOC2A	—	—	—	TMO1	PO6	—	—	—	TXD1 SMOSI1 SSDA1	CTS3# RTS3# SS3#	—	MOSIB	—	—	—	—	—	—	—
	145/144-Pin																					
	100-Pin																				—	
	64-Pin												—								USB0_ VBUSEN	
	48-Pin																					
P27	177/176-Pin	Hi-Z	MTIOC2B	—	—	—	TMCI3	PO7	—	—	—	SCK1	—	—	RSPCKB	—	—	—	—	—	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					

Table 2.2.4 Port 3

—: Setting prohibited —: Pin function eliminated (setting prohibited) : Pin eliminated

Port	Pin Count	Setting Value of Bits PSEL4 to PSEL0																				
		00000b	00001b	00010b	00011b	00100b	00101b	00110b	00111b	01000b	01001b	01010b	01011b	01100b	01101b	01110b	01111b	10000b	10001b	10010b	10011b	11000b
P30	177/176-Pin	Hi-Z	MTIOC4B	—	—	—	TMRI3	PO8	POE8#	—	—	RXD1 SMISO1 SSCL1	—	—	MISOB	—	—	—	—	—	USB0_ DRPD	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P31	177/176-Pin	Hi-Z	MTIOC4D	—	—	—	TMCI2	PO9	—	—	—	—	CTS1# RTS1# SS1#	—	SSLB0	—	—	—	—	—	USB0_ DPUPE	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P32	177/176-Pin	Hi-Z	MTIOC0C	—	TIOCC0	—	TMO3	PO10	RTCOUT	—	—	TXD6 SMOSI6 SSDA6	TXD0 SMOSI0 SSDA0	—	—	—	—	CTX0	—	—	USB0_ VBUSEN	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P33	177/176-Pin	Hi-Z	MTIOC0D	—	TIOCD0	—	TMRI3	PO11	POE3#	—	—	RXD6 SMISO6 SSCL6	RXD0 SMISO0 SSCL0	—	—	—	—	CRX0	—	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P34	177/176-Pin	Hi-Z	MTIOC0A	—	—	—	TMCI3	PO12	POE2#	—	—	SCK6	SCK0	—	—	—	—	—	—	—	USB0_ DPRPD	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P35	177/176-Pin	—																				
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P36	177/176-Pin	—																				
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P37	177/176-Pin	—																				
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					

Table 2.2.5 Port 5

—: Setting prohibited —: Pin function eliminated (setting prohibited) : Pin eliminated

Port	Pin Count	Setting Value of Bits PSEL4 to PSEL0																				
		00000b	00001b	00010b	00011b	00100b	00101b	00110b	00111b	01000b	01001b	01010b	01011b	01100b	01101b	01110b	01111b	10000b	10001b	10010b	10011b	11000b
P50	177/176-Pin	Hi-Z	—	—	—	—	—	—	—	—	—	TXD2 SMOSI2 SSDA2	—	—	SSLB1	—	—	—	—	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P51	177/176-Pin	Hi-Z	—	—	—	—	—	—	—	—	—	SCK2	—	—	SSLB2	—	—	—	—	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P52	177/176-Pin	Hi-Z	—	—	—	—	—	—	—	—	—	RXD2 SMISO2 SSCL2	—	—	SSLB3	—	—	—	—	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P53	177/176-Pin	—																				
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P54	177/176-Pin	Hi-Z	MTIOC4B	—	—	—	TMCI1	—	—	—	—	—	CTS2# RTS2# SS2#	—	—	—	—	CTX1	ET _LINKSTA	—	—	EDACK0
	145/144-Pin																					
	100-Pin																					
	64-Pin												—						—			—
	48-Pin																					
P55	177/176-Pin	Hi-Z	MTIOC4D	—	—	—	TMO3	—	—	—	—	—	—	—	—	—	—	CRX1	ET _EXOUT	—	—	EDREQ0
	145/144-Pin																					
	100-Pin																					
	64-Pin																		—			—
	48-Pin																					
P56	177/176-Pin	Hi-Z	MTIOC3C	—	TIOCA1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EDACK1
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P57	177/176-Pin	Hi-Z	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EDREQ1
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					

Table 2.2.6 Port 6

—: Setting prohibited —: Pin function eliminated (setting prohibited) : Pin eliminated

Port	Pin Count	Setting Value of Bits PSEL4 to PSEL0																				
		00000b	00001b	00010b	00011b	00100b	00101b	00110b	00111b	01000b	01001b	01010b	01011b	01100b	01101b	01110b	01111b	10000b	10001b	10010b	10011b	11000b
P60	177/176-Pin	—																				
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P61	177/176-Pin	—																				
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P62	177/176-Pin	—																				
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P63	177/176-Pin	—																				
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P64	177/176-Pin	—																				
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P65	177/176-Pin	—																				
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P66	177/176-Pin	Hi-Z	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CTX2*1	—	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P67	177/176-Pin	Hi-Z	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CRX2*1	—	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					

Note: 1. No products have a ROM capacity of 1MB or less.

Table 2.2.7 Port 7

—: Setting prohibited —: Pin function eliminated (setting prohibited) : Pin eliminated

Port	Pin Count	Setting Value of Bits PSEL4 to PSEL0																				
		00000b	00001b	00010b	00011b	00100b	00101b	00110b	00111b	01000b	01001b	01010b	01011b	01100b	01101b	01110b	01111b	10000b	10001b	10010b	10011b	11000b
P70	177/176-Pin	—																				
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P71	177/176-Pin	Hi-Z	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ET_MDIO	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P72	177/176-Pin	Hi-Z	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ET_MDC	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P73	177/176-Pin	Hi-Z	—	—	—	—	—	PO16	—	—	—	—	—	—	—	—	—	—	—	ET_WOL	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P74	177/176-Pin	Hi-Z	—	—	—	—	—	PO19	—	—	—	—	CTS11# RTS11 SS11#	—	—	—	—	—	ET _ERXD1	RMII _RXD1	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P75	177/176-Pin	Hi-Z	—	—	—	—	—	PO20	—	—	—	SCK11	—	—	—	—	—	—	ET _ERXD0	RMII _RXD0	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P76	177/176-Pin	Hi-Z	—	—	—	—	—	PO22	—	—	—	RXD11 SMISO11 SSCL11	—	—	—	—	—	—	ET_RX _CLK	REF50CK	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P77	177/176-Pin	Hi-Z	—	—	—	—	—	PO23	—	—	—	TXD11 SMOSI11 SSDA11	—	—	—	—	—	—	ET_RX _ER	RMII_RX _ER	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					

Table 2.2.8 Port 8

—: Setting prohibited —: Pin function eliminated (setting prohibited) : Pin eliminated

Port	Pin Count	Setting Value of Bits PSEL4 to PSEL0																				
		00000b	00001b	00010b	00011b	00100b	00101b	00110b	00111b	01000b	01001b	01010b	01011b	01100b	01101b	01110b	01111b	10000b	10001b	10010b	10011b	11000b
P80	177/176-Pin	Hi-Z	MTIOC3B	—	—	—	—	PO26	—	—	—	SCK10	—	—	—	—	—	—	ET_TX_EN	RMII_TXD_EN	—	EDREQ0
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P81	177/176-Pin	Hi-Z	MTIOC3D	—	—	—	—	PO27	—	—	—	RXD10 SMISO10 SSCL10	—	—	—	—	—	—	ET_ETXD0	RMII_TXD0	—	EDACK0
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P82	177/176-Pin	Hi-Z	MTIOC4A	—	—	—	—	PO28	—	—	—	TXD10 SMOSI10 SSDA10	—	—	—	—	—	—	ET_ETXD1	RMII_TXD1	—	EDREQ1
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P83	177/176-Pin	Hi-Z	MTIOC4C	—	—	—	—	—	—	—	—	—	CTS10# RTS10# SS10#	—	—	—	—	—	ET_CRS	RMII_CRS_DV	—	EDACK1
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P84	177/176-Pin	—																				
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P85	177/176-Pin	—																				
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P86	177/176-Pin	Hi-Z	—	—	TIOCA0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P87	177/176-Pin	Hi-Z	—	—	TIOCA2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					

Table 2.2.9 Port 9

—: Setting prohibited —: Pin function eliminated (setting prohibited) : Pin eliminated

Port	Pin Count	Setting Value of Bits PSEL4 to PSEL0																				
		00000b	00001b	00010b	00011b	00100b	00101b	00110b	00111b	01000b	01001b	01010b	01011b	01100b	01101b	01110b	01111b	10000b	10001b	10010b	10011b	11000b
P90	177/176-Pin	Hi-Z	—	—	—	—	—	—	—	—	—	TXD7 SMOSI7 SSDA7	—	—	—	—	—	—	—	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P91	177/176-Pin	Hi-Z	—	—	—	—	—	—	—	—	—	SCK7	—	—	—	—	—	—	—	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P92	177/176-Pin	Hi-Z	—	—	—	—	—	—	—	—	—	RXD7 SMISO7 SSCL7	—	—	—	—	—	—	—	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P93	177/176-Pin	Hi-Z	—	—	—	—	—	—	—	—	—	—	CTS7# RTS7# SS7#	—	—	—	—	—	—	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P94	177/176-Pin	—																				
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P95	177/176-Pin	—																				
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P96	177/176-Pin	—																				
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
P97	177/176-Pin	—																				
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					

Table 2.2.10 Port A

—: Setting prohibited —: Pin function eliminated (setting prohibited) : Pin eliminated

Port	Pin Count	Setting Value of Bits PSEL4 to PSEL0																				
		00000b	00001b	00010b	00011b	00100b	00101b	00110b	00111b	01000b	01001b	01010b	01011b	01100b	01101b	01110b	01111b	10000b	10001b	10010b	10011b	11000b
PA0	177/176-Pin	Hi-Z	MTIOC4A	—	TIOCA0	—	—	PO16	—	—	—	—	—	—	SSLA1	—	—	—	ET_TX_EN	RMII_TXD_EN	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																		—	—		
	48-Pin																					
PA1	177/176-Pin	Hi-Z	MTIOC0B	MTCLKC	TIOCB0	—	—	PO17	—	—	—	SCK5	—	—	SSLA2	—	—	—	ET_WOL	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																		—			
	48-Pin																					
PA2	177/176-Pin	Hi-Z	—	—	—	—	—	PO18	—	—	—	RXD5 SMISO5 SSCL5	—	—	SSLA3	—	—	—	—	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
PA3	177/176-Pin	Hi-Z	MTIOC0D	MTCLKD	TIOCD0	TCLKB	—	PO19	—	—	—	RXD5 SMISO5 SSCL5	—	—	—	—	—	—	ET_MDIO	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																		—			
	48-Pin																					
PA4	177/176-Pin	Hi-Z	MTIC5U	MTCLKA	TIOCA1	—	TMRI0	PO20	—	—	—	TXD5 SMOSI5 SSDA5	—	—	SSLA0	—	—	—	ET_MDC	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																		—			
	48-Pin																					
PA5	177/176-Pin	Hi-Z	—	—	TIOCB1	—	—	PO21	—	—	—	—	—	—	RSPCKA	—	—	—	ET_LINKSTA	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
PA6	177/176-Pin	Hi-Z	MTIC5V	MTCLKB	TIOCA2	—	TMCI3	PO22	POE2#	—	—	—	CTS5# RTS5# SS5#	—	MOSIA	—	—	—	ET_EXOUT	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																		—			
	48-Pin																					
PA7	177/176-Pin	Hi-Z	—	—	TIOCB2	—	—	PO23	—	—	—	—	—	—	MISOA	—	—	—	ET_WOL	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					

Table 2.2.11 Port B

—: Setting prohibited — : Pin function eliminated (setting prohibited) : Pin eliminated

Port	Pin Count	Setting Value of Bits PSEL4 to PSEL0																				
		00000b	00001b	00010b	00011b	00100b	00101b	00110b	00111b	01000b	01001b	01010b	01011b	01100b	01101b	01110b	01111b	10000b	10001b	10010b	10011b	11000b
PB0	177/176-Pin	Hi-Z	MTIC5W	—	TIOCA3	—	—	PO24	—	—	—	RXD4 SMISO4 SSCL4	RXD6 SMISO6 SSCL6	—	RSPCKA	—	—	—	ET _ERXD1	RMII _RXD1	—	—
	145/144-Pin																					
	100-Pin											—										
	64-Pin																		—	—		
	48-Pin																					
PB1	177/176-Pin	Hi-Z	MTIOC0C	MTIOC4C	TIOCB3	—	TMCI0	PO25	—	—	—	TXD4 SMOSI4 SSDA4	TXD6 SMOSI6 SSDA6	—	—	—	—	—	ET _ERXD0	RMII _RXD0	—	—
	145/144-Pin																					
	100-Pin											—										
	64-Pin																		—	—		
	48-Pin																					
PB2	177/176-Pin	Hi-Z	—	—	TIOCC3	TCLKC	—	PO26	—	—	—	CTS4# RTS4# SS4#	CTS6# RTS6# SS6#	—	—	—	—	—	ET_RX _CLK	REF50CK	—	—
	145/144-Pin																					
	100-Pin											—										
	64-Pin																					
	48-Pin																					
PB3	177/176-Pin	Hi-Z	MTIOC0A	MTIOC4A	TIOCD3	TCLKD	TMO0	PO27	POE3#	—	—	SCK4	SCK6	—	—	—	—	—	ET_RX _ER	RMII_RX _ER	—	—
	145/144-Pin																					
	100-Pin											—										
	64-Pin																		—	—		
	48-Pin																					
PB4	177/176-Pin	Hi-Z	—	—	TIOCA4	—	—	PO28	—	—	—	—	CTS9# RTS9# SS9#	—	—	—	—	—	ET_TX _EN	RMII_TXD _EN	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
PB5	177/176-Pin	Hi-Z	MTIOC2A	MTIOC1B	TIOCB4	—	TMRI1	PO29	POE1#	—	—	SCK9	—	—	—	—	—	—	ET _ETXD0	RMII _TXD0	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																		—	—		
	48-Pin																					
PB6	177/176-Pin	Hi-Z	MTIOC3D	—	TIOCA5	—	—	PO30	—	—	—	RXD9 SMISO9 SSCL9	—	—	—	—	—	—	ET _ETXD1	RMII _TXD1	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																		—	—		
	48-Pin																					
PB7	177/176-Pin	Hi-Z	MTIOC3B	—	TIOCB5	—	—	PO31	—	—	—	TXD9 SMOSI9 SSDA9	—	—	—	—	—	—	ET_CRS	RMII_CRS _DV	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																		—	—		
	48-Pin																					

Table 2.2.12 Port C

—: Setting prohibited —: Pin function eliminated (setting prohibited) : Pin eliminated

Port	Pin Count	Setting Value of Bits PSEL4 to PSEL0																				
		00000b	00001b	00010b	00011b	00100b	00101b	00110b	00111b	01000b	01001b	01010b	01011b	01100b	01101b	01110b	01111b	10000b	10001b	10010b	10011b	11000b
PC0	177/176-Pin	Hi-Z	MTIOC3C	—	TCLKC	—	—	PO17	—	—	—	—	CTS5# RTS5# SS5#	—	SSLA1	—	SCL3	—	ET _ERXD3	—	—	—
	145/144-Pin																					
	100-Pin																—					
	64-Pin																					
	48-Pin																					
PC1	177/176-Pin	Hi-Z	MTIOC3A	—	TCLKD	—	—	PO18	—	—	—	SCK5	—	—	SSLA2	—	SDA3	—	ET _ERXD2	—	—	—
	145/144-Pin																					
	100-Pin																—					
	64-Pin																					
	48-Pin																					
PC2	177/176-Pin	Hi-Z	MTIOC4B	—	TCLKA	—	—	PO21	—	—	—	RXD5 SMISO5 SSCL5	—	—	SSLA3	—	—	IERXD	ET_RX _DV	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																		—			
	48-Pin																					
PC3	177/176-Pin	Hi-Z	MTIOC4D	—	TCLKB	—	—	PO24	—	—	—	TXD5 SMOSI5 SSDA5	—	—	—	—	—	IETXD	ET_TX _ER	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																		—			
	48-Pin																					
PC4	177/176-Pin	Hi-Z	MTIOC3D	MTCLKC	TIOCC6	TCLKE	TMCI1	PO25	POE0#	—	—	SCK5	CTS8# RTS8# SS8#	—	SSLA0	—	—	—	ET_TX _CLK	—	—	—
	145/144-Pin																					
	100-Pin				—	—																
	64-Pin																		—		USB0_ DPRPD	
	48-Pin																					
PC5	177/176-Pin	Hi-Z	MTIOC3B	MTCLKD	TIOCD6	TCLKF	TMRI2	PO29	—	—	—	SCK8	—	—	RSPCKA	—	—	—	ET _ETXD2	—	—	—
	145/144-Pin																					
	100-Pin				—	—																
	64-Pin																		—		USB0_ID	
	48-Pin																					
PC6	177/176-Pin	Hi-Z	MTIOC3C	MTCLKA	TIOCA6	—	TMCI2	PO30	—	—	—	RXD8 SMISO8 SSCL8	—	—	MOSIA	—	—	—	ET _ETXD3	—	—	—
	145/144-Pin																					
	100-Pin				—																	
	64-Pin																		—		USB0_ EXICEN	
	48-Pin																					
PC7	177/176-Pin	Hi-Z	MTIOC3A	MTCLKB	TIOCB6	—	TMO2	PO31	—	—	—	TXD8 SMOSI8 SSDA8	—	—	MISOA	—	—	—	ET_COL	—	—	—
	145/144-Pin																					
	100-Pin				—																	
	64-Pin																		—			
	48-Pin																					

Table 2.2.13 Port D

—: Setting prohibited —: Pin function eliminated (setting prohibited) : Pin eliminated

Port	Pin Count	Setting Value of Bits PSEL4 to PSEL0																				
		00000b	00001b	00010b	00011b	00100b	00101b	00110b	00111b	01000b	01001b	01010b	01011b	01100b	01101b	01110b	01111b	10000b	10001b	10010b	10011b	11000b
PD0	177/176-Pin	Hi-Z	—	—	TIOCA7	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	145/144-Pin																					
	100-Pin	—																				
	64-Pin																					
	48-Pin																					
PD1	177/176-Pin	Hi-Z	MTIOC4B	—	TIOCB7	TCLKG	—	—	—	—	—	—	—	—	MOSIC	—	—	CTX0	—	—	—	—
	145/144-Pin																					
	100-Pin				—	—									—							
	64-Pin																					
	48-Pin																					
PD2	177/176-Pin	Hi-Z	MTIOC4D	—	TIOCA8	—	—	—	—	—	—	—	—	—	MISOC	—	—	CRX0	—	—	—	—
	145/144-Pin																					
	100-Pin				—										—							
	64-Pin																					
	48-Pin																					
PD3	177/176-Pin	Hi-Z	—	—	TIOCB8	TCLKH	—	—	POE8#	—	—	—	—	—	RSPCKC	—	—	—	—	—	—	—
	145/144-Pin																					
	100-Pin				—	—									—							
	64-Pin																					
	48-Pin																					
PD4	177/176-Pin	Hi-Z	—	—	—	—	—	—	POE3#	—	—	—	—	—	SSLC0	—	—	—	—	—	—	—
	145/144-Pin																					
	100-Pin														—							
	64-Pin																					
	48-Pin																					
PD5	177/176-Pin	Hi-Z	MTIC5W	—	—	—	—	—	POE2#	—	—	—	—	—	SSLC1	—	—	—	—	—	—	—
	145/144-Pin																					
	100-Pin														—							
	64-Pin																					
	48-Pin																					
PD6	177/176-Pin	Hi-Z	MTIC5V	—	—	—	—	—	POE1#	—	—	—	—	—	SSLC2	—	—	—	—	—	—	—
	145/144-Pin																					
	100-Pin														—							
	64-Pin																					
	48-Pin																					
PD7	177/176-Pin	Hi-Z	MTIC5U	—	—	—	—	—	POE0#	—	—	—	—	—	SSLC3	—	—	—	—	—	—	—
	145/144-Pin																					
	100-Pin														—							
	64-Pin																					
	48-Pin																					

Table 2.2.14 Port E

—: Setting prohibited —: Pin function eliminated (setting prohibited) : Pin eliminated

Port	Pin Count	Setting Value of Bits PSEL4 to PSEL0																				
		00000b	00001b	00010b	00011b	00100b	00101b	00110b	00111b	01000b	01001b	01010b	01011b	01100b	01101b	01110b	01111b	10000b	10001b	10010b	10011b	11000b
PE0	177/176-Pin	Hi-Z	—	—	TIOCC9	—	—	—	—	—	—	—	—	SCK12	SSLB1	—	—	—	—	—	—	—
	145/144-Pin																					
	100-Pin				—																	
	64-Pin																					
	48-Pin																					
PE1	177/176-Pin	Hi-Z	MTIOC4C	—	TIOCD9	—	—	PO18	—	—	—	—	—	TXD12 SMOSI12 SSDA12 TXDX12 SIOX12	SSLB2	RSPCKB	—	—	—	—	—	—
	145/144-Pin																					
	100-Pin				—																	
	64-Pin																					
	48-Pin																					
PE2	177/176-Pin	Hi-Z	MTIOC4A	—	TIOCA9	—	—	PO23	—	—	—	—	—	RXD12 SMISO12 SSCL12 RXDX12	SSLB3	MOSIB	—	—	—	—	—	—
	145/144-Pin																					
	100-Pin				—																	
	64-Pin																					
	48-Pin																					
PE3	177/176-Pin	Hi-Z	MTIOC4B	—	TIOCB9	—	—	PO26	POE8#	—	—	—	—	CTS12# RTS12# SS12#	MISOB	—	—	—	ET _ERXD3	—	—	—
	145/144-Pin																					
	100-Pin				—														—			
	64-Pin																					
	48-Pin																					
PE4	177/176-Pin	Hi-Z	MTIOC4D	MTIOC1A	TIOCA10	—	—	PO28	—	—	—	—	—	—	SSLB0	—	—	—	ET _ERXD2	—	—	—
	145/144-Pin																					
	100-Pin				—														—			
	64-Pin																					
	48-Pin																					
PE5	177/176-Pin	Hi-Z	MTIOC4C	MTIOC2B	TIOCB10	—	—	—	—	—	—	—	—	—	RSPCKB	—	—	—	ET_RX _CLK	REF50CK	—	—
	145/144-Pin																					
	100-Pin				—														—	—		
	64-Pin																					
	48-Pin																					
PE6	177/176-Pin	Hi-Z	—	—	TIOCA11	—	—	—	—	—	—	—	—	—	MOSIB	—	—	—	—	—	—	—
	145/144-Pin																					
	100-Pin				—																	
	64-Pin																					
	48-Pin																					
PE7	177/176-Pin	Hi-Z	—	—	TIOCB11	—	—	—	—	—	—	—	—	—	MISOB	—	—	—	—	—	—	—
	145/144-Pin																					
	100-Pin				—																	
	64-Pin																					
	48-Pin																					

Table 2.2.15 Port F

—: Setting prohibited —: Pin function eliminated (setting prohibited) : Pin eliminated

Port	Pin Count	Setting Value of Bits PSEL4 to PSEL0																				
		00000b	00001b	00010b	00011b	00100b	00101b	00110b	00111b	01000b	01001b	01010b	01011b	01100b	01101b	01110b	01111b	10000b	10001b	10010b	10011b	11000b
PF0	177/176-Pin	Hi-Z	—	—	—	—	—	—	—	—	—	TXD1 SMOSI1 SSDA1	—	—	—	—	—	—	—	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
PF1	177/176-Pin	Hi-Z	—	—	—	—	—	—	—	—	—	SCK1	—	—	—	—	—	—	—	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
PF2	177/176-Pin	Hi-Z	—	—	—	—	—	—	—	—	—	RXD1 SMISO1 SSCL1	—	—	—	—	—	—	—	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
PF3	177/176-Pin	—																				
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
PF4	177/176-Pin	—																				
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
PF5	177/176-Pin	—																				
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
PF6	177/176-Pin																					
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
PF7	177/176-Pin																					
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					

Table 2.2.16 Port J

—: Setting prohibited —: Pin function eliminated (setting prohibited) : Pin eliminated

Port	Pin Count	Setting Value of Bits PSEL4 to PSEL0																				
		00000b	00001b	00010b	00011b	00100b	00101b	00110b	00111b	01000b	01001b	01010b	01011b	01100b	01101b	01110b	01111b	10000b	10001b	10010b	10011b	11000b
PJ0	177/176-Pin																					
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
PJ1	177/176-Pin																					
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
PJ2	177/176-Pin																					
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
PJ3	177/176-Pin	Hi-Z	MTIOC3C	—	—	—	—	—	—	—	—	CTS6# RTS6# SS6#	CTS0# RTS0# SS0#	—	—	—	—	—	—	—	—	—
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
PJ4	177/176-Pin																					
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
PJ5	177/176-Pin	—																				
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
PJ6	177/176-Pin																					
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					
PJ7	177/176-Pin																					
	145/144-Pin																					
	100-Pin																					
	64-Pin																					
	48-Pin																					

3. Reference Documents

User's Manual: Hardware

RX63N Group and RX631 Group User's Manual: Hardware Rev.1.50
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

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REVISION HISTORY	RX63N Group and RX631 Group Application Note Differences by Pin Count in MPC Pin Functions

Rev.	Date	Description	
		Page	Summary
1.00	Sep. 26, 2013	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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