RX62T

MTU3 Phase Counting Mode

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Introduction

The RX62T Group has on-chip multi-function timer pulse unit 3 (MTU3), which comprises eight 16-bit timer channels.

Target Device

RX62T

Contents

1. Specification

- Comprises eight 16-bit channels
- Operating frequency is 8 to100 MHz
- [Channels 0 to 4, 6, and 7]
- Waveform output on compare match
- Input capture function
- Counter-clearing operation
- Simultaneous writing to multiple timer counters (TCNT)
- Simultaneous clearing on compare match or input capture
- Simultaneous input and output to registers in synchronization with counter operations
- Up to 12-phase PWM output in combination with synchronous operation
- [Channels 0, 3, 4, 6, and 7]
- Buffer operation specifiable
- [Channels 3, 4, 6, and 7]
- Through interlocked operation of channels 3 and 4 or 6 and 7, output of positive and negative signals in six phases (for a total of 12 phases) in Complementary -PWM and reset-PWM operation
- In Complementary PWM mode, transfer of values from buffer registers to temporary registers on peaks and troughs of the timer-counter values or writing to the buffer registers (MTU3_4.TGRD and MTU3_7.TGRD)
- Double-buffering selectable in Complementary PWM mode
- [Channels 3 and 4]
- Through interlocking with channel 0, a mode for driving AC synchronous motors (brushless DC motors) by using Complementary PWM output and reset PWM output is settable and allows the selection of two types of waveform output (chopping or level)
- [Channels 1 and 2]
- Independently specifiable phase-counting mode
- Capable of cascade-connected operation
- [Channel 5]
- Capable of operation as a dead-time compensation counter

Fig. 1-1 is the block diagram of Multi-Function Timer Pulse Unit 3 (MTU3).

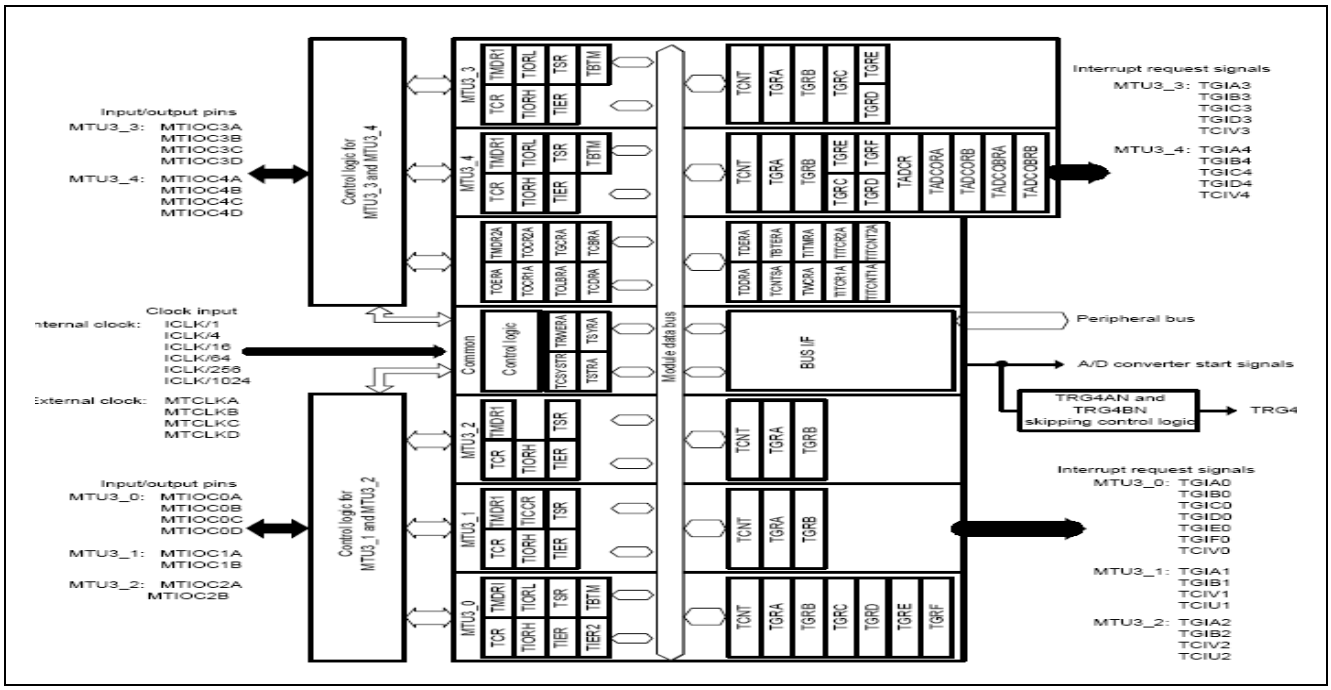


Figure 1-1 Block diagram for MTU3

Table 1-1 Specifications of Multi-Function Timer Pulse Unit 3 (MTU3) Register

TSTR	Timer start register
TOERA	Timer output master enable register A
TGCRA	Timer gate control register A
TOCR1A	Timer output control register 1A
TOCR2A	Timer output control register 2A
TCDRA	Timer cycle data register A
TDDRA	Timer dead time data register A
TCNTSA	Timer subcounter A
TCBRA	Timer cycle buffer register A
TITCR1A	Timer interrupt skipping set register 1A
TITCR2A	Timer interrupt skipping set register 2A
TITCNT1A	Timer interrupt skipping counter 1A
TITCNT2A	Timer interrupt skipping counter 2A
TBTERA	Timer buffer transfer set register A
TOLBRA	Timer output level buffer register A
TCR	Timer control register
TMDR1	Timer mode register 1
TMDR2A	Timer mode register 2A
TIORH	Timer I/O control register H
TIORL	Timer I/O control register L
TIER	Timer interrupt enable register
TCNT	Timer counter
TGRA	Timer general register A
TGRB	Timer general register B
TGRC	Timer general register C
TGRD	Timer general register D
TGRE	Timer general register E
TGRF	Timer general register F
TSR	Timer status register
TDERA	Timer dead time enable register A
TBTM	Timer buffer operation transfer mode register
TADCR	Timer A/D converter start request control register
TADCORA	Timer A/D converter start request cycle set register A
TADCORB	Timer A/D converter start request cycle set register B
TADCOBRA	Timer A/D converter start request cycle set buffer register A
TADCOBRB	Timer A/D converter start request cycle set buffer register B

2. Multi-Function Timer Pulse Unit 3 for Phase Counting Mode

2.1 Example of Phase Counting Mode operation

In phase counting mode, the phase difference between two external input clocks is detected and TCNT is incremented or decremented accordingly. This mode can be set for channels 1 and 2.

When phase counting mode is specified, an external clock is selected as the counter input clock and TCNT operates as an up/down-counter regardless of the setting of bits TPSC[2:0] and bits CKEG[1:0] in TCR. However, the functions of bits CCLR[1:0] in TCR and of TIOR, TIER, and TGR are valid, and input capture/compare match and interrupt functions can be used.

This can be used for two-phase encoder pulse input.

If an overflow occurs while TCNT is counting up, the TCFV flag in TSR is set to 1. If an underflow occurs while TCNT is counting down, the TCFU flag is TSR is set to 1.

The TCFD flag in TSR is the count direction flag. Read the TCFD flag to check whether TCNT is counting up or down.

Fig. 2-1 shows an example of Phase Counting Mode operation.

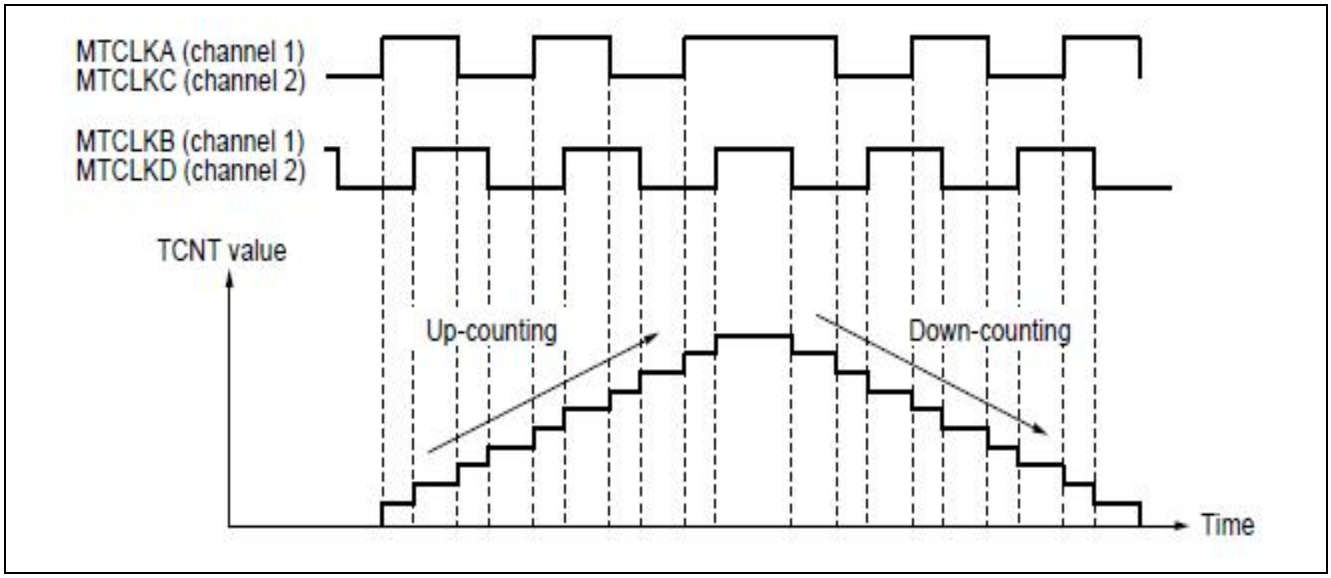


Figure 2-1 Example of Phase Counting Mode operation

2.2 Example of Procedure for Setting Phase Counting Mode

Fig. 2-2 shows an example of the procedure for setting Phase Counting Mode.

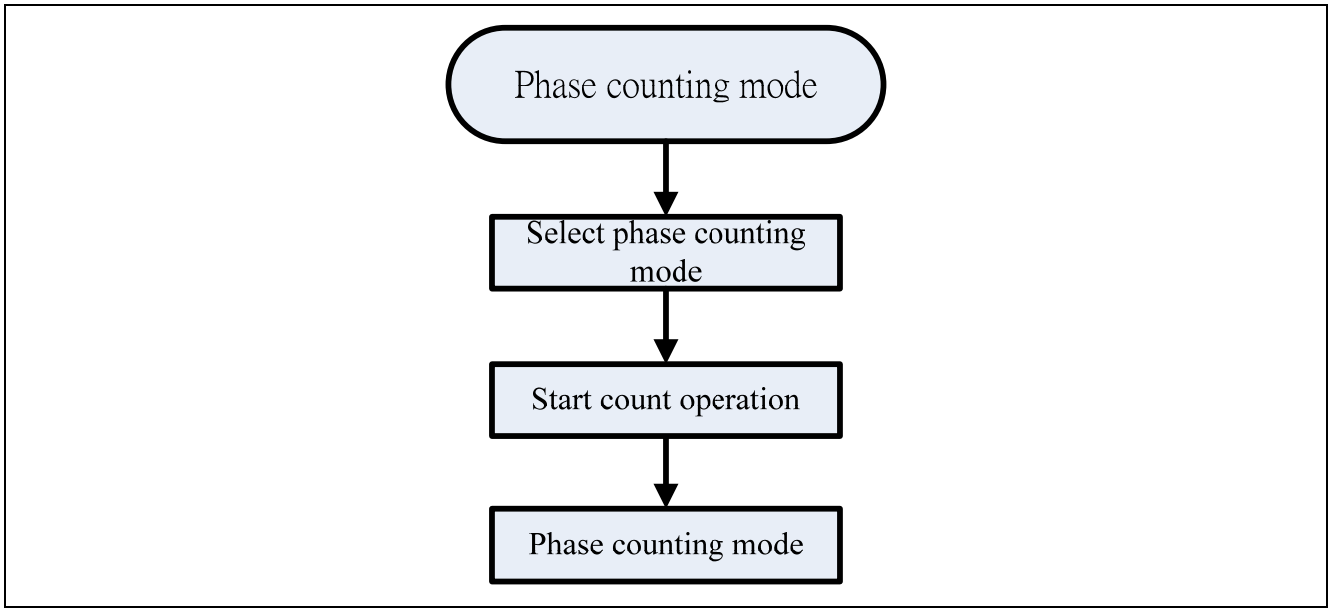


Figure 2-2 Example of Procedure for Setting Phase Counting Mode

2.3 Phase Counting Mode Application Example

Fig. 2-3 shows an example in which channel 1 is in phase counting mode, and channel 1 is coupled with channel 0 to input 2-phase encoder pulses of a servo motor in order to detect position or speed.

Channel 1 is set to phase counting mode, and the encoder pulse A-phase and B-phase are input to MTCLKA and MTCLKB.

In channel 0, MTU0.TGRC compare match is specified as the TCNT clearing source and MTU0.TGRA and MTU0.TGRC are used for the compare match function and are set with the speed control cycle and position control cycle. MTU0.TGRB is used for input capture, with MTU0.TGRB and MTU0.TGRD operating in buffer mode. The channel 1 counter input clock is designated as the MTU3_0.TGRB input capture source, and the widths of 2-phase encoder 4-multiplication pulses are detected.

MTU1.TGRA and MTU1.TGRB for channel 1 are designated for the input capture function and MTU0.TGRA and MTU0.TGRC compare matches in channel 0 are selected as the input capture sources to store the up/down-counter values for the control cycles.

This procedure enables the accurate detection of position and speed.

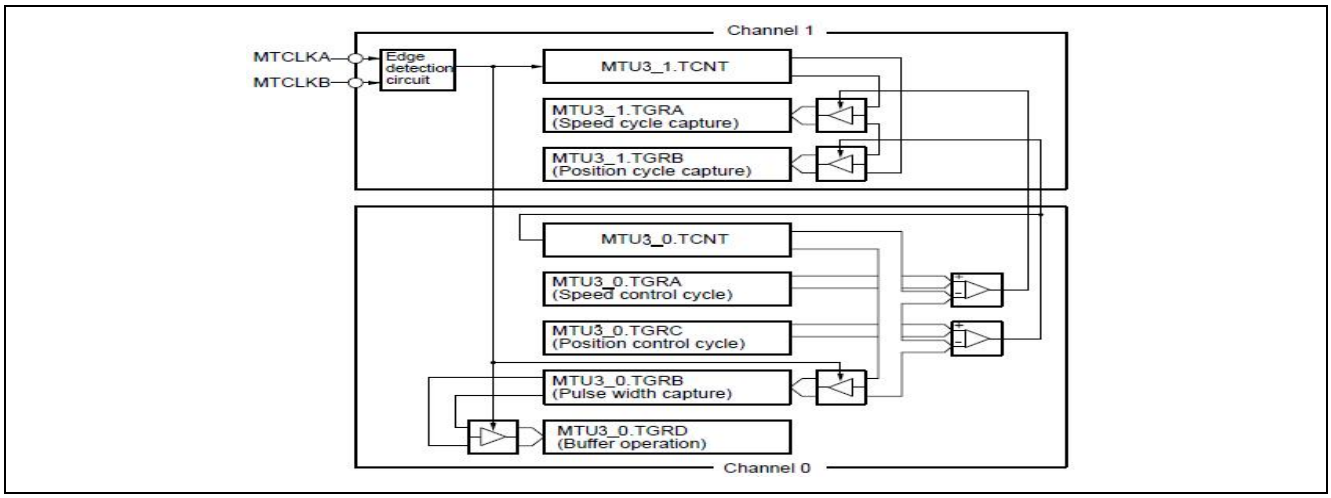


Figure 2-3 Phase Counting Mode Application Example

3. Multi-Function Timer Pulse Unit 3 Software Register Setting

Timer Control Register (TCR):

TCR controls the TCNT operation for each channel. The MTU has a total of ten TCR registers, one each for channels 0 to 4, 6, and 7. TCR values should be specified only while TCNT operation is stopped.

	b7	b6	b5	b4	b3	b2	b1	b0
	CCLR[2:0]			CKEG[1:0]		TPSC[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	TPSC[2:0]	Time Prescaler Select	See tables 15.7 to 15.10.	R/W
b4, b3	CKEG[1:0]	Clock Edge Select	b4 b3 0 0: Count at rising edge 0 1: Count at falling edge 1 x: Count at both edges	R/W
b7 to b5	CCLR[2:0]	Counter Clear	See tables 15.5 and 15.6.	R/W

[Legend]
x: Don't care

Figure 3-1 TCR Setting

Timer General Register (TGR):

TGR is a 16-bit readable/writable register.

TGRA, TGRB, TGRC, and TGRD function as either output compare or input capture registers. TGRC and TGRD for channels 0, 3, 4, 6, and 7 can also be designated for operation as buffer registers. TGR buffer register combinations are TGRA and TGRC, and TGRB and TGRD.

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: TGR must not be accessed in eight bits; it should always be accessed in 16 bits. TGR is initialized to FFFFh.

Figure 3-2 TGR Setting

Timer Mode Register (TMDR):

TMDR1 specifies the operating mode of each channel. The MTU3 has a total of seven TMDR1 registers, one each for channels 0 to 4, 6, and 7. TMDR1 values should be specified only while TCNT operation is stopped.

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	BFB	BFA	MD[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	MD[3:0]	Mode Select	These bits specify the timer operating mode. See table 15.12 for details.	R/W
b4	BFA	Buffer Operation A	0: TGRA and TGRC operate normally 1: TGRA and TGRC used together for buffer operation	R/W
b5	BFB	Buffer Operation B	0: TGRB and TGRD operate normally 1: TGRB and TGRD used together for buffer operation	R/W
b6	BFE	Buffer Operation E	0: MTU3_0.TGRE and MTU3_0.TGRF operate normally 1: MTU3_0.TGRE and MTU3_0.TGRF used together for buffer operation	R/W
b7	—	(Reserved)	This bit is always read as 0. The write value should be 0.	R/W

Figure 3-3 TMDR Setting

4. Experimental Result

Fig. 4-1shows an example of operation in phase counting mode 1, and variable A in sample code summarizes the TCNT up-count/down-count conditions.

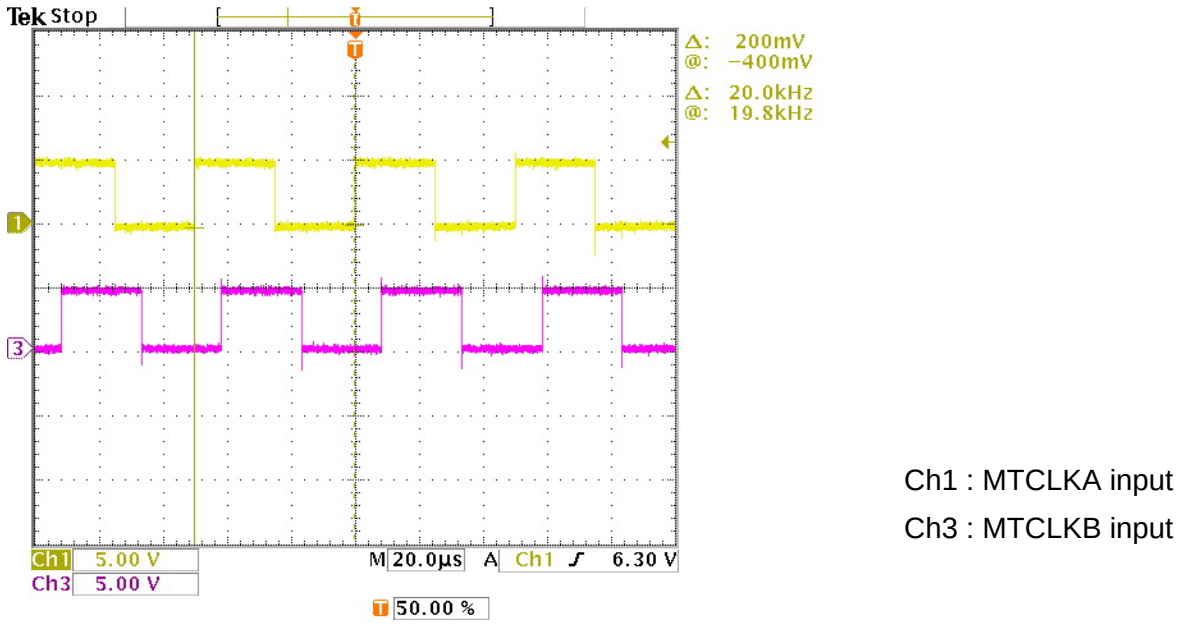


Figure 4-1 MTCLKA and MTCLKB input for encoder pulse

Fig. 4-2 shows an example of operation in phase counting mode 2, and variable A in sample code summarizes the TCNT up-count/down-count conditions.

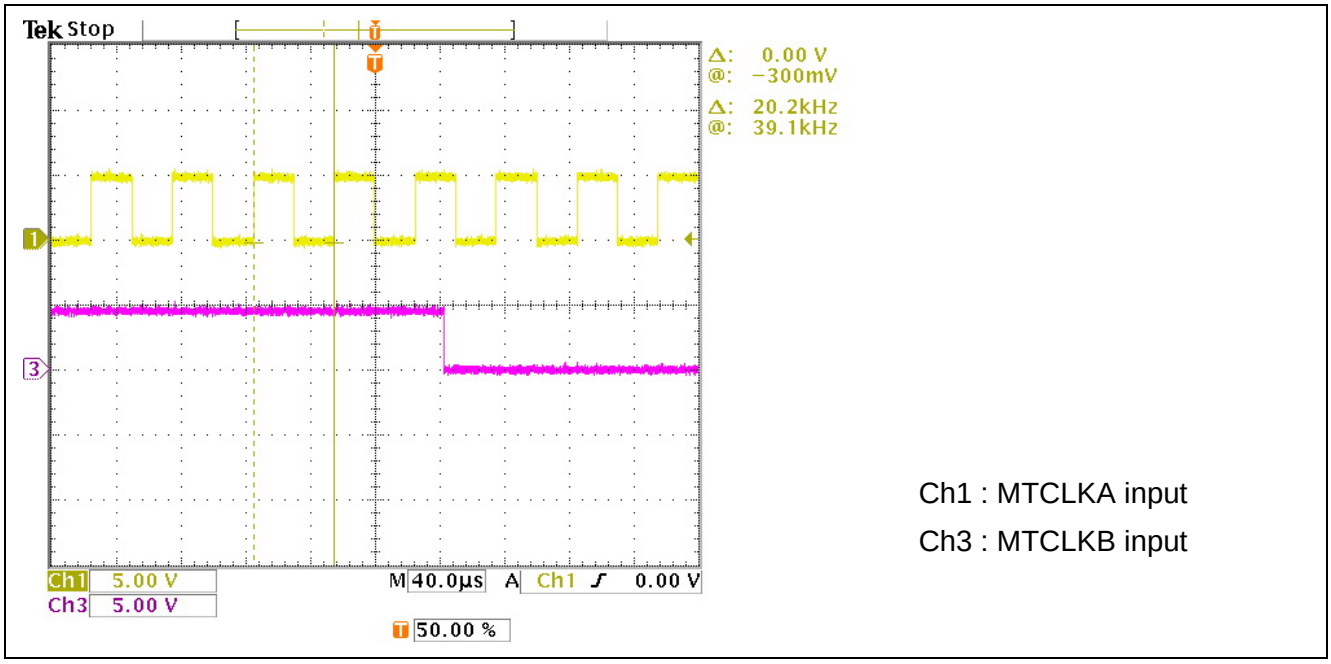


Figure 4-2 MTCLKA and MTCLKB input for encoder pulse

Fig. 4-3 shows an example of operation in phase counting mode 3, and variable A in sample code summarizes the TCNT up-count/down-count conditions.

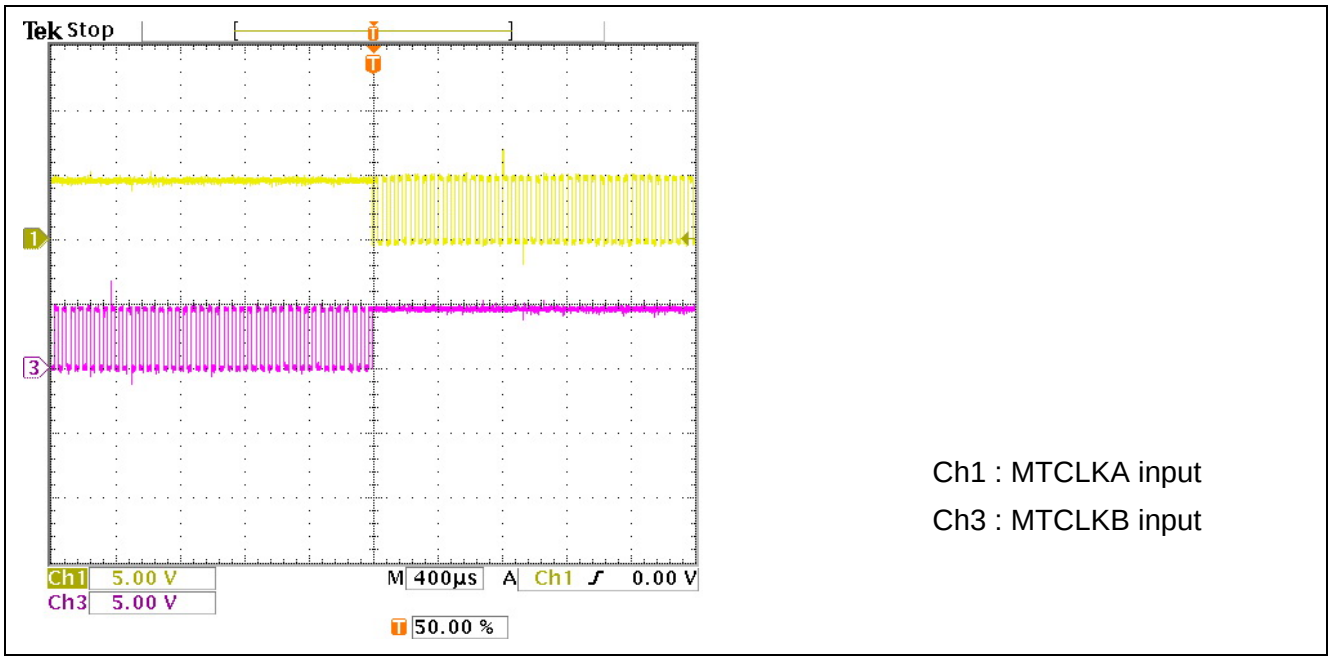
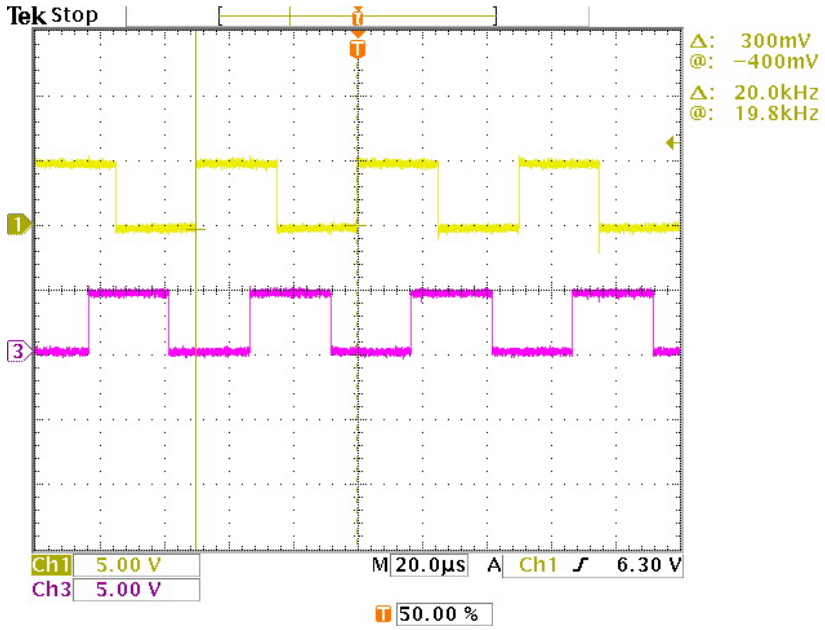


Figure 4-3 MTCLKA and MTCLKB input for encoder pulse

Fig. 4-4 shows an example of operation in phase counting mode 4, and variable A in sample code summarizes the TCNT up-count/down-count conditions.



Ch1 : MTCLKA input

Ch3 : MTCLKB input

Figure 4-4 MTCLKA and MTCLKB input for encoder pulse

5. Conclusion

We can use Multi-Function Timer Pulse Unit 3 for Phase Counting Mode control.

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	October 1. 11	—	First edition issued

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   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

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   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
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   Access to reserved addresses is prohibited.

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4. Clock Signals

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