

RX62T

MTU3 Complementary PWM Mode

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Introduction

The RX62T Group has on-chip Multi-Function Timer Pulse Unit 3 (MTU3), which comprises eight 16-bit timer channels.

Target Device

RX62T

Contents

| 1. | Specification | 2 |
|-----|--|----|
| 2.1 | Multi-Function Timer Pulse Unit 3 for Complementary PWM Mode Example of Complementary PWM mode operation Example of Procedure for Setting Complementary PWM Mode | 4 |
| 3. | Multi-Function Timer Pulse Unit 3 Software Register Setting | 6 |
| 4. | Experiment Result | 9 |
| 5. | Conclusion | 10 |



1. Specification

- Comprises eight 16-bit channels
- Operating frequency is 8 to100 MHz
- [Channels 0 to 4, 6, and 7]
- Waveform output on compare match
- Input capture function
- Counter-clearing operation
- Simultaneous writing to multiple timer counters (TCNT)
- Simultaneous clearing on compare match or input capture
- Simultaneous input and output to registers in synchronization with counter operations
- Up to 12-phase PWM output in combination with synchronous operation
- [Channels 0, 3, 4, 6, and 7]
- Buffer operation specifiable
- [Channels 3, 4, 6, and 7]
- Through interlocked operation of channels 3 and 4 or 6 and 7, output of positive and negative signals in six phases (for a total of 12 phases) in Complementary -PWM and reset-PWM operation
- In Complementary PWM mode, transfer of values from buffer registers to temporary registers on peaks and troughs of the timer-counter values or writing to the buffer registers (MTU3_4.TGRD and MTU3_7.TGRD)
- Double-buffering selectable in Complementary PWM mode
- [Channels 3 and 4]
- Through interlocking with channel 0, a mode for driving AC synchronous motors (brushless DC motors) by using Complementary PWM output and reset PWM output is settable and allows the selection of two types of waveform output (chopping or level)
- [Channels 1 and 2]
- Independently specifiable phase-counting mode
- Capable of cascade-connected operation
- [Channel 5]
- Capable of operation as a dead-time compensation counter

Figure 1-1 is the block diagram of Multi-Function Timer Pulse Unit 3 (MTU3).

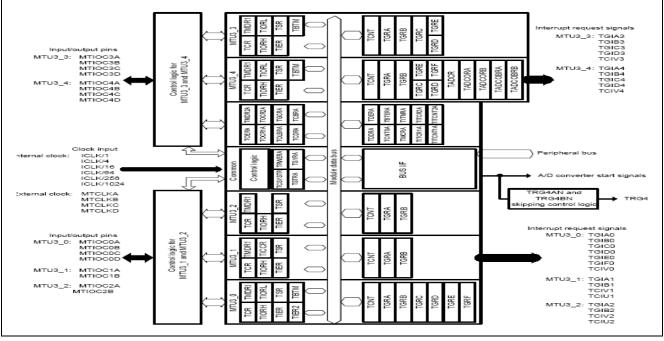


Figure 1-1 Block diagram for MTU3



Table 1-1 Specifications of Multi-Function Timer Pulse Unit 3 (MTU3) Register

| <u>г</u> | |
|----------|---|
| TSTR | Timer start register |
| TOERA | Timer output master enable register A |
| TGCRA | Timer gate control register A |
| TOCR1A | Timer output control register 1A |
| TOCR2A | Timer output control register 2A |
| TCDRA | Timer cycle data register A |
| TDDRA | Timer dead time data register A |
| TCNTSA | Timer subcounter A |
| TCBRA | Timer cycle buffer register A |
| TITCR1A | Timer interrupt skipping set register 1A |
| TITCR2A | Timer interrupt skipping set register 2A |
| TITCNT1A | Timer interrupt skipping counter 1A |
| TITCNT2A | Timer interrupt skipping counter 2A |
| TBTERA | Timer buffer transfer set register A |
| TOLBRA | Timer output level buffer register A |
| TCR | Timer control register |
| TMDR1 | Timer mode register 1 |
| TMDR2A | Timer mode register 2A |
| TIORH | Timer I/O control register H |
| TIORL | Timer I/O control register L |
| TIER | Timer interrupt enable register |
| TCNT | Timer counter |
| TGRA | Timer general register A |
| TGRB | Timer general register B |
| TGRC | Timer general register C |
| TGRD | Timer general register D |
| TGRE | Timer general register E |
| TGRF | Timer general register F |
| TSR | Timer status register |
| TDERA | Timer dead time enable register A |
| ТВТМ | Timer buffer operation transfer mode register |
| TADCR | Timer A/D converter start request control register |
| TADCORA | Timer A/D converter start request cycle set register A |
| TADCORB | Timer A/D converter start request cycle set register B |
| TADCOBRA | Timer A/D converter start request cycle set buffer register A |
| TADCOBRB | Timer A/D converter start request cycle set buffer register B |



2. Multi-Function Timer Pulse Unit 3 for Complementary PWM Mode

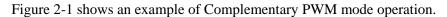
2.1 Example of Complementary PWM mode operation

In Complementary PWM mode, three phases of non-overlapping positive and negative PWM waveforms (six phases in total) can be output by combining channels 3 and 4 and channels 6 and 7. PWM waveforms without non-overlapping interval are also available.

In Complementary PWM mode, MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D, MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7B, MTIOC7C, and MTIOC7D pins function as PWM output pins, and the MTIOC3A and MTIOC6A pins can be set for toggle output synchronized with the PWM cycle.

MTU3_3.TCNT, MTU3_4.TCNT, MTU3_6.TCNT, and MTU3_7.TCNT function as up/down-counters.

A function to directly cut off the PWM output by using an external signal is supported as a port function.



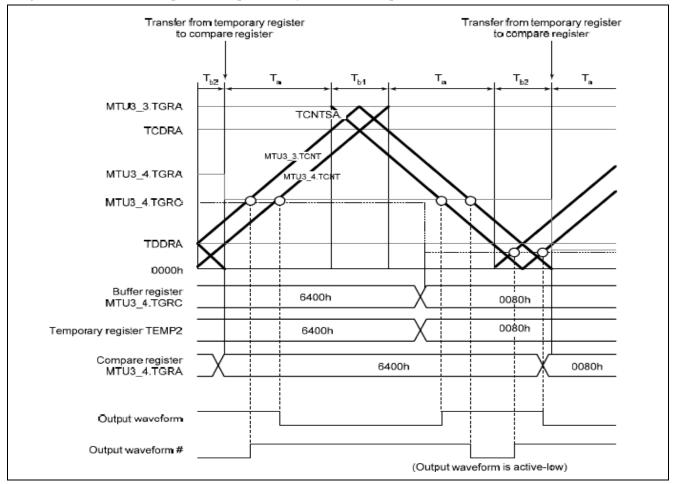


Figure 2-1 Example of Complementary PWM mode operation



2.2 Example of Procedure for Setting Complementary PWM Mode

Figure 2-2 shows an example of the procedure for setting Complementary PWM mode.

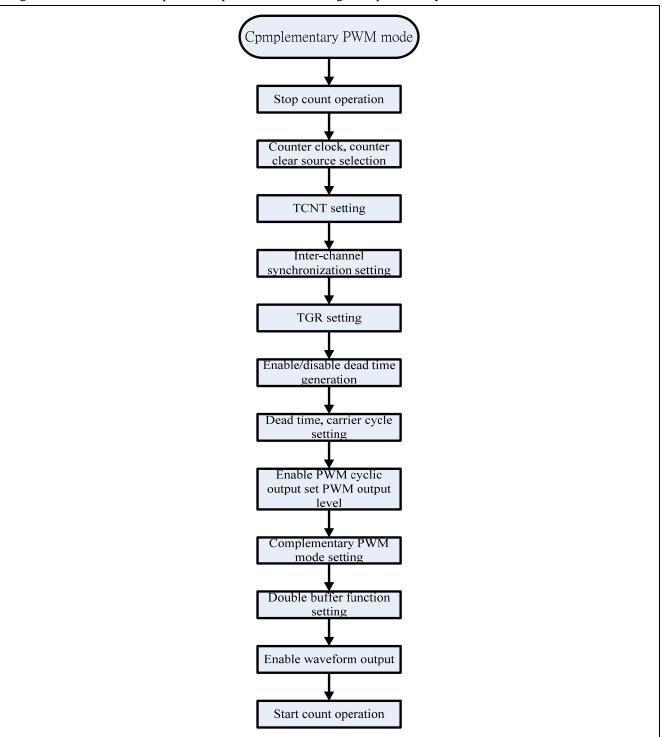


Figure 2-2 Example of Procedure for Setting Complementary PWM Mode



3. Multi-Function Timer Pulse Unit 3 Software Register Setting

Timer Control Register (TCR):

TCR controls the TCNT operation for each channel. The MTU3 has a total of ten TCR registers, one each for channels 0 to 4, 6, and 7. TCR values should be specified only while TCNT operation is stopped.

| | | | | CKEG[1:0] | | | TPSC[2:0] | | 3 | |
|------------|-------------------|----------------|--------|-----------|---------------|-----------|-----------|---|---|-----|
| V | alue after reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| Bit | Symbol | Bit Name | | Des | cription | | | | | R/W |
| b2 to b0 | TPSC[2:0] | Time Prescaler | Select | See | tables 15.7 t | to 15.10. | | | | R/W |
| b4, b3 | CKEG[1:0] | Clock Edge Sel | lect | b4 b | 3 | | | | | R/W |
| | | | | 0 0: | Count at risi | ng edge | | | | |
| | | | | 0 1: | Count at fall | ing edge | | | | |
| | | | | 1 x: | Count at bot | h edges | | | | |
| b7 to b5 | CCLR[2:0] | Counter Clear | | See | tables 15.5 | and 15.6. | | | | R/W |
| Legend] | | | | | | | | | | |
| : Don't ca | are | | | | | | | | | |

Figure 3-1 TCR Setting

Timer General Register (TGR):

TGR is a 16-bit readable/writable register.

TGRA, TGRB, TGRC, and TGRD function as either output compare or input capture registers. TGRC and TGRD for channels 0, 3, 4, 6, and 7 can also be designated for operation as buffer registers. TGR buffer register combinations are TGRA and TGRC, and TGRB and TGRD.

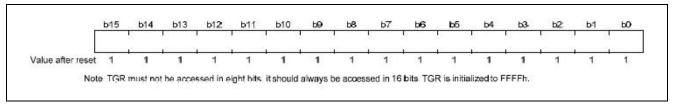


Figure 3-2 TGR Setting

Timer Dead Time Enable Registers (TDERA and TDERB):

TDERA and TDERB control dead time generation in Complementary PWM mode. The MTU3 has one TDER each for channel 3 and channel 6. TDERA and TDERB should be modified only while TCNT stops.



| | _ | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | |
|-----------|----------------|--------------------|--|----|------------------|-------------------------------------|----------|----|----|------|
| | | | - | - | - | - | - 1 | - | - | TDER |
| V | alue after re | eset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| | | | | | | | | | | |
| Bit | Symbol | Bit Name | e | | Descrip | tion | | | | R/W |
| Bit b0 | Symbol TDER | 1000-000-000-000-0 | e ne Enable | | the state of the | tion ad tim <mark>e is</mark> ge | enerated | | | |
| Bit | | 1000-000-000-000-0 | Contraction of the local sectors of the local secto | | 0: No de | | | | | R/W |



Timer Output Control Registers (TOCRA):

TOCR1A and TOCR1B enable or disable PWM-synchronized toggle output in Complementary PWM mode and reset-synchronized PWM mode, and control inversion of PWM output level.

| | | _ | b7 | b6 | b5 | b4 | b3 | b2 | b1 | bO | |
|--------------|--------------|----------------------------------|-----------|----------------------------------|---|---------------|--------------|----------------|-----------------|-------|--|
| | | [| — | PSYE | I | — | TOCL | TOCS | OLSN | OLSP | |
| Va | lue after re | eset | 0 | 0 | 0 | 0 | 0 * | 0 | 0 | 0 | |
| Bit | Symbol | Note: Bit Nan | written | t can be set to ' to the bit. | Descrip | 020 | power-on re: | set. After 1 i | is written. O c | R/W | |
| bO | OLSP | Output Level Select P *2 | | | See tabl | R/W | | | | | |
| b1 | OLSN | Output Level Select N *2 | | | See table 15.39. | | | | | | |
| b2 | TOCS | TOC Select | | | 0: TOCF | R/W | | | | | |
| b3 | TOCL | TOC Register Write Protection *1 | | | CL TOC Register Write Protection *1 0: Write access to the TOCS, OLSN, and OLSP bits is enabled 1: Write access to the TOCS, OLSN, and OLSP bits is disabled | | | | | | |
| | 20 - 20 - | (Reserv | /ed) | | These b | . R/W | | | | | |
| b5, b4 | | PWM Synchronous Output Enable | | | 0: Toggle output is disabled | | | | | | |
| | PSYE | PWM S | ynchronou | s Output Enable | o. roggi | e eacharte . | | | | | |
| b5, b4 b6 | PSYE | PWM S | ynchronou | s Output Enable | | e output is e | | | | 0.000 | |

Figure 3-4 TOCRA Setting

Timer Mode Register (TMDR):

TMDR1 specifies the operating mode of each channel. The MTU3 has a total of seven TMDR1 registers, one each for channels 0 to 4, 6, and 7. TMDR1 values should be specified only while TCNT operation is stopped.



| | | b7 | b6 | b5 | ь4 | Ь3 | Ь2 | b1 | ьо | |
|--------------------|---------|--|--|-------------|-------------|--------------|----------------|---------------|-----|-----|
| Value after reset: | | - | | BFB | BFA | | MD[| 3:0] | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| Bit | Symbol | Bit Name | | Descripti | on | | | | | R/W |
| b3 to b0 | MD[3:0] | Mode Select | ode Select These bits specify the timer operating mode. See table 15.12 for details. | | | | | | | |
| b4 | BFA | Buffer Operation | A | 0: TGRA | and TGRC of | perate norma | ally | | | R/W |
| 5 | | | | 1: TGRA | and TGRC us | sed together | for buffer op | eration | | |
| b5 | BFB | Buffer Operation | B | 0: TGRB | and TGRD of | perate norma | ally | | | R/W |
| | | Str. | | 1: TGRB | and TGRD us | sed together | for buffer op | eration | | |
| b6 | BFE | Buffer Operation E 0: MTU3_0.TGRE and MTU3_0.TGRF operate normally | | | | | | | R/W | |
| | | | | 1: MTU3_ | 0.TGRE and | MTU3_0.TO | GRF used tog | ether for buf | fer | |
| | | | | operati | on | | | | | |
| b7 | | (Reserved) | | This bit is | always read | as 0. The w | rite value sho | ould be 0. | | R/W |

Figure 3-5 TMDR Setting

Timer Output Master Enable Register (TOER):

TOERA enables or disables output settings for output pins MTIOC4D, MTIOC4C, MTIOC3D, MTIOC4B, MTIOC4A, and MTIOC3B.

TOERB enables or disables output settings for output pins MTIOC7D, MTIOC7C, MTIOC6D, MTIOC7B, MTIOC7A, and MTIOC6B.

These pins do not output correctly if the TOER bits have not been set. In channels 3, 4, 6, and 7, set TOER prior to setting TIOR.

| | | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|------------|------------------|---|--------------------------|--------|---|------------------------------|--------------|----------------|---------------|--------------|
| | | | | | OE4D | OE4C | OE3D | OE4B | OE4A | OE3B |
| | Value after rese | t: | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | Symbol | Bit N | ame | | Des | cription | | | | R/W |
| 00 | OE3B | Maste | er Enable M | TIOC3B | | TU3 output i TU3 output i | | | | R/W |
| b1 | OE4A | Maste | er Enable M | TIOC4A | 0: MTU3 output is disabled * 1: MTU3 output is enabled | | | | | R/W |
| o2 | OE4B | Master Enable MTIOC4B 0: MTU3 output is disabled * 1: MTU3 output is enabled | | | | | R/W | | | |
| 03 | OE3D | Master Enable MTIOC3D | | | 0: MTU3 output is disabled * 1: MTU3 output is enabled | | | | | R/W |
| b 4 | OE4C | Master Enable MTIOC4C | | | 0: MTU3 output is disabled * 1: MTU3 output is enabled | | | R/W | | |
| 5 | OE4D | Maste | er Enable M ⁻ | TIOC4D | | TU3 output i TU3 output i | | | | R/W |
| b7, b6 | | (Rese | erved) | | The | se bits are al | ways read as | s 1. The write | e value shoui | ld be 1. R/W |

Figure 3-6 TOER Setting



4. Experiment Result

Fig. 4-1 to Fig. 4-3 the f_{sw} is 20 kHz, dead_time is 2 *us*. Fig. 4-1 is MTU3 for 25% duty; Fig. 4-2 is MTU3 for 50% duty; and Fig. 4-3 is MTU3 for 75% duty.

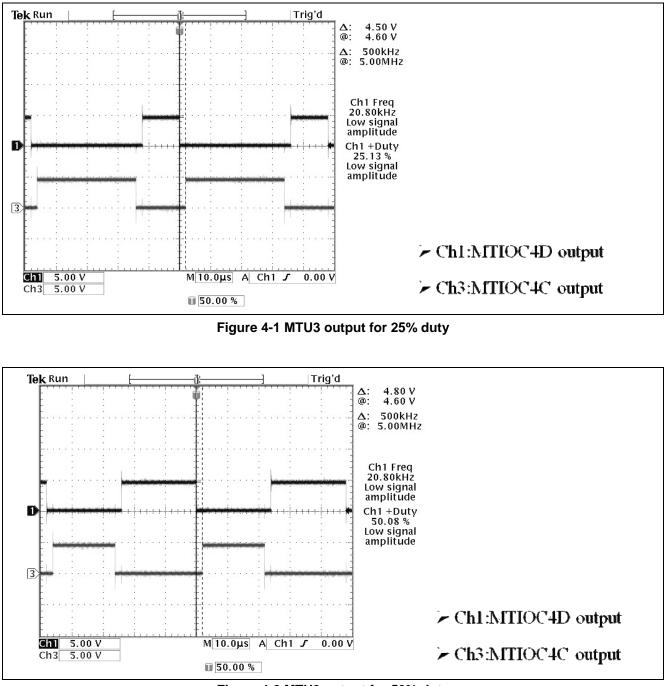


Figure 4-2 MTU3 output for 50% duty





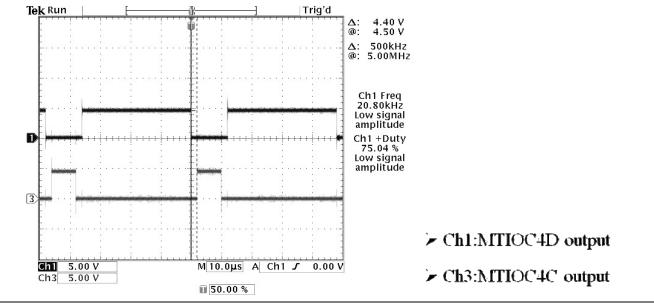


Figure 4-3 MTU3 output for 75% duty

5. Conclusion

From experimental result, we can use Multi-Function Timer Pulse Unit 3 for Complementary PWM control.

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| | | Descript | ion |
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