# RX62T Group

Usage Example of 12-Bit AD Converter in One Shunt Current Detection Method

## Contents

# 1    Overview

## 1.1    Configuration

This application note describes a setting example of AD detection timing synchronized with PWM output and examples of using built-in programmable gain amplifiers (hereinafter referred to as PGA) and built-in comparators on the basis of a motor control board using one shunt current detection method (Figure 1).

Settings for S/W registers in this application note are generated by using Renesas Electronics' free tool, 'Peripheral I/O driver generator tool: Peripheral Driver Generator V.2 (hereinafter called PDG2) Ver2.02'. For details of register setting values, refer to PDG2 User's Manual.
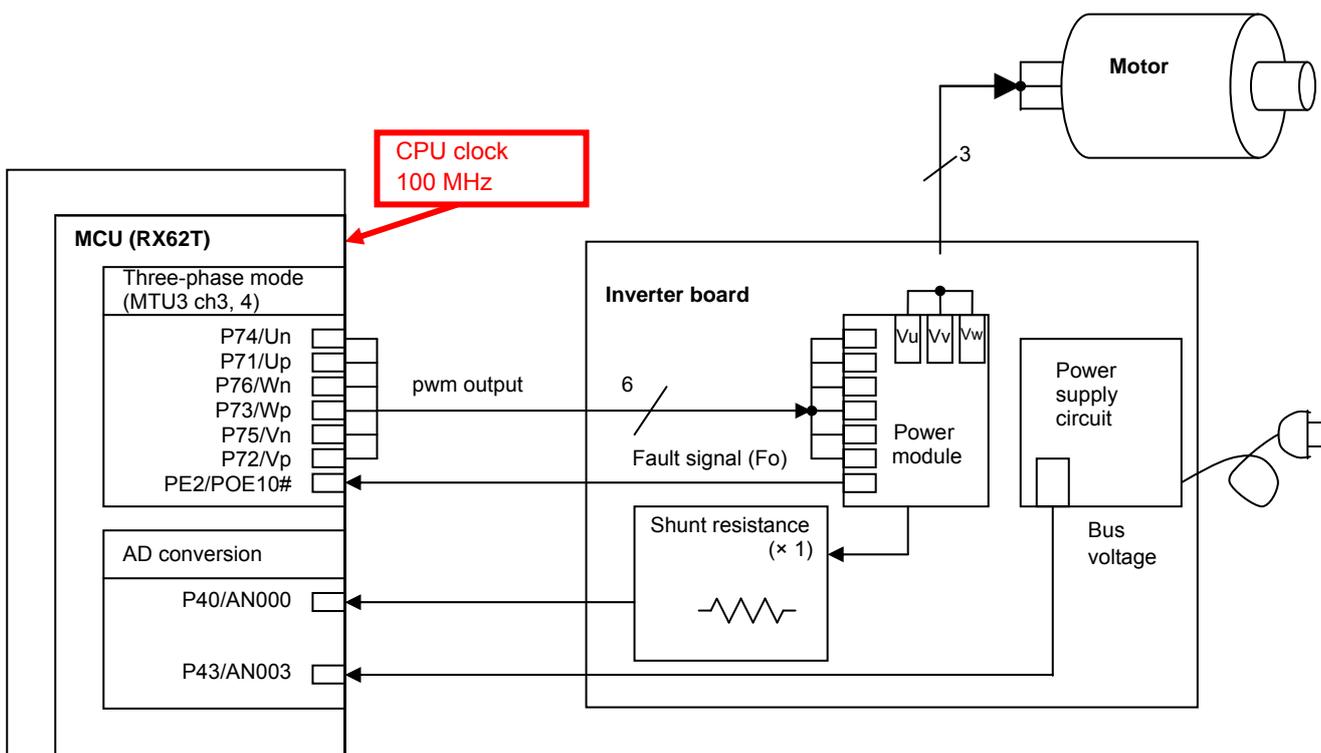


**Figure 1. System Configuration Diagram**

## 1.2     List of Used Functions

Table 1 shows a list of RX62T functions used in this application note.

**Table 1. List of Functions Used by S/W**

| Function | Name | Content |
|---|---|---|
| Three-phase output | MTU3 (ch3,4) | · Sine wave output using the complementally PWM mode by MTU3 (ch3, 4)<br>· Input two times at any given timing of three-phase PWM using AD delayed trigger generator function |
| Current input for shunt | 12-bit ADA (AN000) | · Support one shunt current detection method with AD 1 ch (double data registers) |
| Shunt current amplification | PGA | · The shunt current is amplified twice by using a built-in PGA. |
| Bus voltage input | 12-bit ADA (AN003) | · AD input by trigger from MTU3 synchronization |
| Fault signal input | POE (POE10) | · Shutdown of three-phase outputs upon detecting the "falling" edge of overcurrent signal when a fault occurs from IPM.<br> (High impedance) |
| Overcurrent detection | Comparator in 12-bit ADA | ·Shutdown of three-phase outputs upon detecting positive and negative overcurrents by using the window comparator function. |

## 2    Contents of Control

### 2.1    Port Assignment

**Table 2. Port Assignment**

| Purpose of Use | I/O | RX62T | | RX62T-RSK | |
| --- | --- | --- | --- | --- | --- |
| | | Use function | Pin No | JA | J |
| Vcc | HW | Vcc | 14,42,60 | JA1-1,JA6-23 | J1-1,J2-17,J3-10 |
| Vss | HW | Vss | 3,12,44,62 | JA1-2,4,JA2-4,JA6-24 | J1-3,12,J2-19,J3-12 |
| VCL | HW | VCL | 5 | – | – |
| AVcc | HW | AVCC0 | 92 | JA1-5 | J4-17 |
| AVss | HW | AVSS0 | 95 | JA1-6 | J4-20 |
| PLLVss | HW | PLLVss | 31 | – | – |
| EXTAL | HW | EXTAL | 13 | – | J1-13 |
| XTAL | HW | XTAL | 11 | – | J1-11 |
| MD1 | HW | MD1 | 6 | – | J1-6 |
| RESET | HW | RES# | 10 | JA2-1 | J1-10 |
| ASEMD0 | HW | MD0 | 7 | – | J1-7 |
| Fault signal input | IN | POE10#-A | 15 | JA2-3 | J1-15 |
| Motor UP-phase output | OUT | MTIOC3B | 56 | JA2-13 | J3-6 |
| Motor UN-phase output | OUT | MTIOC3D | 53 | JA2-14 | J3-3 |
| Motor VP-phase output | OUT | MTIOC4A | 55 | JA2-15 | J3-5 |
| Motor WP-phase output | OUT | MTIOC4B | 54 | JA2-17 | J3-4 |
| Motor VN-phase output | OUT | MTIOC4C | 52 | JA2-16 | J3-2 |
| Motor WN-phase output | OUT | MTIOC4D | 51 | JA2-18 | J3-1 |
| AD input for bus voltage | IN | AN003 | 88 | JA1-12 | J4-13 |
| AD input for 1-shunt current | IN | AN000 | 91 | JA1-9 | J4-16 |

## 2.2 Timing Diagram

Figure 2 is a diagram showing one carrier of PWM and timing to capture AD values.
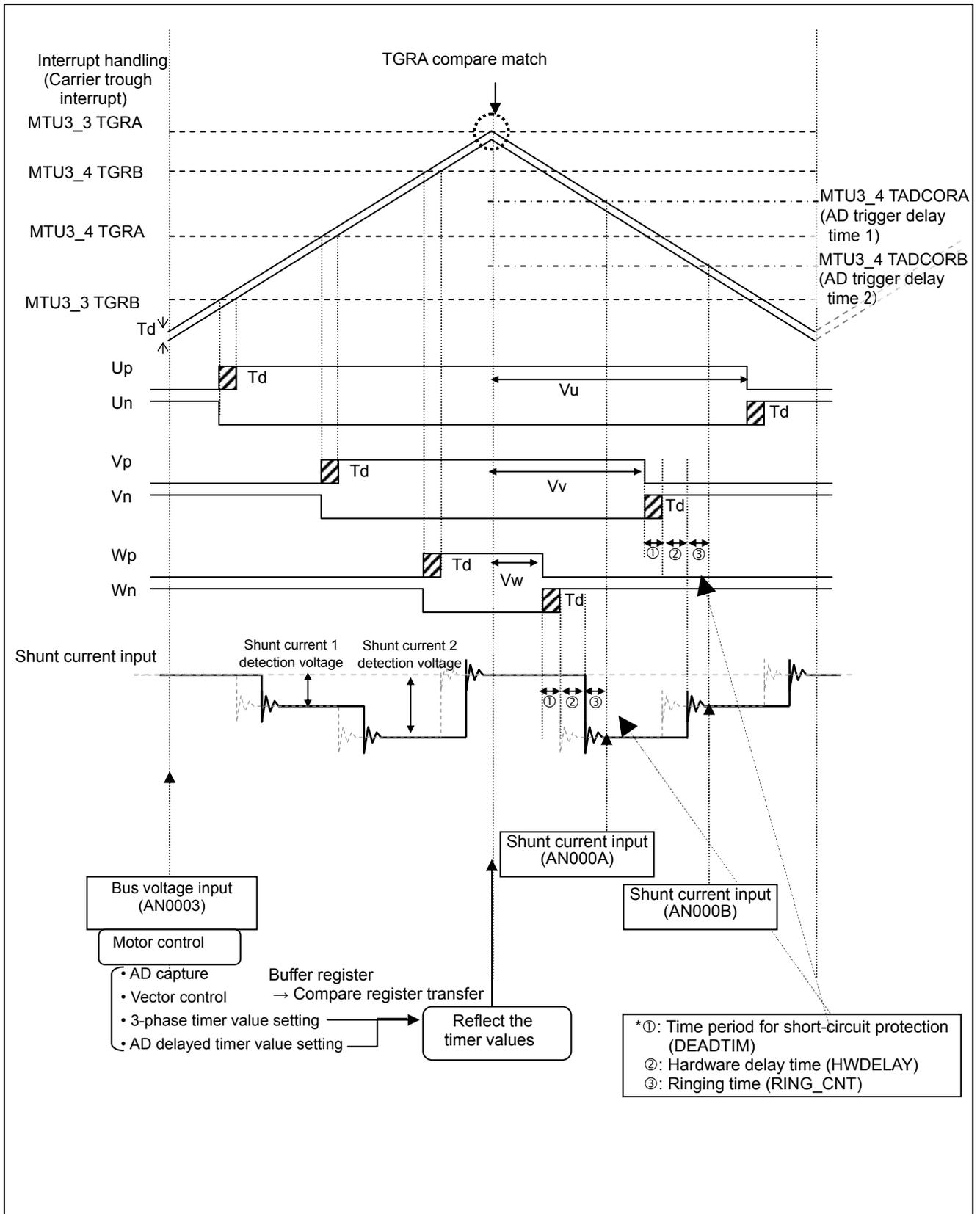


**Figure 2. AD Conversion Timing Diagram**

## 2.3        12-bit AD Converter (S12ADA)

(1)  AD Detection Items

Table 3 lists items detected by the AD conveters.

**Table 3. AD Detection Items**

| Item | A/D input port |
|---|---|
| Shunt current 1 | AN000A |
| Shunt current 2 | AN000B |
| Bus voltage | AN003 |

(2) AD Converter Settings

Table 4 shows settings for the 12-bit AD converters.

**Table 4. AD Conversion Mode Setting**

| Item | Content |
|---|---|
| Conversion mode | 2-channel scan mode |
| Conversion pin | Group 0: AN000A, AN000B<br>Group 1: AN001 to AN003 |
| Trigger select | Group 0: MTU3 TRG4AN or TRG4BN<br>Group 1: MTU3 TRGA4N (carrier trough) |
| Bit select | 12 bits (right aligned) |
| Sampling method | Sample-and-hold function + dedicated sample-and-hold for each channel |
| Frequency select | PCLK = 50MHz, ADCLK = 50MHz |
| A/D conversion time | 1.82μs (4 cycles ÷ PCLK + 88 cycles ÷ ADCLK) |
| A/D conversion interrupt | Unused |
| PGA | Amplification rate: 2 times (AN000A, AN000B) |
| Comparator function select | Window comparator (High: 6/8AVCC, Low: 1/8AVCC) |
| Noise cancellation filter | Comparator detection results are sampled 16 times with PCLK/8 |
| Comparator interrupt | Used as a POE interrupt request |

(3) How to Calculate the AD Conversion Time

To use PGA, it is necessary to use a dedicated sample-and-hold circuit set for each channel of 12-bit AD converters (excluding AN003 and AN103).

The AD conversion time can be calculated by a below formula which is described in Section 27.3.3, p.1225 in RX62T Group Hardwar Manual Rev1.10 .

• When a dedicated sample-and-hold circuit for the channel is used and self diagnosis function is not used:
$tSCAN = tD + tSPLSH + (tCONV \times n) + tED$
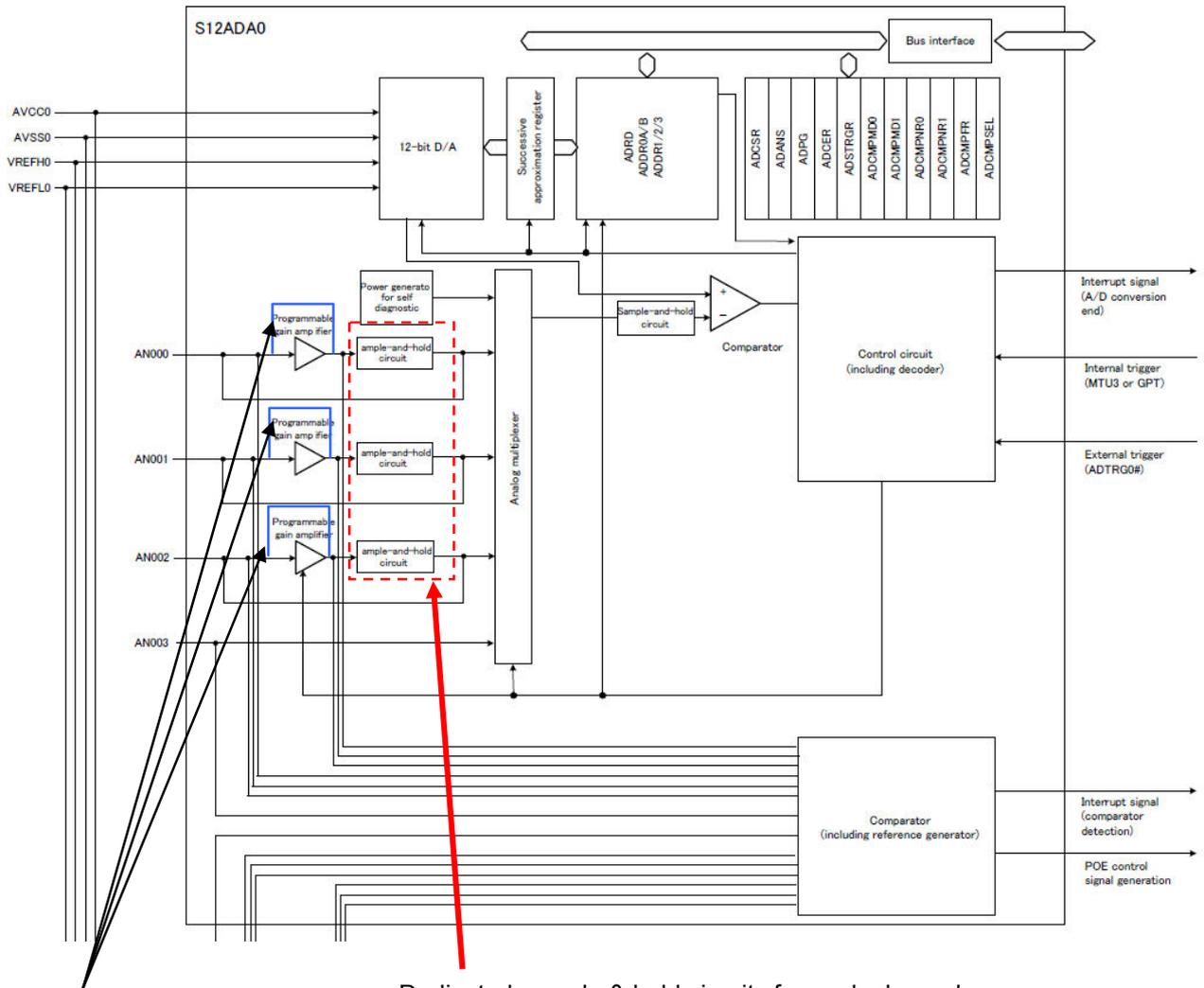
**Figure 3. Excerpt from AD Converter Block Diagram**

## 2.4　　Port Output Enable 3 (POE3)

(1) Item Detected by Port Output Enable 3

Table 5 shows an item detected by Port Output Enable 3.

**Table 5.  Item Detected by Port Output Enable 3**

| Item | Port | Content |
|---|---|---|
| Fault signal input | POE10 | Detect a fault signal from IPM |

(2) Settings for Port Output Enable 3

Table 6 shows settings for POE3.

**Table 6. Settings for POE3**

| Item | Content |
|---|---|
| Target | Three-phase output ports (6 pins) |
| High-impedance conditions | • Comparator detection (AN000)<br>• POE10 input level detection<br>• When upper and lower arms in any phase of the three-phase PWM outputs have simultaneously reached an active level |
| Interrupt | POE10: priority level 15 |
| Interrupt source | A request is accepted at the falling edge of POE10 pin. |

## 2.5　　Multi-Function Timer Unit 3 (MTU3)

(1) Settings for the multi-function timer unit 3

Table 7 shows settings for the multi-function timer unit 3.

**Table 7. Setting Items in Multi-Function Timer Unit 3**

| Item | Content |
|---|---|
| Used channel | MTU3 ch3, 4 |
| Operating mode | Complementary PWM mode |
| Frequency select | ICLK = 100MHz |
| Dead time | 2μs |
| Buffer transfer timing | Buffer transfer at counter trough |
| Interrupt skipping | None |
| Interrupt | Interrupts at MTU3_4 underflow (priority level 10) |

## 3    PDG2 Setting

Sample S/W registers for this application note are generated and set by using PDG2. This chapter illustrates settings to configure an operation environment in user system by using PDG2.

*Note
The sample S/W is adjusted to operate on a PC in which PDG2 has not been installed. Therefore, settings according to displays shown below do not mean that a project built on the High-performance Embedded Workshop (HEW) has the same configuration as the sample S/W.
There is no difference in operations.

## 3.1    System Setting
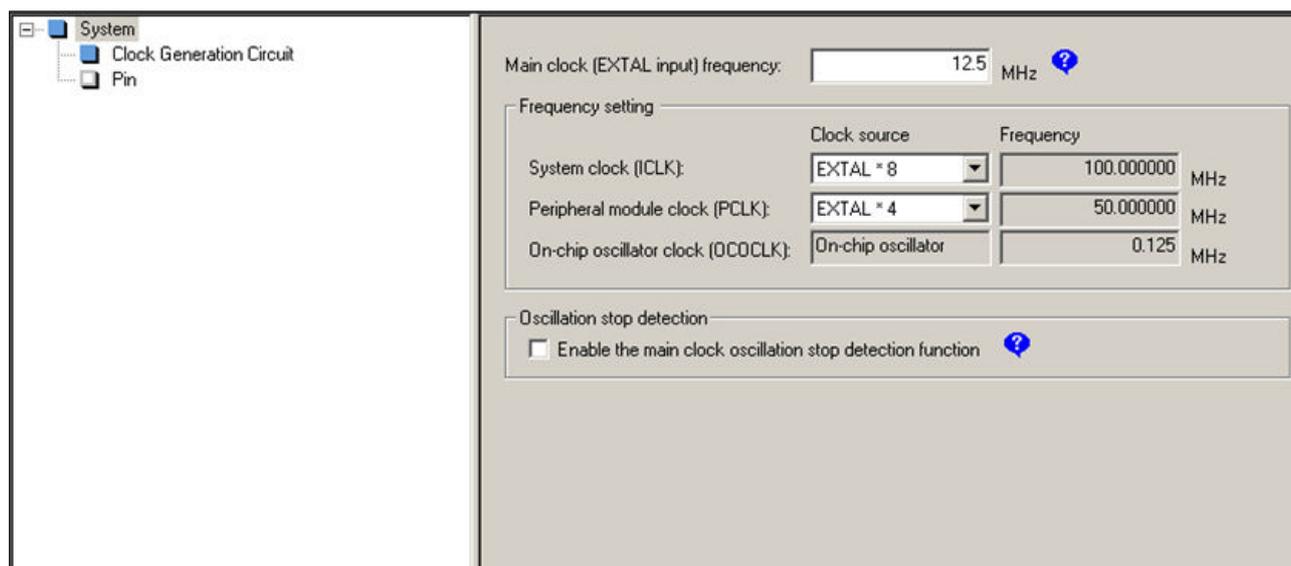


Figure 4. System Setting Display

### 3.2    MTU3ch3 Setting

When the complementary PWM mode is selected as operation mode for MTU3ch3, ch4 is automatically set in accordance with ch3 setting.
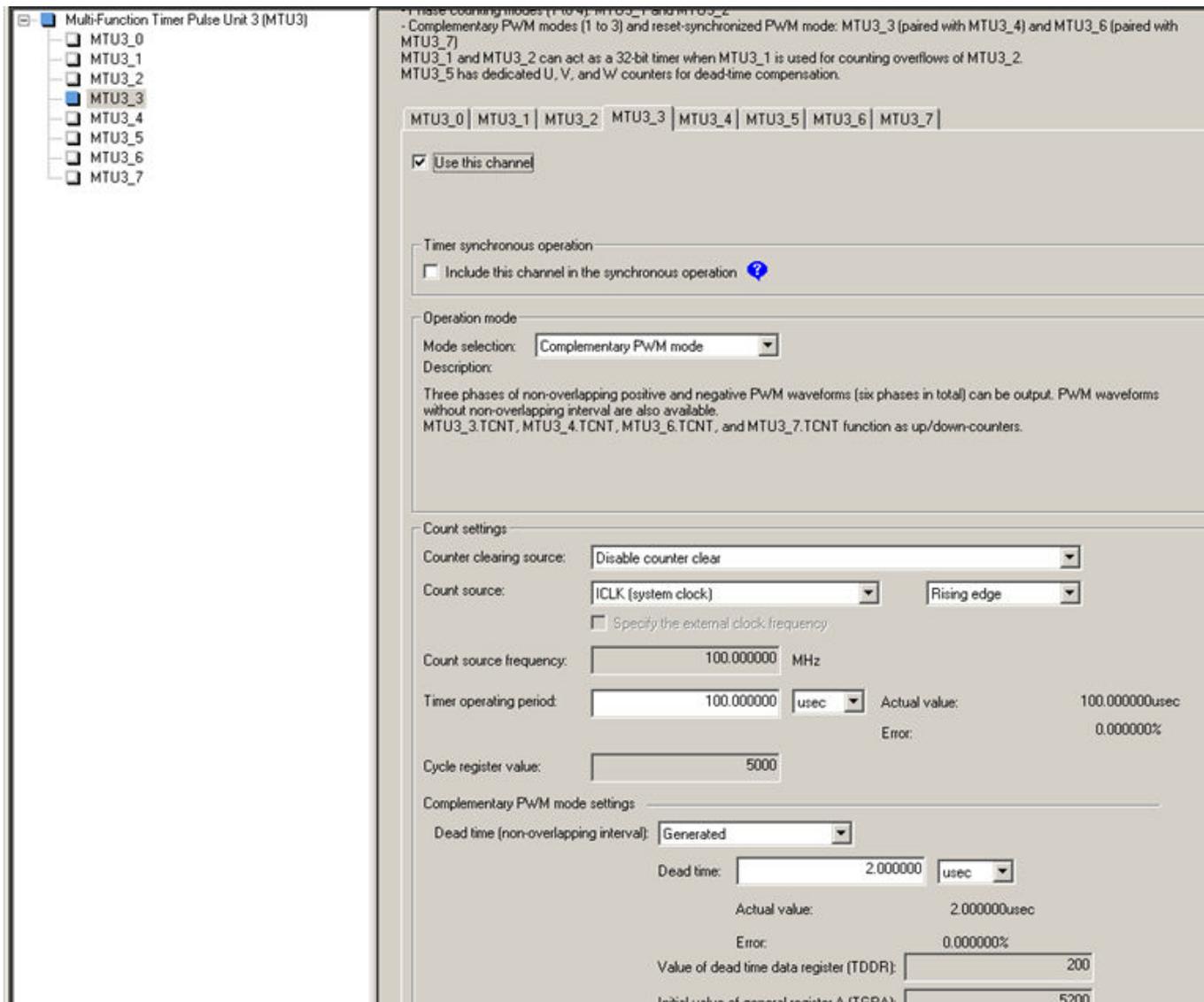


Figure 5. MTU3 Setting Display 1

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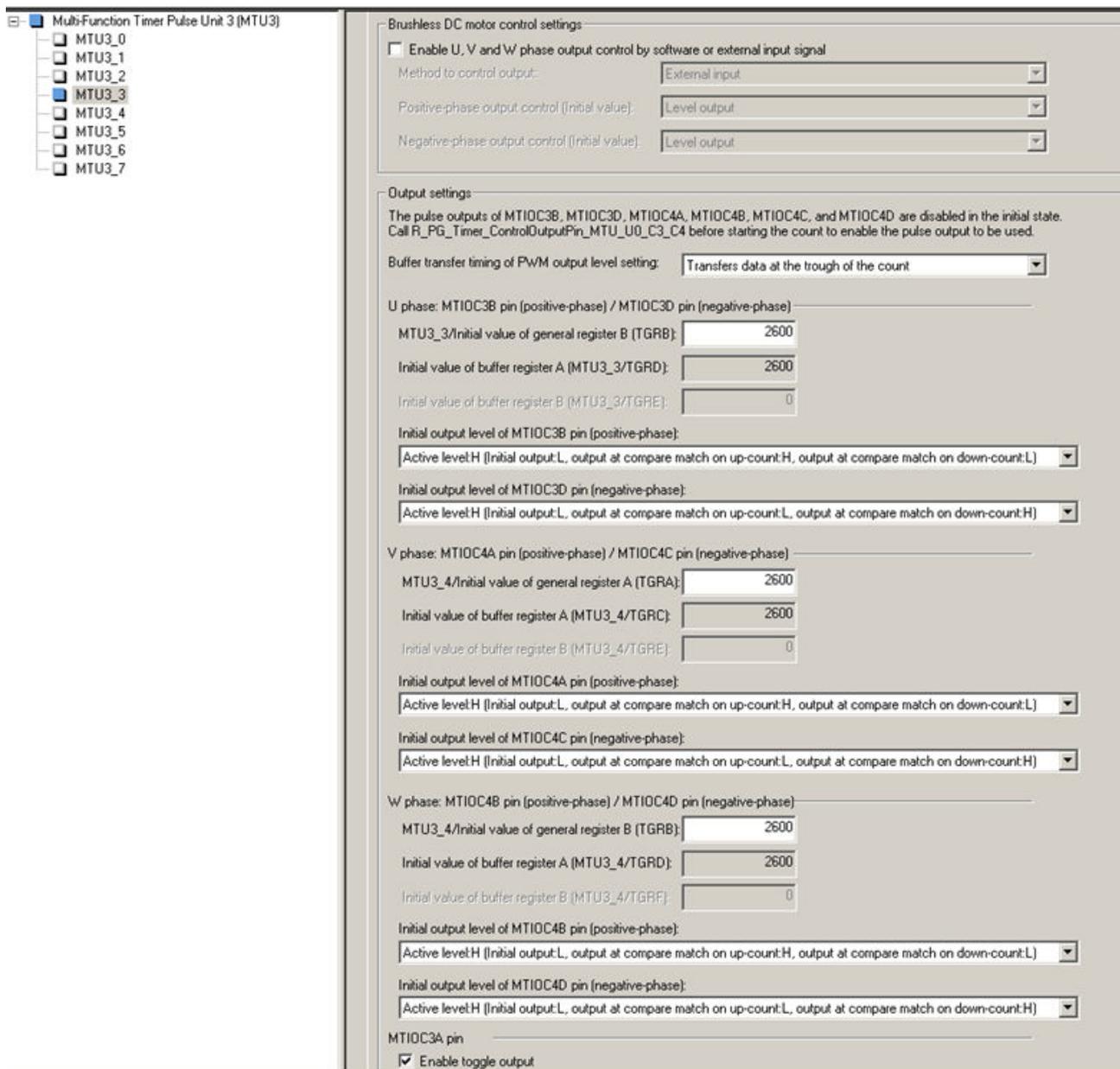
Figure 6. MTU3 Setting Display 2
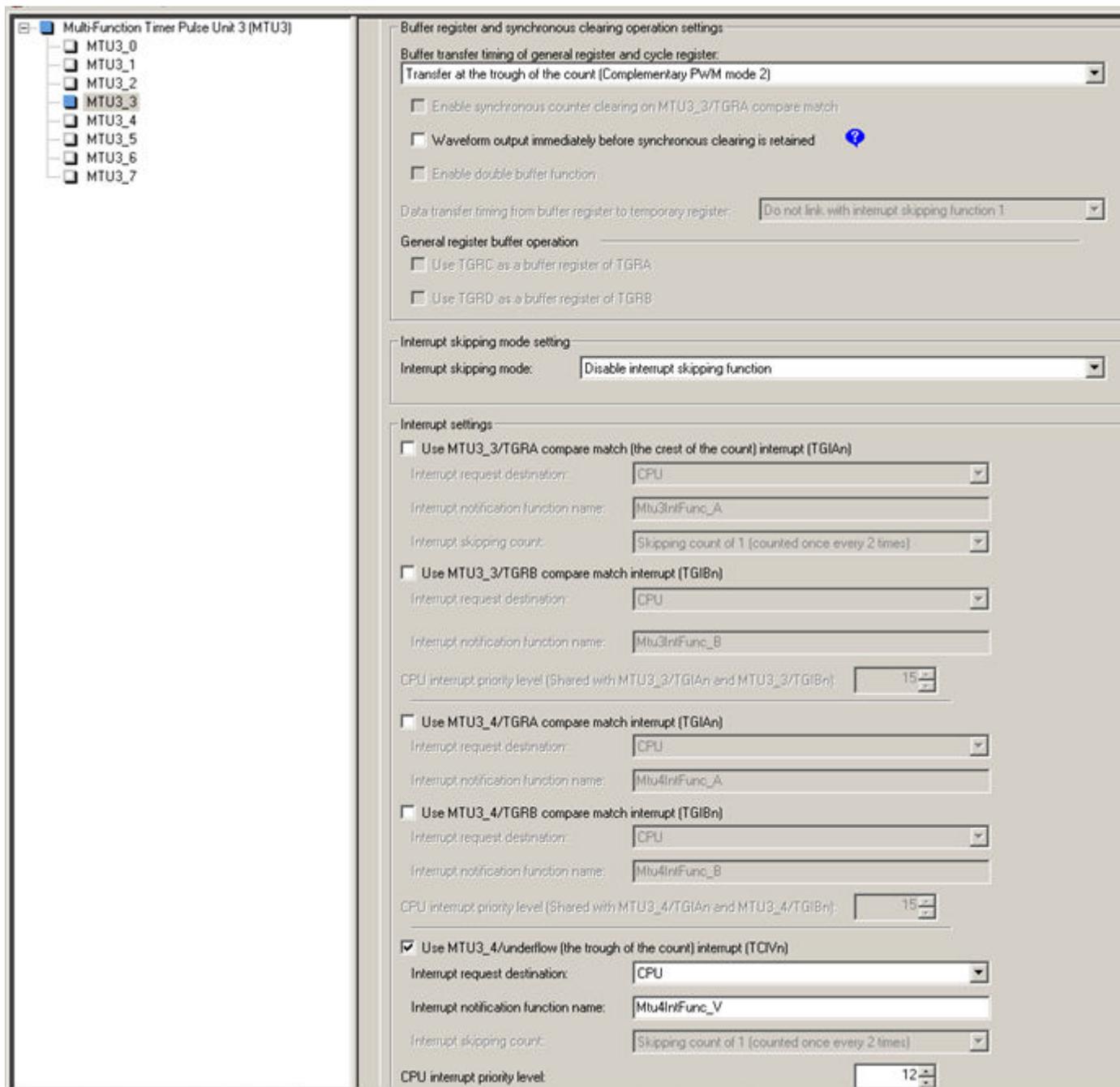
Figure 7. MTU3 Setting Display 3
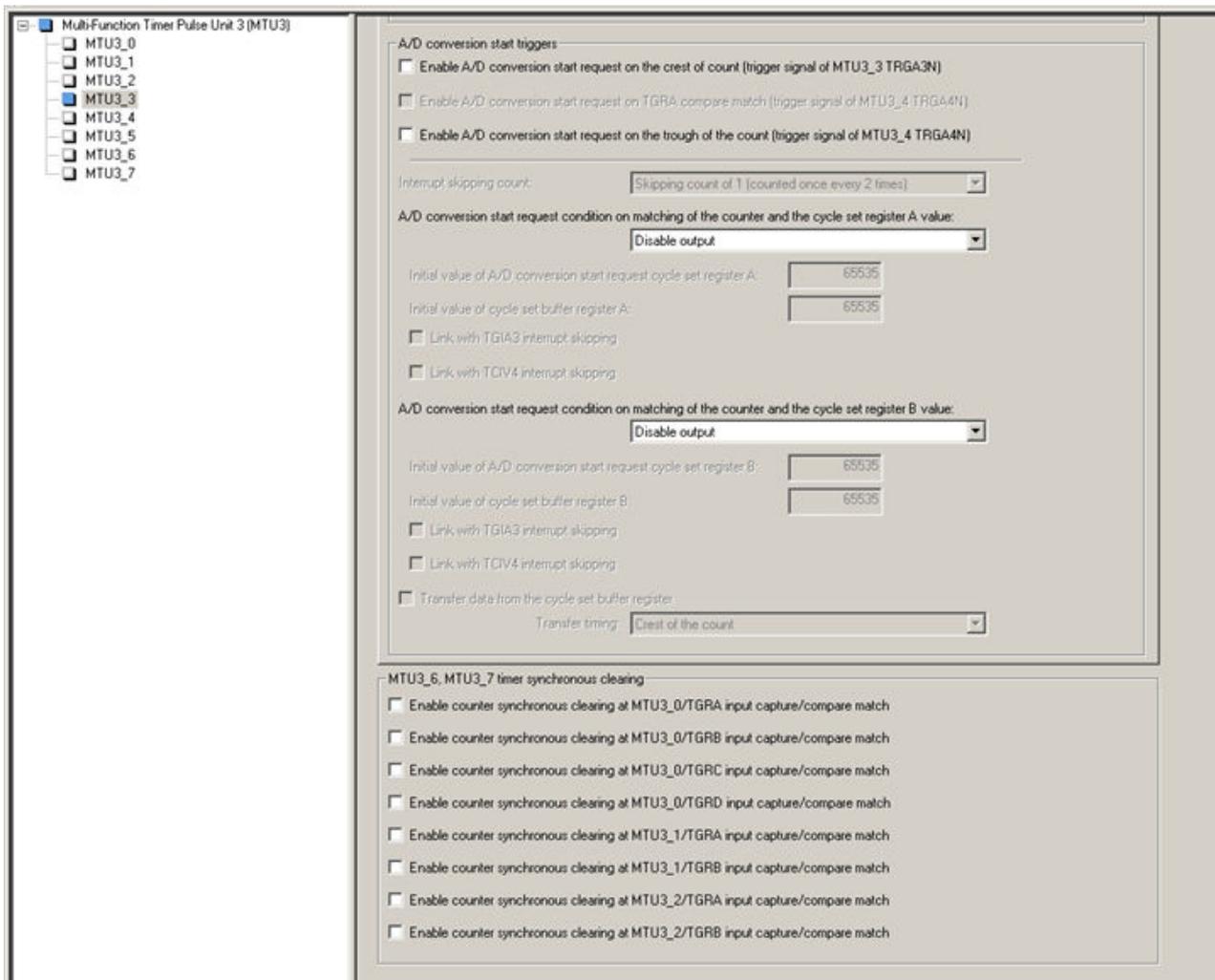
Figure 8. MTU3 Setting Display 4

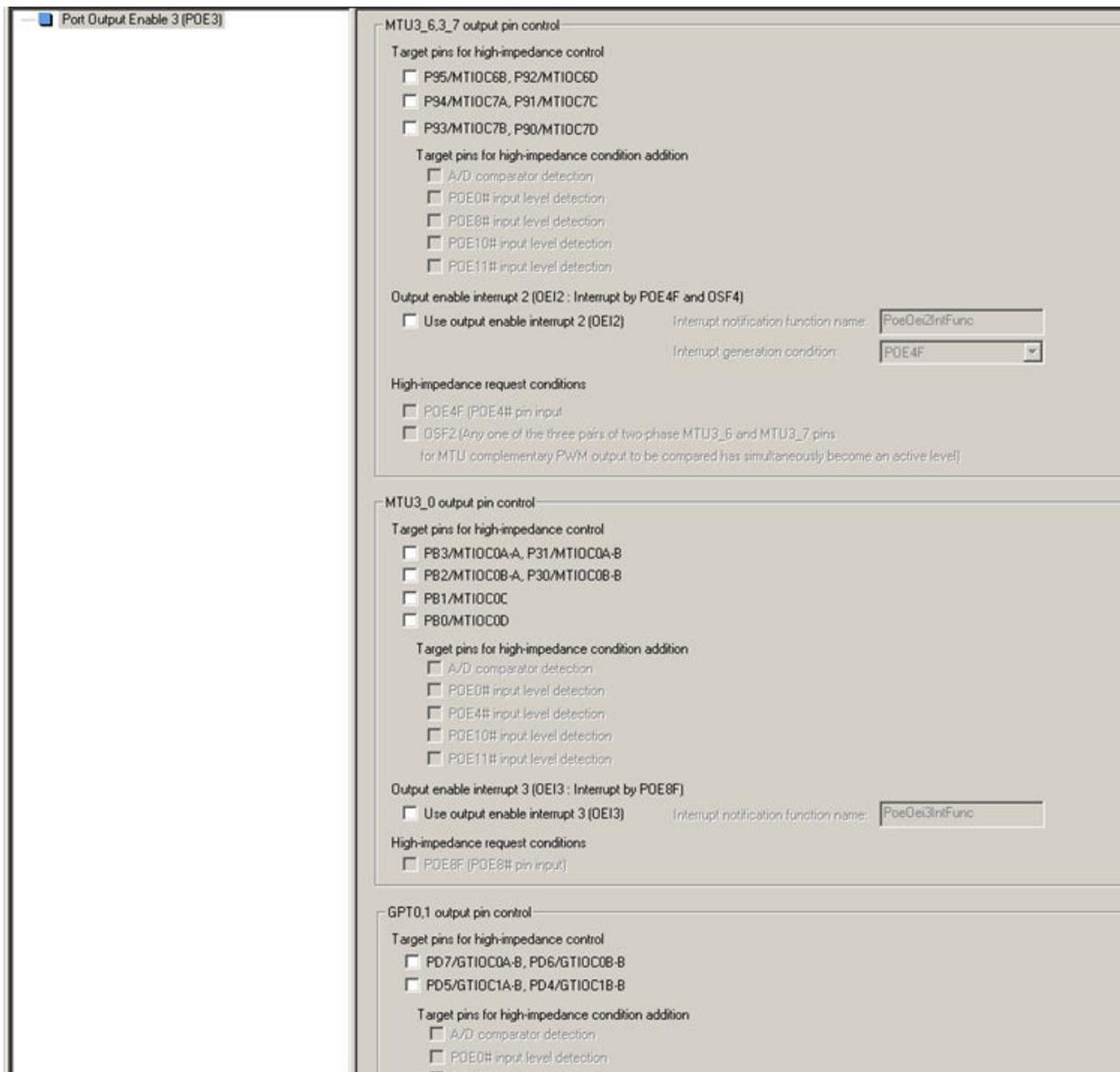### 3.3     POE3 Setting
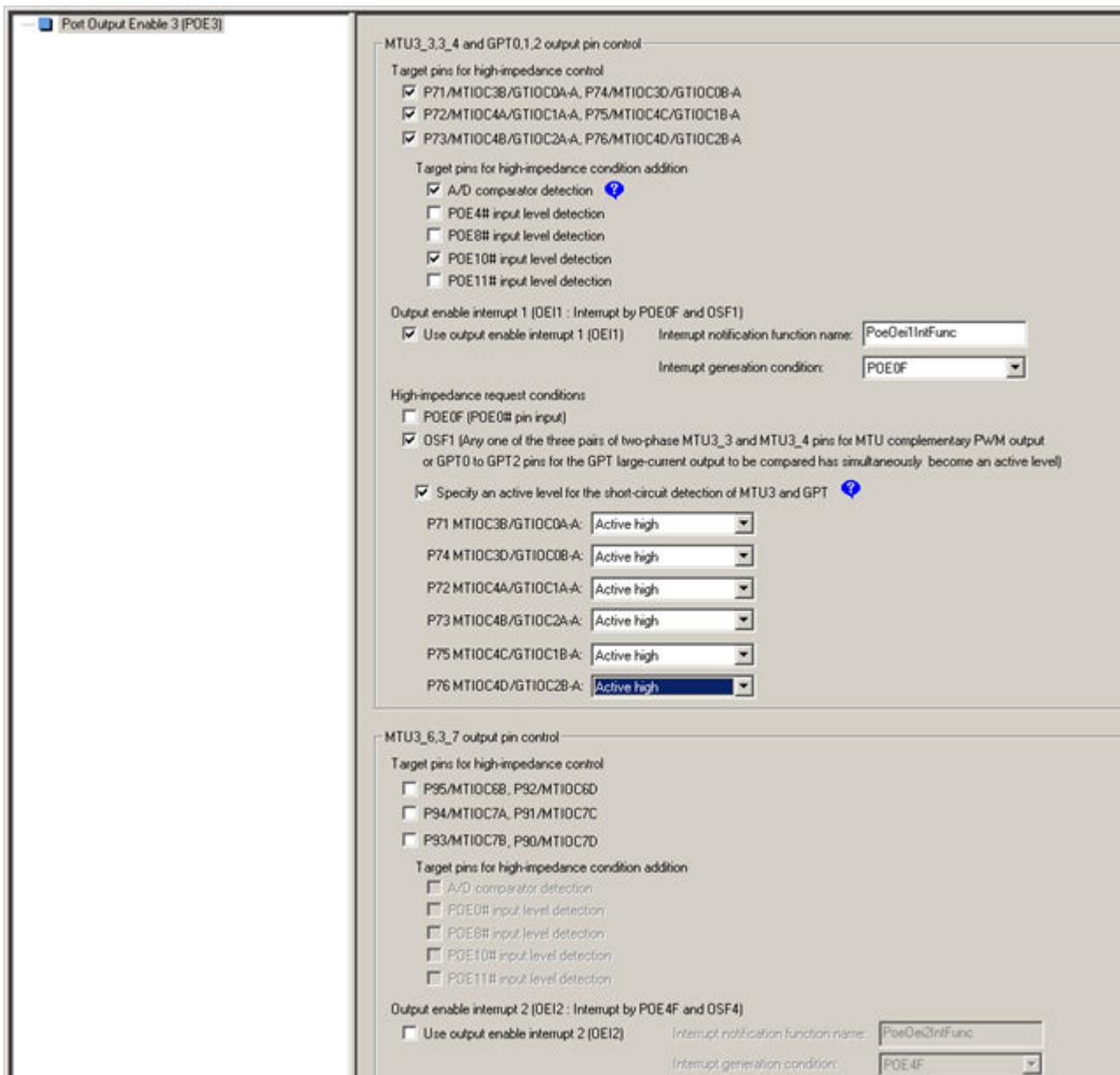


Figure 9. POE3 Setting Display 1

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Figure 10. POE3 Setting Display 2
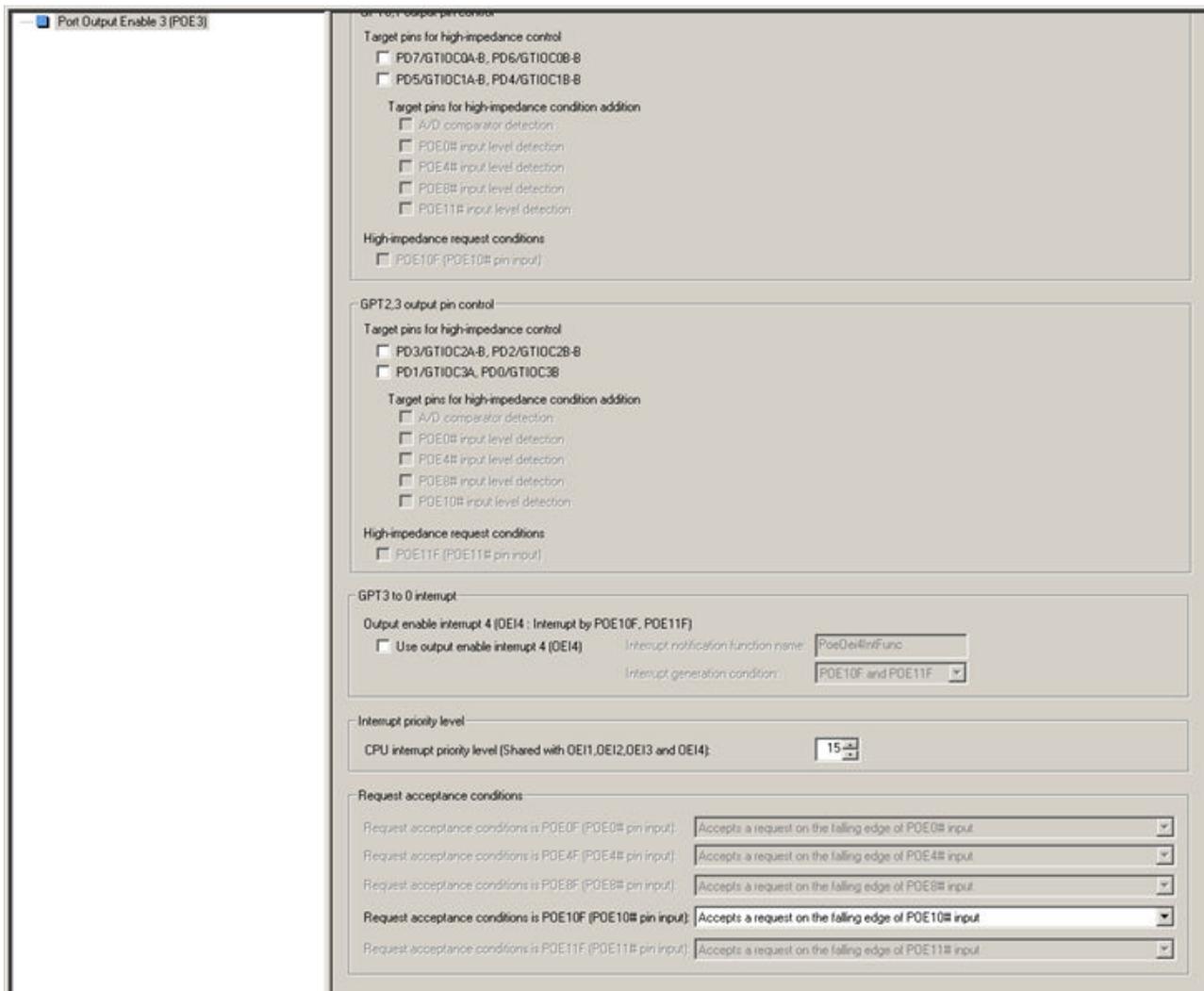
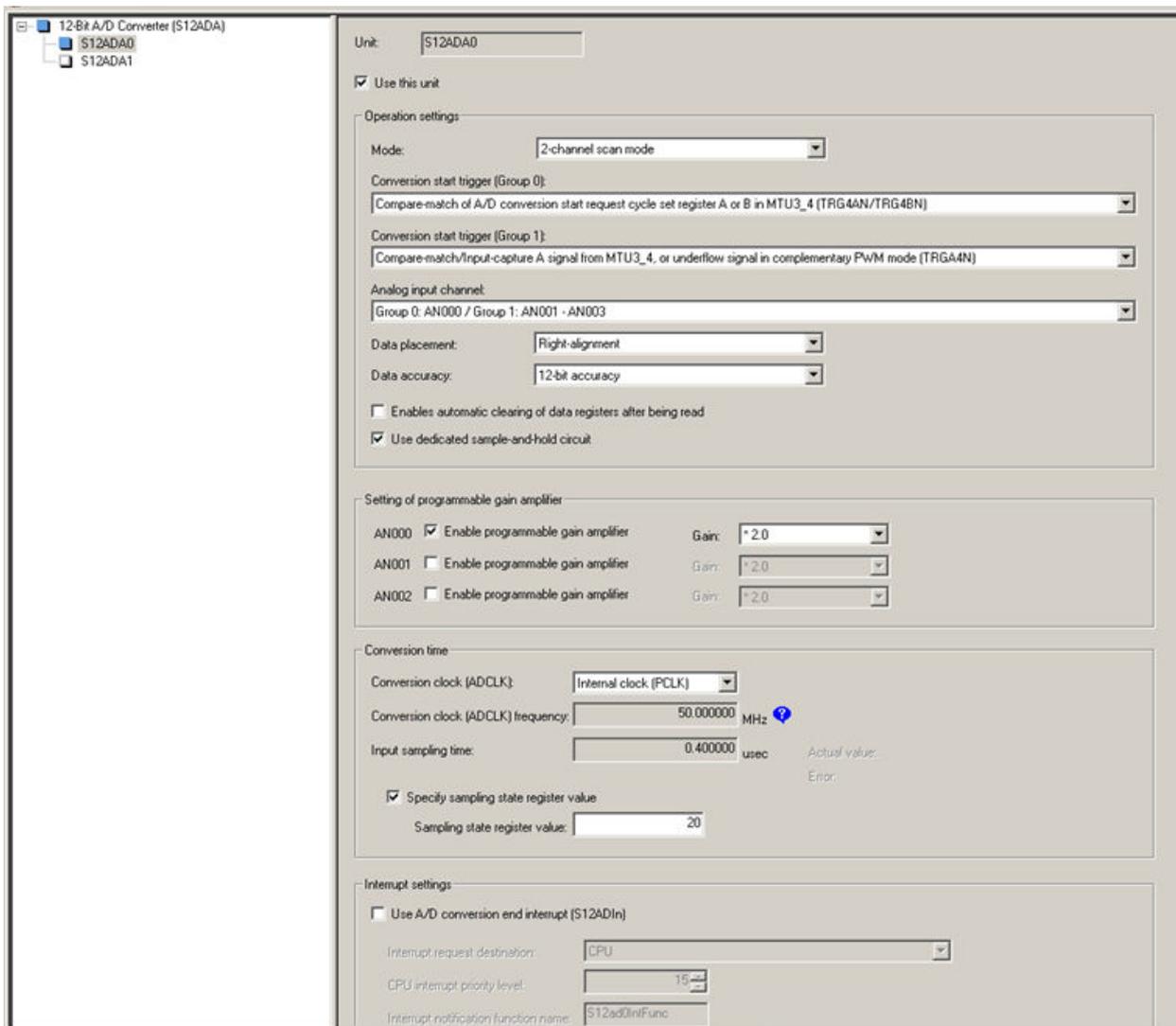Figure 11. POE3 Setting Display 3

## 3.4      12-Bit ADA Setting



Figure 12. 12-Bit AD Setting Display

## 4    S/W Descriptions

This chapter describes settings of modules which are not supported by PDG2 and control flows.

### 4.1    Register Settings

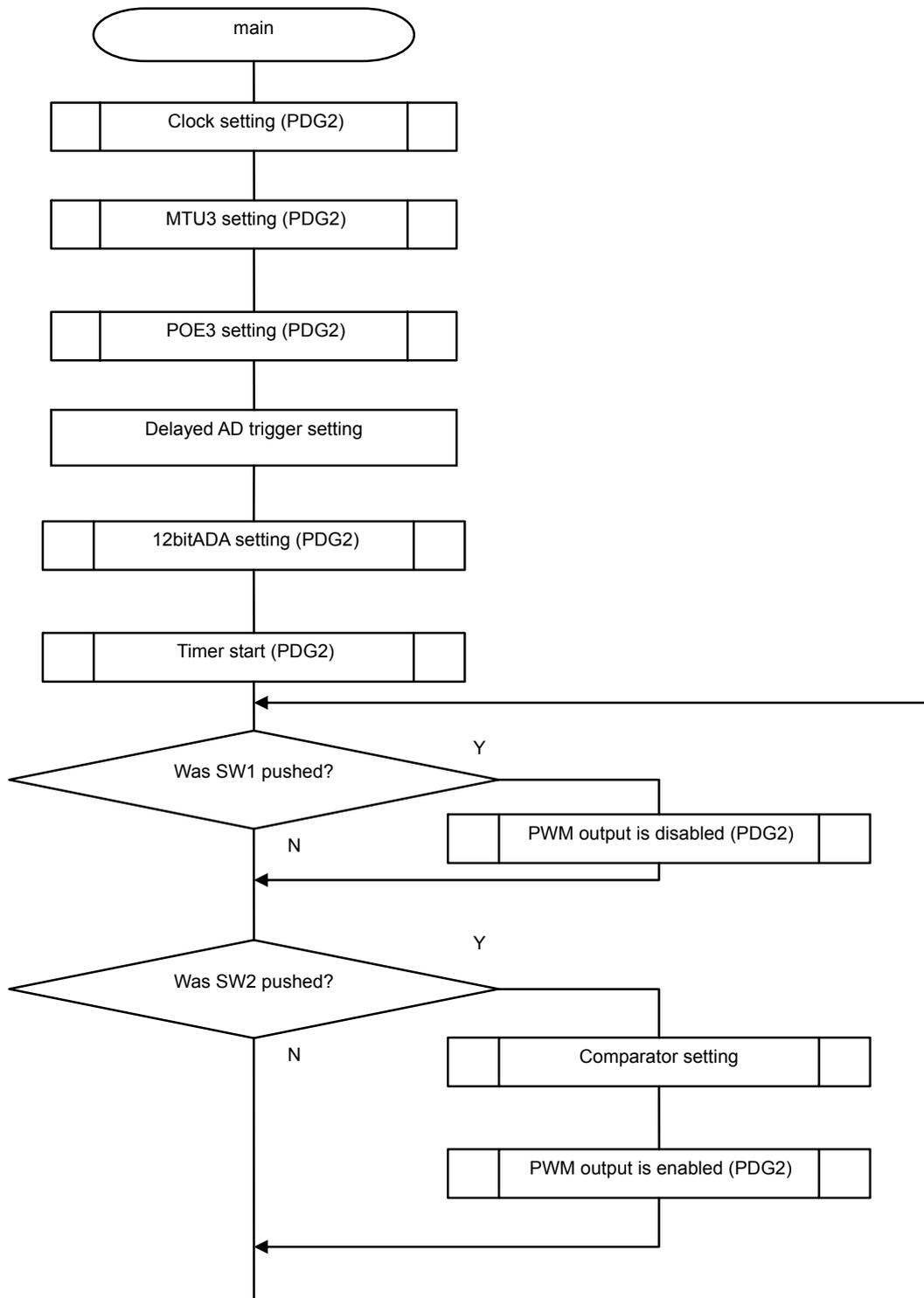| Register | Initial value | Content |
|---|---|---|
| MTU4.TIER.BIT.TTGE | 1 | Enable to generate an AD conversion start request |
| MTU4.TIER.BIT.TTGE2 | 1 | Enable an AD conversion request at trough |
| MTU4.TADCOBRA | 5200 | Set a cycle for  AD conversion start request (buffer) |
| MTU4.TADCOBRB | 5200 | Set a cycle for  AD conversion start request (buffer) |
| MTU4.TADCORA | 5200 | Set a cycle for  AD conversion start request |
| MTU4.TADCORB | 5200 | Set a cycle for  AD conversion start request |
| MTU4.TADCR.WORD | 0x4050 | Buffer transfer at TCNT4 peak<br>As for TRG4AN and TRG4BN, AD converter start requests are enabled when TCNT4 decrements.<br>Not  link the transfer with interrupt skipping function |
| S12AD.ADCMPFR.BIT.C000FLAG | 0 | Clear the comparator detection flag for AN000 |
| S12AD.ADCMPMD0.BIT.CEN000 | 3 | Use AN000 as the window comparator (Low/High) |
| S12AD.ADCMPMD1.WORD | 0x0661 | REFL: AVCC0 × 1/8, REFH: AVCC0 × 6/8<br>Use a signal before amplified by the PGA as a comparator input with reference to REFH/REFL |
| S12AD.ADCMPNR0.BIT.C000NR | 10 | Sample the comparator result 16 times at PCLK/2 |
| S12AD.ADCMPSEL.WORD | 0x0301 | Use the  detection in the comparator  as an interrupt or POE request |
| POE.POECR4.BIT.CMADDMT34ZE | 1 | Add the S12ADA.ADCMPFR.CjFLAG (j = 0 to 2 and 4 to 6) flag to high-impedance conditions of MTU3_3 and MTU3_4 |
| IR (S12AD,CMPI) | 0 | Clear the interrupt request flag (comparator IR) |
| IPR (S12AD,CMPI) | 0x0c | Comparator interrupt priority level = 12 |
| IEN (S12AD,CMPI) | 1 | Enable comparator interrupts |
| POE.ICSR4.BIT.POE10F | 0 | Clear the POE10 interrupt request flag |
| POE.OCSR1.BIT.OSF1 | 0 | Clear the output short flag |

### 4.2    Settings of Variables

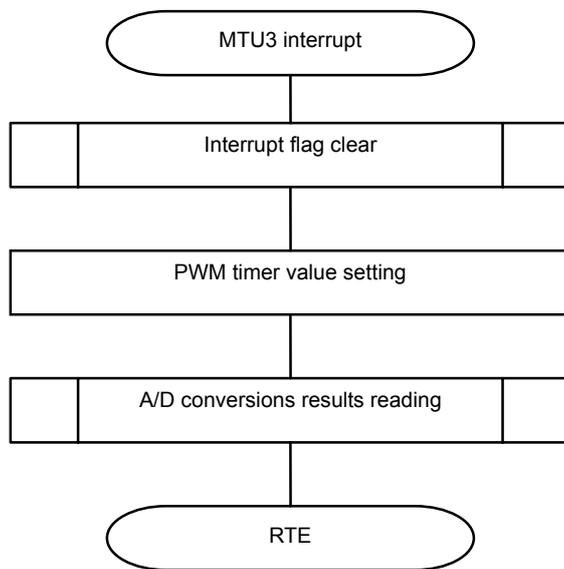| Defined name | (Type) Initial value | Content |
|---|---|---|
| du | (float) 0 | Variable to store the U-phase output value |
| dv | (float) 5200 / 3 | Variable to store the V-phase output value |
| dw | (float) 5200 / 3 × 2 | Variable to store the W-phase output value |
| AD_data [5] | (short) 0 | Variable to store the AD conversion result (For details, refer to the section about 12-bit A/D converter in PDG2 reference manual.) |
| t_c1 | (int) 0 | Counter to prevent chattering (for SW1) |
| t_c2 | (int) 0 | Counter to prevent chattering (for SW2) |

### 4.3    Settings of Constants

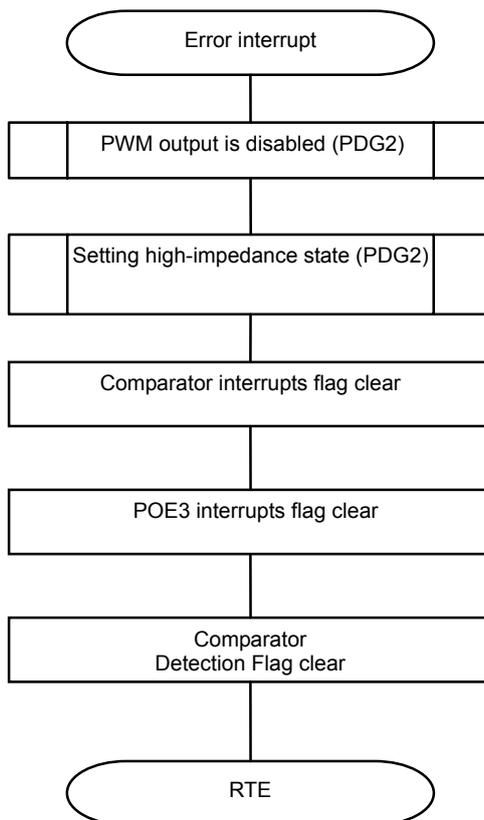| Defined name | Value | Content |
|---|---|---|
| CARR_CNT | 10000 | Carrier cycle |
| DTT_CNT | 200 | Dead time |
| CMP_TIMING_1 | 5 | Constant to generate a timing for AD conversion start trigger |
| CMP_TIMING_2 | 15 | Constant to generate a timing for AD conversion start trigger |
| PWM_CHANGE_VAL | 0.1 | Constant to control changes in PWM output |

## 4.4     Main Function Flow

```
                    ┌──────────────────────┐
                    │         main         │
                    └──────────────────────┘
                               │
            ┌──────┬──────────────────────┬──────┐
            │      │  Clock setting (PDG2) │      │
            └──────┴──────────────────────┴──────┘
                               │
            ┌──────┬──────────────────────┬──────┐
            │      │  MTU3 setting (PDG2)  │      │
            └──────┴──────────────────────┴──────┘
                               │
            ┌──────┬──────────────────────┬──────┐
            │      │  POE3 setting (PDG2)  │      │
            └──────┴──────────────────────┴──────┘
                               │
            ┌──────────────────────────────────┐
            │     Delayed AD trigger setting    │
            └──────────────────────────────────┘
                               │
            ┌──────┬──────────────────────┬──────┐
            │      │ 12bitADA setting (PDG2)│     │
            └──────┴──────────────────────┴──────┘
                               │
            ┌──────┬──────────────────────┬──────┐
            │      │   Timer start (PDG2)  │      │
            └──────┴──────────────────────┴──────┘
                               │
                         <Was SW1 pushed?>──── Y ──┐
                               │ N                  │
                               │        ┌──────┬──────────────────────┬──────┐
                               │        │      │ PWM output is disabled (PDG2)│   │
                               │◄───────┴──────┴──────────────────────┴──────┘
                               │
                         <Was SW2 pushed?>──── Y ──┐
                               │ N                  │
                               │        ┌──────┬──────────────────────┬──────┐
                               │        │      │   Comparator setting  │      │
                               │        └──────┴──────────────────────┴──────┘
                               │                    │
                               │        ┌──────┬──────────────────────┬──────┐
                               │        │      │ PWM output is enabled (PDG2) │   │
                               │◄───────┴──────┴──────────────────────┴──────┘
                               │
                               └───────────────────────────────────────────►
```

## 4.5     MTU3 Interrupt Flow

```
┌──────────────────────────────┐
│        MTU3 interrupt         │
└──────────────────────────────┘
                │
┌──┬──────────────────────────┬──┐
│  │     Interrupt flag clear     │  │
└──┴──────────────────────────┴──┘
                │
┌──────────────────────────────┐
│     PWM timer value setting      │
└──────────────────────────────┘
                │
┌──┬──────────────────────────┬──┐
│  │  A/D conversions results reading  │  │
└──┴──────────────────────────┴──┘
                │
┌──────────────────────────────┐
│              RTE               │
└──────────────────────────────┘
```

## 4.6     Error Interrupt Flow

```
┌──────────────────────────────┐
│        Error interrupt        │
└──────────────────────────────┘
                │
┌──┬──────────────────────────┬──┐
│  │  PWM output is disabled (PDG2)  │  │
└──┴──────────────────────────┴──┘
                │
┌──┬──────────────────────────┬──┐
│  │ Setting high-impedance state (PDG2) │  │
└──┴──────────────────────────┴──┘
                │
┌──────────────────────────────┐
│  Comparator interrupts flag clear  │
└──────────────────────────────┘
                │
┌──────────────────────────────┐
│    POE3 interrupts flag clear    │
└──────────────────────────────┘
                │
┌──────────────────────────────┐
│          Comparator           │
│      Detection Flag clear      │
└──────────────────────────────┘
                │
┌──────────────────────────────┐
│              RTE               │
└──────────────────────────────┘
```

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  http://www.renesas.com/

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## Revision Record

| Rev. | Date | Description | |
|---|---|---|---|
| | | **Page** | **Summary** |
| 1.00 | 2012.02.17 | — | First edition issued |
| | | | |
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## General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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