RX610 Group, RX630 Group

Differences between RX610 Group and RX630 Group

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Abstract

This application note provides reference information on the differences between RX610 Group and RX630 Group microcontrollers.

Products

RX610 Group, RX630 Group

Contents

1. Switching from the RX610 Group to the RX630 Group 3
1.1 Newly Added Functions 3
1.2 Eliminated Functions 3
1.3 Modified Functions 4
1.3.1 Modification Type 1: Items Requiring Reconsideration Due to Specification Changes or Elimination of Functions 4
1.3.2 Modification Type 2: Items Requiring Reconsideration of Error Handling Due to Changes to the Interrupt Controller 4
1.3.3 Modification Type 3: Items Requiring Reconsideration of Software Due to Partial Changes to Functions 4
1.4 Compatible Functions 4
1.4.1 Compatible Functions 4
1.4.2 Backward-Compatible Function 4

2. Description of Differences 5
2.1 Differences in Functions and Specifications 5

3. Reference Documents 36

1. Switching from the RX610 Group to the RX630 Group

The RX610 Group and RX630 Group are not interchangeable devices. Therefore, care must be exercised when switching to the RX630 Group. For details, see section 2., Description of Differences, as well as RX610 Group—User's Manual: Hardware and RX630 Group—User's Manual: Hardware.

1.1 Newly Added Functions

(1) Power-on reset (POR) circuit
(2) Software reset
(3) Cold start/warm start determination function
(4) Option-setting memory
(5) Voltage detection circuit (LVDA)
(6) Low-speed on-chip oscillator (LOCO), high-speed on-chip oscillator (HOCO)
(7) Frequency measurement circuit (MCK)
(8) Battery backup function
(9) Register write protection function
(10) Memory-protection unit (MPU)
(11) Multi-function pin controller (MPC)
(12) Multi-function timer pulse unit 2 (MTU2a)
(13) Port output enable 2 (POE2a)
(14) Realtime clock (RTCa)
(15) Independent watchdog timer (IWDTa)
(16) USB 2.0 function module (USBa)
(17) Serial peripheral interface (RSPI)
(18) IEBus controller (IEB)
(19) 12-bit A/D converter (S12ADa)
(20) Temperature sensor

1.2 Eliminated Functions

(1) MD1 pin (mode 1 pin), MDE pin (endian selection pin)
(2) MD1 pin and MDE pin status flags (MD1 and MDE in MDMONR)
(3) On-chip ROM startup status flag (IROM in MDSR), etc.
(4) Reset control/status register (RSTCSR)
(5) Standby timer select bits (STS4 to STS0 in SBYCR)
(6) Deep standby wait control register (DPSWCR)
(7) Interrupt request destination setting register i (ISELRi) (i = interrupt vector number)
(8) IRQ detection enable register n (IRQERn) (n = 0 to 15)
(9) Software standby release IRQ enable register (SSIER)

1.3 Modified Functions

1.3.1 Modification Type 1: Items Requiring Reconsideration Due to Specification Changes or Elimination of Functions

(1) MCU operation mode entry methods: MD pin eliminated, UB codes A and B added.
(2) Endian determination method: Bits MDE2 to MDE0 in MDEB and MDES
(3) Clock oscillator circuit: Low-speed on-chip oscillator (LOCO) startup, PLL frequency division, and oscillation stop detection added, etc.
(4) Low power consumption functions: Oscillation settling time modified, etc.
(5) Interrupt controller (ICUb): Interrupt priority level (max.): 7 → 15, group interrupts, unit selection, etc.
(6) Buses: Address/data multiplex bus, peripheral bus update bus priority added, etc.
(7) DMA controller (DMACA): Operand and transfer methods modified, etc.
(8) Data transfer controller (DTCa): Bus priority modified, change transfer after repeat transfer eliminated.
(9) I/O ports: Modifications to multi-function pin controller, etc.
(10) Watchdog timer (WDTA): 8-bit → 14-bit
(11) 10-bit A/D converter (ADb): 4 channels × 4 units → (8 channels × 1 unit) × 1 extended channel
(12) ROM (flash memory for code storage): Write units modified, etc.
(13) Data flash (flash memory for data storage): Block and write units modified.
(14) Boundary scan: Command structure and ID codes modified.

1.3.2 Modification Type 2: Items Requiring Reconsideration of Error Handling Due to Changes to the Interrupt Controller

(1) Serial communications interfaces (SCIc and SCId): 7 channels → 13 channels, functions added, etc.

1.3.3 Modification Type 3: Items Requiring Reconsideration of Software Due to Partial Changes to Functions

(1) Programmable pulse generator (PPG): Trigger sources modified.

1.4 Compatible Functions

1.4.1 Compatible Functions

(1) 8-bit timer (TMR)
(2) Compare match timer (CMT)
(3) CRC calculator (CRC)

1.4.2 Backward-Compatible Function

(1) D/A converter (DAa): D/A and A/D conversion synchronous start function added.

2. Description of Differences

2.1 Differences in Functions and Specifications

Tables 2.1 to 2.31 list the differences in functions and specifications.

Table 2.1 Differences in Functions and Specifications (1)

<table>
<tr><th colspan="2">Item</th><th>RX610 Group</th><th>RX630 Group</th></tr>
<tr><td>Memory</td><td>ROM/RAM</td><td>• Memory configurations
<table><tr><td>ROM/RAM capacity</td><td>—</td></tr><tr><td></td><td>—</td></tr><tr><td></td><td>768 KB / 128 KB</td></tr><tr><td></td><td>1.0 MB / 128 KB</td></tr><tr><td></td><td>1.5 MB / 128 KB</td></tr><tr><td></td><td>2.0 MB / 128 KB</td></tr></table></td><td>• Memory configurations
<table><tr><td>ROM/RAM capacity</td><td>384 KB / 64 KB</td></tr><tr><td></td><td>512 KB / 64 KB</td></tr><tr><td></td><td>768 KB / 96 KB</td></tr><tr><td></td><td>1.0 MB / 96 KB</td></tr><tr><td></td><td>1.5 MB / 128 KB</td></tr><tr><td></td><td>2.0 MB / 128 KB</td></tr></table></td></tr>
<tr><td rowspan="3">MCU operating modes</td><td rowspan="3">Operating modes</td><td>• Mode entry
<table><tr><th>MD1</th><th>MD0</th><th>Operating mode</th></tr><tr><td>0</td><td>1</td><td>Boot mode</td></tr><tr><td>1</td><td>0</td><td>—</td></tr><tr><td></td><td></td><td>User boot mode</td></tr><tr><td>1</td><td>1</td><td>Single-chip mode</td></tr></table></td><td>• Mode entry
<table><tr><th>PC7</th><th>MD</th><th>UB code A</th><th>Operating mode</th></tr><tr><td>Low</td><td>Low</td><td>—</td><td>Boot mode</td></tr><tr><td>High</td><td>Low</td><td>—</td><td>USB boot mode</td></tr><tr><td></td><td></td><td>to 426F6F74h</td><td>User boot mode</td></tr><tr><td>—</td><td>High</td><td>—</td><td>Single-chip mode</td></tr></table></td></tr>
<tr><td>• Endian selection
• MDE pin
MDE pin = Low: Little-endian
MDE pin = High: Big-endian</td><td>• Endian selection
• MDEB.MDE[2:0] or MDES.MDE[2:0]
MDE[2:0] = 111b: Little-endian
MDE[2:0] = 000b: Big-endian</td></tr>
<tr><td>Registers/ bits</td><td>• Mode monitor register (MDMONR)
<table><tr><td>b0</td><td>MD0</td><td>MD0 pin status flag</td></tr><tr><td>b1</td><td>MD1</td><td>MD1 pin status flag</td></tr><tr><td>b7</td><td>MDE</td><td>MDE pin status flag</td></tr></table>• Mode status register (MDSR)
<table><tr><td>b0</td><td>IROM</td><td>On-chip ROM startup status flag</td></tr><tr><td>b1</td><td>EXB</td><td>External bus startup status flag</td></tr><tr><td>b2
b3</td><td>BSW[1:0]</td><td>External bus width flags</td></tr><tr><td>b4</td><td>BOTS</td><td>Boot mode startup flag</td></tr><tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b6</td><td>UBTS</td><td>User boot mode startup flag</td></tr></table></td><td>• Mode monitor register (MDMONR)
<table><tr><td>b0</td><td>MD</td><td>MD pin status flag</td></tr><tr><td>b1</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b7</td><td>—</td><td>(Reserved bit)</td></tr></table>• Mode status register (MDSR)
<table><tr><td>b0</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b1</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b2
b3</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b4</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b5</td><td>UBTS</td><td>User boot mode startup flag</td></tr><tr><td>b6</td><td>—</td><td>(Reserved bit)</td></tr></table></td></tr>
<tr><td>Resets</td><td>Functions</td><td>• Specification overview
<table><tr><td>Reset types</td><td>Pin reset</td></tr><tr><td></td><td>—</td></tr><tr><td></td><td>—</td></tr><tr><td></td><td>—</td></tr><tr><td></td><td>—</td></tr><tr><td></td><td>Deep software standby reset</td></tr><tr><td></td><td>—</td></tr><tr><td></td><td>Watchdog timer reset</td></tr><tr><td></td><td>—</td></tr><tr><td>—</td><td>—</td></tr></table></td><td>• Specification overview
<table><tr><td>Reset types</td><td>RES# pin reset</td></tr><tr><td></td><td>Power-on reset</td></tr><tr><td></td><td>Voltage monitoring 0 reset</td></tr><tr><td></td><td>Voltage monitoring 1 reset</td></tr><tr><td></td><td>Voltage monitoring 2 reset</td></tr><tr><td></td><td>Deep software standby reset</td></tr><tr><td></td><td>Independent watchdog timer reset</td></tr><tr><td></td><td>Watchdog timer reset</td></tr><tr><td></td><td>Software reset</td></tr><tr><td>Extended function</td><td>Cold start/warm start determination function</td></tr></table></td></tr>
<tr><td rowspan="3">Registers/ bits</td><td>• Reset status register (RSTSR)
<table><tr><td>b0</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b1</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b2</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b7</td><td>DPSRSTF</td><td>Deep software standby reset flag</td></tr></table></td><td>• Reset status register 0 (RSTSR0)
<table><tr><td>b0</td><td>PORF</td><td>Power-on reset detect flag</td></tr><tr><td>b1</td><td>LVD0RF</td><td>Voltage-monitoring 0 reset detect flag</td></tr><tr><td>b2</td><td>LVD1RF</td><td>Voltage-monitoring 1 reset detect flag</td></tr><tr><td>b3</td><td>LVD2RF</td><td>Voltage-monitoring 2 reset detect flag</td></tr><tr><td>b7</td><td>DPSRSTF</td><td>Deep software standby reset flag</td></tr></table></td></tr>
<tr><td>—</td><td>• Reset status register 1 (RSTSR1)
• Reset status register 2 (RSTSR2)</td></tr>
<tr><td>• Reset control/status register (RSTCSR)
—</td><td>—
• Software reset register (SWRR)</td></tr>
</table>

Table 2.2 Differences in Functions and Specifications (2)

Item		RX610 Group	RX630 Group
Option-setting memory	Registers/ bits	—	• Option function select register 0 (OFS0) • Option function select register 1 (OFS1) • Endian select register B (MDEB) • Endian select register S (MDES)
Voltage detection circuit	Registers/ bits	—	• Voltage monitoring 1 circuit control register 1 (LVD1CR1) • Voltage monitoring 1 circuit status register (LVD1SR) • Voltage monitoring 2 circuit control register 1 (LVD2CR1) • Voltage monitoring 2 circuit status register (LVD2SR) • Voltage monitoring circuit control register (LVCMPCR) • Voltage detection level select register (LVDLVLR) • Voltage monitoring 1 circuit control register 0 (LVD1CR0) • Voltage monitoring 2 circuit control register 0 (LVD2CR0)
Clock oscillator	Functions	• Specification overview Clock types: ICLK: 100.0 MHz (max); PCLK: 50.0 MHz (max); —; BCLK: 25.0 MHz (max); BCLK output pin: 25.0 MHz (max); —; —; —; —; —; —; —	• Specification overview Clock types: ICLK: 100.0 MHz (max); PCLKB: 50.0 MHz (max); FCLK: 50.0 MHz (max); BCLK: 50.0 MHz (max); BCLK output pin: 25.0 MHz (max); UCLK: 48.0 MHz (max); CANMCLK: 20.0 MHz (max); IECLK: 50.0 MHz (max); RTCMCLK: 4.0 MHz to 16.0 MHz; RTCSCLK: 32.768 kHz; IWDTCLK: 125.000 kHz (typ); JTAGTCK: 10.0 MHz (max)
	Main clock oscillator	• Specification overview Resonator: Crystal oscillator; — Frequency: 8.0 MHz to 14.0 MHz External clock: 14.0 MHz (max)	• Specification overview Resonator: Crystal oscillator; Ceramic oscillator Frequency: 4.0 MHz to 16.0 MHz External clock: 20.0 MHz (max)
	Sub-clock oscillator	—	• Specification overview Resonator: Crystal oscillator Frequency: 32.768 Hz
	Low-speed on-chip oscillator	—	• Oscillation frequency: 125.0 kHz
	High-speed on-chip oscillator	—	• Oscillation frequency: 50.0 MHz • HOCO power supply control
	IWDT-dedicated on-chip oscillator	—	• Oscillation frequency: 125.0 kHz

Table 2.3 Differences in Functions and Specifications (3)

<table>
<tr><th colspan="2">Item</th><th>RX610 Group</th><th>RX630 Group</th></tr>
<tr><td>Clock oscillator</td><td>Registers/ bits</td><td>• System clock control register (SCKCR)
<table>
<tr><td>b0
b7</td><td>—</td><td>(Reserved bits)</td></tr>
<tr><td>b8
b11</td><td>PCK [3:0]</td><td>Peripheral module clock (PCLK) select bits</td></tr>
<tr><td>b16
b19</td><td>BCK [3:0]</td><td>External bus clock (BCLK) select bits</td></tr>
<tr><td>b23</td><td>PSTOP1</td><td>BCLK output stop bit</td></tr>
<tr><td>b24
b27</td><td>ICK [3:0]</td><td>System clock (ICLK) select bits</td></tr>
<tr><td>b28
b31</td><td>—</td><td>(Reserved bits)</td></tr>
</table>
• b7 to b0: Reserved bits
These bits are always read as 0. The write value should always be 0.
• PCK[3:0], BCK[3:0], ICK[3:0]
0000b: ×8
0001b: ×4
0010b: ×2
0011b: ×1</td><td>• System clock control register (SCKCR)
<table>
<tr><td>b0
b3</td><td>—</td><td>(Reserved bits)</td></tr>
<tr><td>b4
b7</td><td>—</td><td>(Reserved bits)</td></tr>
<tr><td>b8
b11</td><td>PCKB[3:0]</td><td>Peripheral module clock B (PCLKB) select bits</td></tr>
<tr><td>b16
b19</td><td>BCK [3:0]</td><td>External bus clock (BCLK) select bits</td></tr>
<tr><td>b23</td><td>PSTOP1</td><td>BCLK pin output control bit</td></tr>
<tr><td>b24
b27</td><td>ICK [3:0]</td><td>System clock (ICLK) select bits</td></tr>
<tr><td>b28
b31</td><td>FCK [3:0]</td><td>FlashIF clock (FCLK) select bits</td></tr>
</table>
• b7 to b4, b3 to b0: Reserved bits
These bits should be set to 0001b.
• PCKB[3:0], BCK[3:0], ICK[3:0], FCK[3:0]
0000b: ×1/1
0001b: ×1/2
0010b: ×1/4
0011b: ×1/8
0100b: ×1/16
0101b: ×1/32
0110b: ×1/64</td></tr>
<tr><td></td><td></td><td rowspan="14">—</td><td>• System clock control register 2 (SCKCR2)</td></tr>
<tr><td></td><td></td><td>• System clock control register 3 (SCKCR3)</td></tr>
<tr><td></td><td></td><td>• PLL control register (PLLCR)</td></tr>
<tr><td></td><td></td><td>• PLL control register 2 (PLLCR2)</td></tr>
<tr><td></td><td></td><td>• External bus clock control register (BCKCR)</td></tr>
<tr><td></td><td></td><td>• Main clock oscillator control register (MOSCCR)</td></tr>
<tr><td></td><td></td><td>• Sub-clock oscillator control register (SOSCCR)</td></tr>
<tr><td></td><td></td><td>• Low-speed on-chip oscillator control register (LOCOCR)</td></tr>
<tr><td></td><td></td><td>• IWDT-dedicated on-chip oscillator control register (ILOCOCR)</td></tr>
<tr><td></td><td></td><td>• High-speed on-chip oscillator control register (HOCOCR)</td></tr>
<tr><td></td><td></td><td>• Oscillation stop detection control register (OSTDCR)</td></tr>
<tr><td></td><td></td><td>• Oscillation stop detection status register (OSTDSR)</td></tr>
<tr><td></td><td></td><td>• Main clock oscillator forced oscillation control register (MOFCR)</td></tr>
<tr><td></td><td></td><td>• High-speed on-chip oscillator power supply control register (HOCOPCR)</td></tr>
<tr><td>Frequency measurement circuit</td><td>Registers/ bits</td><td>—</td><td>• Counter-clock extension register 1 (SCK1)
• Counter-clock extension register 2 (SCK2)</td></tr>
</table>

Table 2.4 Differences in Functions and Specifications (4)

<table>
<tr><th colspan="2">Item</th><th>RX610 Group</th><th>RX630 Group</th></tr>
<tr><td rowspan="3">Low power consumption functions</td><td>Functions</td><td>• Specification overview
<table><tr><td rowspan="4">Low power consumption states</td><td>Sleep mode</td></tr><tr><td>All-module clock stop mode</td></tr><tr><td>Software standby mode</td></tr><tr><td>Deep software standby mode</td></tr><tr><td rowspan="2">—</td><td>—</td></tr><tr><td>—</td></tr></table></td><td>• Specification overview
<table><tr><td rowspan="4">Low power consumption states</td><td>Sleep mode</td></tr><tr><td>All-module clock stop mode</td></tr><tr><td>Software standby mode</td></tr><tr><td>Deep software standby mode</td></tr><tr><td rowspan="2">Function for lower operating power consumption</td><td>Low-speed operation mode 1</td></tr><tr><td>Low-speed operation mode 2</td></tr></table></td></tr>
<tr><td>Registers/ bits</td><td>• Standby control register (SBYCR)
<table><tr><td>b8 b12</td><td>STS[4:0]</td><td>Standby timer select bits</td></tr><tr><td>b14</td><td>OPE</td><td>Output port enable bit</td></tr><tr><td>b15</td><td>SSBY</td><td>Software standby bit</td></tr></table>
• SBYCR.STS[4:0]
00000b: (Setting prohibited)
00001b: (Setting prohibited)
00010b: (Setting prohibited)
00011b: (Setting prohibited)
00100b: (Setting prohibited)
00101b: Waiting time = 64 cycles
00110b: Waiting time = 512 cycles
00111b: Waiting time = 1024 cycles
01000b: Waiting time = 2048 cycles
01001b: Waiting time = 4096 cycles
01010b: Waiting time = 16384 cycles
01011b: Waiting time = 32768 cycles
01100b: Waiting time = 65536 cycles
01101b: Waiting time = 131072 cycles
01110b: Waiting time = 262144 cycles
01111b: Waiting time = 524288 cycles

• Module stop control register A (MSTPCRA)
<table><tr><td>b4</td><td>MSTPA4</td><td>8-bit timer 3/2 (unit 1) module stop bit</td></tr><tr><td>b5</td><td>MSTPA5</td><td>8-bit timer 1/0 (unit 0) module stop bit</td></tr><tr><td>b9</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b10</td><td>MSTPA10</td><td>Programmable pulse generator 1 (unit 1) module stop bit</td></tr><tr><td>b11</td><td>MSTPA11</td><td>Programmable pulse generator 0 (unit 0) module stop bit</td></tr><tr><td>b12</td><td>MSTPA12</td><td>16-bit timer pulse unit 1 (unit 1) module stop bit</td></tr><tr><td>b13</td><td>MSTPA13</td><td>16-bit timer pulse unit 0 (unit 0) module stop bit</td></tr><tr><td>b14</td><td>MSTPA14</td><td>Compare match timer 1 (unit 1) module stop bit</td></tr><tr><td>b15</td><td>MSTPA15</td><td>Compare match timer 0 (unit 0) module stop bit</td></tr><tr><td>b17</td><td>—</td><td>(Reserved bit)</td></tr></table></td><td>• Standby control register (SBYCR)
<table><tr><td>b8 b12</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b14</td><td>OPE</td><td>Output port enable bit</td></tr><tr><td>b15</td><td>SSBY</td><td>Software standby bit</td></tr></table>
• Main clock oscillator wait control register (MOSCWTCR)
<table><tr><td>b0 b4</td><td>MSTS[4:0]</td><td>Main clock oscillator waiting time bits</td></tr></table>
• MOSCWTCR. MSTS[4:0]
00000b: Waiting time = 2 cycles
00001b: Waiting time = 4 cycles
00010b: Waiting time = 8 cycles
00011b: Waiting time = 16 cycles
00100b: Waiting time = 32 cycles
00101b: Waiting time = 64 cycles
00110b: Waiting time = 512 cycles
00111b: Waiting time = 1024 cycles
01000b: Waiting time = 2048 cycles
01001b: Waiting time = 4096 cycles
01010b: Waiting time = 16384 cycles
01011b: Waiting time = 32768 cycles
01100b: Waiting time = 65536 cycles
01101b: Waiting time = 131072 cycles
01110b: Waiting time = 262144 cycles
01111b: Waiting time = 524288 cycles

• PLL wait control register (PLLWTCR)
<table><tr><td>b0 b4</td><td>PSTS[4:0]</td><td>PLL waiting time bits</td></tr></table>
• PLLWTCR.PSTS[4:0]
00000b: Waiting time = 16 cycles
... ...
01111b: Waiting time = 4194304 cycles

• Module stop control register A (MSTPCRA)
<table><tr><td>b4</td><td>MSTPA4</td><td>8-bit timer 3/2 (unit 1) module stop bit</td></tr><tr><td>b5</td><td>MSTPA5</td><td>8-bit timer 1/0 (unit 0) module stop bit</td></tr><tr><td>b9</td><td>MSTPA9</td><td>Multifunction timer pulse unit 2 module stop bit</td></tr><tr><td>b10</td><td>MSTPA10</td><td>Programmable pulse generator (unit 1) module stop bit</td></tr><tr><td>b11</td><td>MSTPA11</td><td>Programmable pulse generator (unit 0) module stop bit</td></tr><tr><td>b12</td><td>MSTPA12</td><td>16-bit timer pulse unit 1 (unit 1) module stop bit</td></tr><tr><td>b13</td><td>MSTPA13</td><td>16-bit timer pulse unit 0 (unit 0) module stop bit</td></tr><tr><td>b14</td><td>MSTPA14</td><td>Compare match timer (unit 1) module stop bit</td></tr><tr><td>b15</td><td>MSTPA15</td><td>Compare match timer (unit 0) module stop bit</td></tr><tr><td>b17</td><td>MSTPA17</td><td>12-bit A/D converter module stop bit</td></tr></table></td></tr>
</table>

Table 2.5 Differences in Functions and Specifications (5)

Item		RX610 Group	RX630 Group
Low power consumption functions	Registers/ bits	• Module stop control register A (MSTPCRA)	• Module stop control register A (MSTPCRA)

b19	MSTPA19	D/A converter module stop bit	b19	MSTPA19	D/A converter module stop bit
b20	MSTPA20	A/D converter (unit 3) module stop bit	b20	—	(Reserved bit)
b21	MSTPA21	A/D converter (unit 2) module stop bit	b21	—	(Reserved bit)
b22	MSTPA22	A/D converter (unit 1) module stop bit	b22	—	(Reserved bit)
b23	MSTPA23	A/D converter (unit 0) module stop bit	b23	MSTPA23	10-bit A/D converter (unit 0) module stop bit
b24	—	(Reserved bit)	b24	MSTPA24	module stop A24 bit
b27	MSTPA27	Data transfer controller module stop bit	b27	MSTPA27	module stop A27 bit
b28	MSTPA28	DMA controller module stop bit	b28	MSTPA28	DMA controller/ Data transfer controller module stop bit
b29	—	(Reserved bit)	b29	MSTPA29	module stop A29 bit
b31	ACSE	All-module clock stop mode enable bit	b31	ACSE	All-module clock stop mode enable bit

• Module stop control register B (MSTPCRB)

b0	—	(Reserved bit)	b0	MSTPB0	CAN module 0 module stop bit
b1	—	(Reserved bit)	b1	MSTPB1	CAN module 1 module stop bit
b2	—	(Reserved bit)	b2	MSTPB2	CAN module 2 module stop bit
b4	—	(Reserved bit)	b4	MSTPB4	Serial communications interface SCId module stop bit
b8	—	(Reserved bit)	b8	MSTPB8	Temperature sensor module stop bit
b16	—	(Reserved bit)	b16	MSTPB16	Serial peripheral interface 1 module stop bit
b17	—	(Reserved bit)	b17	MSTPB17	Serial peripheral interface 0 module stop bit
b19	—	(Reserved bit)	b19	MSTPB19	Universal serial bus interface (port 0) module stop bit
b20	MSTPB20	I^2C bus interface 1 (unit 1) module stop bit	b20	MSTPB20	I^2C bus interface 1 module stop bit
b21	MSTPB21	I^2C bus interface 0 (unit 0) module stop bit	b21	MSTPB21	I^2C bus interface 0 module stop bit
b23	MSTPB23	CRC calculator module stop bit	b23	MSTPB23	CRC calculator module stop bit
b24	—	(Reserved bit)	b24	MSTPB24	Serial communications interface 7 module stop bit
b25	MSTPB25	Serial communications interface 6 module stop bit	b25	MSTPB25	Serial communications interface 6 module stop bit
b26	MSTPB26	Serial communications interface 5 module stop bit	b26	MSTPB26	Serial communications interface 5 module stop bit
b27	MSTPB27	Serial communications interface 4 module stop bit	b27	MSTPB27	Serial communications interface 4 module stop bit
b28	MSTPB28	Serial communications interface 3 module stop bit	b28	MSTPB28	Serial communications interface 3 module stop bit
b29	MSTPB29	Serial communications interface 2 module stop bit	b29	MSTPB29	Serial communications interface 2 module stop bit
b30	MSTPB30	Serial communications interface 1 module stop bit	b30	MSTPB30	Serial communications interface 1 module stop bit
b31	MSTPB31	Serial communications interface 0 module stop bit	b31	MSTPB31	Serial communications interface 0 module stop bit

Table 2.6 Differences in Functions and Specifications (6)

<table>
<tr><th colspan="2">Item</th><th>RX610 Group</th><th>RX630 Group</th></tr>
<tr><td rowspan="4">Low power consumption functions</td><td rowspan="4">Registers/ bits</td><td>• Module stop control register C (MSTPCRC)
<table><tr><td>b0</td><td>MSTPC0</td><td>RAM0 module stop bit</td></tr><tr><td>b1</td><td>MSTPC1</td><td>RAM1 module stop bit</td></tr><tr><td>b16</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b17</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b18</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b19</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b22</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b24</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b25</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b26</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b27</td><td>—</td><td>(Reserved bit)</td></tr></table></td><td>• Module stop control register C (MSTPCRC)
<table><tr><td>b0</td><td>MSTPC0</td><td>RAM0 module stop bit</td></tr><tr><td>b1</td><td>MSTPC1</td><td>RAM1 module stop bit</td></tr><tr><td>b16</td><td>MSTPC16</td><td>I²C bus interface 3 module stop bit</td></tr><tr><td>b17</td><td>MSTPC17</td><td>I²C bus interface 2 module stop bit</td></tr><tr><td>b18</td><td>MSTPC18</td><td>IEBUS module stop bit</td></tr><tr><td>b19</td><td>MSTPC19</td><td>Frequency measurement circuit module stop bit</td></tr><tr><td>b22</td><td>MSTPC22</td><td>Serial peripheral interface 2 module stop bit</td></tr><tr><td>b24</td><td>MSTPC24</td><td>Serial communications interface 11 module stop bit</td></tr><tr><td>b25</td><td>MSTPC25</td><td>Serial communications interface 10 module stop bit</td></tr><tr><td>b26</td><td>MSTPC26</td><td>Serial communications interface 9 module stop bit</td></tr><tr><td>b27</td><td>MSTPC27</td><td>Serial communications interface 8 module stop bit</td></tr></table></td></tr>
<tr><td>—</td><td>• Operating power control register (OPCCR)
• Sleep mode return clock source switching register (RSTCKCR)
• Sub-clock oscillator wait control register (SOSCWTCR)</td></tr>
<tr><td>• Deep standby control register (DPSBYCR)
<table><tr><td>b0</td><td>RAMCUT0</td><td>On-chip RAM off 0 bit</td></tr><tr><td>b1</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b4</td><td>RAMCUT1</td><td>On-chip RAM off 1 bit</td></tr><tr><td>b5</td><td>RAMCUT2</td><td>On-chip RAM off 2 bit</td></tr><tr><td>b6</td><td>IOKEEP</td><td>I/O port retention bit</td></tr><tr><td>b7</td><td>DPSBY</td><td>Deep software standby bit</td></tr></table>• RAMCUT2 to RAMCUT0
000b: Power is supplied to the on-chip RAM (RAM0) and USB resume detecting unit in deep software standby mode.
111b: Power is not supplied to the on-chip RAM (RAM0) and USB resume detecting unit in deep software standby mode.</td><td>• Deep standby control register (DPSBYCR)
<table><tr><td>b0
b1</td><td>DEEPCUT [1:0]</td><td>Deep cut bits</td></tr><tr><td>b4</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b6</td><td>IOKEEP</td><td>I/O port retention bit</td></tr><tr><td>b7</td><td>DPSBY</td><td>Deep software standby bit</td></tr></table>• DEEPCUT[1:0]
00b: Power is supplied to the RAM (RAM0) and USB resume detecting unit in deep software standby mode.
01b: Power is not supplied to the RAM (RAM0) and USB resume detecting unit in deep software standby mode.
10b: (Setting prohibited)
11b: Power is not supplied to the RAM (RAM0) and USB resume detecting unit in deep software standby mode. In addition, the LVD is stopped and the low power consumption function of the power-on reset circuit is enabled.</td></tr>
<tr><td>• Deep standby wait control register (DPSWCR)
• DPSWCR.WTSTS[5:0]
00101b: Waiting time = 64 cycles
00110b: Waiting time = 512 cycles
00111b: Waiting time = 1024 cycles
01000b: Waiting time = 2048 cycles
01001b: Waiting time = 4096 cycles
01010b: Waiting time = 16384 cycles
01011b: Waiting time = 32768 cycles
01100b: Waiting time = 65536 cycles
01101b: Waiting time = 131072 cycles
01110b: Waiting time = 262144 cycles
01111b: Waiting time = 524288 cycles</td><td>—
(LOCO return)</td></tr>
</table>

Table 2.7 Differences in Functions and Specifications (7)

<table>
<tr><th colspan="2">Item</th><th>RX610 Group</th><th>RX630 Group</th></tr>
<tr><td>Low power consumption functions</td><td>Registers/ bits</td><td>

• Deep standby interrupt enable register (DPSIER)

<table>
<tr><td>b0</td><td>DIRQ0E</td><td>IRQ0 pin enable bit</td></tr>
<tr><td>b1</td><td>DIRQ1E</td><td>IRQ1 pin enable bit</td></tr>
<tr><td>b2</td><td>DIRQ2E</td><td>IRQ2 pin enable bit</td></tr>
<tr><td>b3</td><td>DIRQ3E</td><td>IRQ3 pin enable bit</td></tr>
<tr><td>b4</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b6</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b7</td><td>DNMIE</td><td>NMI pin enable bit</td></tr>
</table>

—

• Deep standby interrupt flag register (DPSIFR)

<table>
<tr><td>b0</td><td>DIRQ0F</td><td>IRQ0 deep standby cancel flag</td></tr>
<tr><td>b1</td><td>DIRQ1F</td><td>IRQ1 deep standby cancel flag</td></tr>
<tr><td>b2</td><td>DIRQ2F</td><td>IRQ2 deep standby cancel flag</td></tr>
<tr><td>b3</td><td>DIRQ3F</td><td>IRQ3 deep standby cancel flag</td></tr>
<tr><td>b4</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b6</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b7</td><td>DNMIF</td><td>NMI deep standby cancel flag</td></tr>
</table>

</td><td>

• Deep standby interrupt enable register 0 (DPSIER0)

<table>
<tr><td>b0</td><td>DIRQ0E</td><td>IRQ0-DS pin enable bit</td></tr>
<tr><td>b1</td><td>DIRQ1E</td><td>IRQ1-DS pin enable bit</td></tr>
<tr><td>b2</td><td>DIRQ2E</td><td>IRQ2-DS pin enable bit</td></tr>
<tr><td>b3</td><td>DIRQ3E</td><td>IRQ3-DS pin enable bit</td></tr>
<tr><td>b4</td><td>DIRQ4E</td><td>IRQ4-DS pin enable bit</td></tr>
<tr><td>b5</td><td>DIRQ5E</td><td>IRQ5-DS pin enable bit</td></tr>
<tr><td>b6</td><td>DIRQ6E</td><td>IRQ6-DS pin enable bit</td></tr>
<tr><td>b7</td><td>DIRQ7E</td><td>IRQ7-DS pin enable bit</td></tr>
</table>

• Deep standby interrupt enable register 2 (DPSIER2)

<table>
<tr><td>b0</td><td>DLVD1IE</td><td>LVD1 deep standby cancel signal enable bit</td></tr>
<tr><td>b1</td><td>DLVD2IE</td><td>LVD2 deep standby cancel signal enable bit</td></tr>
<tr><td>b2</td><td>DRTCIIE</td><td>RTC interval interrupt deep standby cancel signal enable bit</td></tr>
<tr><td>b3</td><td>DRTCAIE</td><td>RTC alarm interrupt deep standby cancel signal enable bit</td></tr>
<tr><td>b4</td><td>DNMIE</td><td>NMI pin enable bit</td></tr>
<tr><td>b5</td><td>DRIICDIE</td><td>SDA2-DS deep standby cancel signal enable bit</td></tr>
<tr><td>b6</td><td>DRIICCIE</td><td>SCL2-DS deep standby cancel signal enable bit</td></tr>
<tr><td>b7</td><td>DUSBIE</td><td>USB suspend/resume deep standby cancel signal enable bit</td></tr>
</table>

• Deep standby interrupt enable register 1 (DPSIER1)

• Deep standby interrupt enable register 3 (DPSIER3)

• Deep standby interrupt flag register 0 (DPSIFR0)

<table>
<tr><td>b0</td><td>DIRQ0F</td><td>IRQ0-DS deep standby cancel flag</td></tr>
<tr><td>b1</td><td>DIRQ1F</td><td>IRQ1-DS deep standby cancel flag</td></tr>
<tr><td>b2</td><td>DIRQ2F</td><td>IRQ2-DS deep standby cancel flag</td></tr>
<tr><td>b3</td><td>DIRQ3F</td><td>IRQ3-DS deep standby cancel flag</td></tr>
<tr><td>b4</td><td>DIRQ4F</td><td>IRQ4-DS deep standby cancel flag</td></tr>
<tr><td>b5</td><td>DIRQ5F</td><td>IRQ5-DS deep standby cancel flag</td></tr>
<tr><td>b6</td><td>DIRQ6F</td><td>IRQ6-DS deep standby cancel flag</td></tr>
<tr><td>b7</td><td>DIRQ7F</td><td>IRQ7-DS deep standby cancel flag</td></tr>
</table>

• Deep standby interrupt flag register 2 (DPSIFR2)

<table>
<tr><td>b0</td><td>DLVD1IF</td><td>LVD1 deep standby cancel flag</td></tr>
<tr><td>b1</td><td>DLVD2IF</td><td>LVD2 deep standby cancel flag</td></tr>
<tr><td>b2</td><td>DRTCIIF</td><td>RTC interval interrupt deep standby cancel flag</td></tr>
<tr><td>b3</td><td>DRTCAIF</td><td>RTC alarm interrupt deep standby cancel flag</td></tr>
<tr><td>b4</td><td>DNMIF</td><td>NMI deep standby cancel flag</td></tr>
<tr><td>b5</td><td>DRIICDIF</td><td>SDA2-DS deep standby cancel flag</td></tr>
<tr><td>b6</td><td>DRIICCIF</td><td>SCL2-DS deep standby cancel flag</td></tr>
<tr><td>b7</td><td>DUSBIF</td><td>USB suspend/resume deep standby cancel flag</td></tr>
</table>

</td></tr>
</table>

Table 2.8 Differences in Functions and Specifications (8)

<table>
<tr><th colspan="2">Item</th><th>RX610 Group</th><th>RX630 Group</th></tr>
<tr><td rowspan="4">Low power consumption functions</td><td rowspan="4">Registers/ bits</td><td>—</td><td>• Deep standby interrupt flag register 1 (DPSIFR1)
• Deep standby interrupt flag register 3 (DPSIFR3)</td></tr>
<tr><td>• Deep standby interrupt edge register (DPSIEGR)
<table><tr><td>b0</td><td>DIRQ0EG</td><td>IRQ0 edge select bit</td></tr><tr><td>b1</td><td>DIRQ1EG</td><td>IRQ1 edge select bit</td></tr><tr><td>b2</td><td>DIRQ2EG</td><td>IRQ2 edge select bit</td></tr><tr><td>b3</td><td>DIRQ3EG</td><td>IRQ3 edge select bit</td></tr><tr><td>b4</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b6</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b7</td><td>DNMIEG</td><td>NMI edge select bit</td></tr></table></td><td>• Deep standby interrupt edge register 0 (DPSIEGR0)
<table><tr><td>b0</td><td>DIRQ0EG</td><td>IRQ0-DS pin edge select bit</td></tr><tr><td>b1</td><td>DIRQ1EG</td><td>IRQ1-DS pin edge select bit</td></tr><tr><td>b2</td><td>DIRQ2EG</td><td>IRQ2-DS pin edge select bit</td></tr><tr><td>b3</td><td>DIRQ3EG</td><td>IRQ3-DS pin edge select bit</td></tr><tr><td>b4</td><td>DIRQ4EG</td><td>IRQ4-DS pin edge select bit</td></tr><tr><td>b5</td><td>DIRQ5EG</td><td>IRQ5-DS pin edge select bit</td></tr><tr><td>b6</td><td>DIRQ6EG</td><td>IRQ6-DS pin edge select bit</td></tr><tr><td>b7</td><td>DIRQ7EG</td><td>IRQ7-DS pin edge select bit</td></tr></table>• Deep standby interrupt edge register 2 (DPSIEGR 2)
<table><tr><td>b0</td><td>DLVD1EG</td><td>LVD1 edge select bit</td></tr><tr><td>b1</td><td>DLVD2EG</td><td>LVD2 edge select bit</td></tr><tr><td>b4</td><td>DNMIEG</td><td>NMI edge select bit</td></tr><tr><td>b5</td><td>DRIICDEG</td><td>SDA2-DS edge select bit</td></tr><tr><td>b6</td><td>DRIICCEG</td><td>SCL2-DS edge select bit</td></tr></table></td></tr>
<tr><td>—</td><td>• Deep standby interrupt edge register 1 (DPSIEGR1)
• Deep standby interrupt edge register 3 (DPSIEGR3)</td></tr>
<tr><td>Battery backup function</td><td>Functions</td><td>—</td><td>• Specification overview
<table><tr><td>Battery backup power supplied to</td><td>Sub-clock oscillator
Realtime clock</td></tr></table></td></tr>
<tr><td>Register write protection function</td><td>Registers/ bits</td><td>—</td><td>• Protect register (PRCR)</td></tr>
<tr><td rowspan="4">Interrupt controller</td><td rowspan="4">Functions</td><td>• Peripheral function interrupts
<table><tr><td>Interrupts</td><td>Interrupts from peripheral modules</td></tr><tr><td>Sources</td><td>116</td></tr><tr><td>Interrupt detection</td><td>Edge detection/level detection</td></tr></table></td><td>• Peripheral function interrupts
<table><tr><td>Interrupts</td><td>Interrupts from peripheral modules</td></tr><tr><td>Sources</td><td>180</td></tr><tr><td>Interrupt detection</td><td>Edge detection/level detection</td></tr></table></td></tr>
<tr><td>—</td><td>• Group function interrupts
<table><tr><td>Edge detection</td><td>7 (groups 0 to 6)</td></tr><tr><td>Level detection</td><td>1 (group 12)</td></tr></table>• Unit selection function
<table><tr><td>Units</td><td>6</td></tr></table></td></tr>
<tr><td>• Non-maskable interrupts
<table><tr><td>Interrupt types</td><td>NMI pin interrupt
—
—
—
—
—</td></tr></table></td><td>• Non-maskable interrupts
<table><tr><td>Interrupt types</td><td>NMI pin interrupt
Digital filter function: Supported
Oscillation stop detection
WDT underflow/ refresh error
IWDT underflow/ refresh error
Voltage-monitoring 1 interrupt
Voltage-monitoring 2 interrupt</td></tr></table></td></tr>
<tr><td>• Return from power-down modes
<table><tr><td>Sleep mode</td><td>Non-maskable interrupts
All interrupt sources</td></tr><tr><td>All-module clock stop mode</td><td>Non-maskable interrupts
IRQ0 to IRQ15 interrupts
WDT interrupts
TMR interrupts
—
—</td></tr><tr><td>Software standby mode</td><td>Non-maskable interrupts
IRQ0 to IRQ15 interrupts
—
—</td></tr></table></td><td>• Return from power-down modes
<table><tr><td>Sleep mode</td><td>Non-maskable interrupts
All interrupt sources</td></tr><tr><td>All-module clock stop mode</td><td>Non-maskable interrupts
IRQ0 to IRQ15 interrupts
— (WDT: Non-maskable interrupts)
TMR interrupts
USB resume interrupts
RTC alarm/periodic interrupts</td></tr><tr><td>Software standby mode</td><td>Non-maskable interrupts
IRQ0 to IRQ15 interrupts
USB resume interrupts
RTC alarm/periodic interrupts</td></tr></table></td></tr>
</table>

Table 2.9 Differences in Functions and Specifications (9)

Item		RX610 Group	RX630 Group
Interrupt controller	Vector table	• Vector table (1/4)	• Vector table (1/4)

No	Interrupt	Name	DTCER	IPR
0	—	(Reserved)	—	—
1	—	(Reserved)	—	—
2	—	(Reserved)	—	—
3	—	(Reserved)	—	—
4	—	(Reserved)	—	—
5	—	(Reserved)	—	—
6	—	(Reserved)	—	—
7	—	(Reserved)	—	—
8	—	(Reserved)	—	—
9	—	(Reserved)	—	—
10	—	(Reserved)	—	—
11	—	(Reserved)	—	—
12	—	(Reserved)	—	—
13	—	(Reserved)	—	—
14	—	(Reserved)	—	—
15	—	(Reserved)	—	—
16	Bus error	BUSERR	—	00
21	FCU	FIFERR	—	01
23		FRDYI		02
27	—	(Reserved)	—	—
28	CMT unit 0	CMI0	028	04
29		CMI1	029	05
30	CMT unit 1	CMI2	030	06
31		CMI3	031	07
33	—	(Reserved)	—	—
34	—	(Reserved)	—	—
35	—	(Reserved)	—	—
39	—	(Reserved)	—	—
40	—	(Reserved)	—	—
41	—	(Reserved)	—	—
42	—	(Reserved)	—	—
43	—	(Reserved)	—	—
44	—	(Reserved)	—	—
45	—	(Reserved)	—	—
46	—	(Reserved)	—	—
47	—	(Reserved)	—	—
48	—	(Reserved)	—	—
49	—	(Reserved)	—	—
50	—	(Reserved)	—	—
51	—	(Reserved)	—	—
52	—	(Reserved)	—	—
53	—	(Reserved)	—	—
54	—	(Reserved)	—	—
55	—	(Reserved)	—	—
56	—	(Reserved)	—	—
57	—	(Reserved)	—	—
58	—	(Reserved)	—	—
59	—	(Reserved)	—	—
62	—	(Reserved)	—	—
64	External pin	IRQ0	064	20
65		IRQ1	065	21
66		IRQ2	066	22
67		IRQ3	067	23
68		IRQ4	068	24
69		IRQ5	069	25
70		IRQ6	070	26
71		IRQ7	071	27
72		IRQ8	072	28
73		IRQ9	073	29
74		IRQ10	074	2A
75		IRQ11	075	2B
76		IRQ12	076	2C
77		IRQ13	077	2D
78		IRQ14	078	2E
79		IRQ15	079	2F
90	—	(Reserved)	—	—

No	Interrupt	Name	DTCER	IPR
0	—	Unconditional trap (dedicated)	—	—
1	—	Unconditional trap (dedicated)	—	—
2	—	Unconditional trap (dedicated)	—	—
3	—	Unconditional trap (dedicated)	—	—
4	—	Unconditional trap (dedicated)	—	—
5	—	Unconditional trap (dedicated)	—	—
6	—	Unconditional trap (dedicated)	—	—
7	—	Unconditional trap (dedicated)	—	—
8	—	Unconditional trap (dedicated)	—	—
9	—	Unconditional trap (dedicated)	—	—
10	—	Unconditional trap (dedicated)	—	—
11	—	Unconditional trap (dedicated)	—	—
12	—	Unconditional trap (dedicated)	—	—
13	—	Unconditional trap (dedicated)	—	—
14	—	Unconditional trap (dedicated)	—	—
15	—	Unconditional trap (dedicated)	—	—
16	BSC	BUSERR	—	000
21	FCU	FIFERR	—	001
23		FRDYI		002
27	ICU	SWINT	027	003
28	CMT0	CMI0	028	004
29	CMT1	CMI1	029	005
30	CMT2	CMI2	030	006
31	CMT3	CMI3	031	007
33	USB0	D0FIFO0	033	033
34		D1FIFO0	034	034
35		USBI0	—	035
39	RSPI0	SPRI0	039	039
40		SPTI0	040	
41		SPII0	—	
42	RSPI1	SPRI1	042	042
43		SPTI1	043	
44		SPII1	—	
45	RSPI2	SPRI2	045	045
46		SPTI2	046	
47		SPII2	—	
48	CAN0	RXF0	—	048
49		TXF0		
50		RXM0		
51		TXM0		
52	CAN1	RXF1	—	052
53		TXF1		
54		RXM1		
55		TXM1		
56	CAN2	RXF2	—	056
57		TXF2		
58		RXM2		
59		TXM2		
62	RTC	CUP	—	062
64	ICU	IRQ0	064	064
65		IRQ1	065	065
66		IRQ2	066	066
67		IRQ3	067	067
68		IRQ4	068	068
69		IRQ5	069	069
70		IRQ6	070	070
71		IRQ7	071	071
72		IRQ8	072	072
73		IRQ9	073	073
74		IRQ10	074	074
75		IRQ11	075	075
76		IRQ12	076	076
77		IRQ13	077	077
78		IRQ14	078	078
79		IRQ15	079	079
90	USB	USBR0	—	090

Table 2.10 Differences in Functions and Specifications (10)

Item		RX610 Group	RX630 Group
Interrupt controller	Vector table	• Vector table (2/4)	• Vector table (2/4)

No	Interrupt	Name	DTCER	IPR
92	—	(Reserved)	—	—
93	—	(Reserved)	—	—
96	WDT	WOVI	—	40
98	AD0	ADI0	098	44
99	AD1	ADI1	099	45
100	AD2	ADI2	100	46
101	AD3	ADI3	101	47
102	—	(Reserved)	—	—
104	TPU0	TGI0A	104	4C
105		TGI0B	105	
106		TGI0C	106	
107		TGI0D	107	
108		TGI0V	—	4D
109	—	(Reserved)	—	—
110	—	(Reserved)	—	—
111	TPU1	TGI1A	111	4E
112		TGI1B	112	
114		(Reserved)	—	—
115		TGI1V	—	4F
116		TGI1U		
117	TPU2	TGI2A	117	50
118		TGI2B	118	
120		TGI2V	—	51
121		TGI2U		
122	TPU3	TGI3A	122	52
123		TGI3B	123	
124		TGI3C	124	
125		TGI3D	125	
126		TGI3V	—	53
127	TPU4	TGI4A	127	54
128		TGI4B	128	
129		(Reserved)	—	—
130		(Reserved)	—	—
131		TGI4V	—	55
132		TGI4U		
133	TPU5	TGI5A	133	56
134		TGI5B	134	
135		(Reserved)	—	—
136		TGI5V	—	57
137		TGI5U		
138	TPU6	TGI6A	138	58
139		TGI6B	139	
140		TGI6C	140	
141		TGI6D	141	
142		TGI6V	—	59
143		(Reserved)	—	—
144		(Reserved)	—	—
145	TPU7	TGI7A	145	5A
146		TGI7B	146	
147		(Reserved)	—	—
148		(Reserved)	—	—
149		TGI7V	—	5B
150		TGI7U		
151	TPU8	TGI5A	151	5C
152		TGI5B	152	
153		(Reserved)	—	—
154		TGI5V	—	5D
155		TGI5U		
156	TPU9	TGI9A	156	5E
157		TGI9B	157	
158		TGI9C	158	
159		TGI9D	159	
160		TGI9V	—	5F

No	Interrupt	Name	DTCER	IPR
92	RTC	ALM	—	092
93		PRD		093
96	—	(Reserved)	—	—
98	AD	ADI0	098	098
99	—	(Reserved)	—	—
100	—	(Reserved)	—	—
101	—	(Reserved)	—	—
102	S12AD	S12ADI0	102	102
104	—	(Reserved)	—	—
105	—	(Reserved)	—	—
106	ICU	GROUP0	—	106
107		GROUP1	—	107
108		GROUP2	—	108
109		GROUP3	—	109
110		GROUP4	—	110
111		GROUP5	—	111
112		GROUP6	—	112
114		GROUP12	—	114
115	—	(Reserved)	—	—
116	—	(Reserved)	—	—
117	—	(Reserved)	—	—
118	—	(Reserved)	—	—
120	—	(Reserved)	—	—
121	—	(Reserved)	—	—
122	SCI12	SCIX0	—	122
123		SCIX1		
124		SCIX2		
125		SCIX3		
126	TPU0	TGI0A	126	126
127		TGI0B	127	
128		TGI0C	128	
129		TGI0D	129	
130	TPU1	TGI1A	130	130
131		TGI1B	131	
132	TPU2	TGI2A	132	132
133		TGI2B	133	
134	TPU3	TGI3A	134	134
135		TGI3B	135	
136		TGI3C	136	
137		TGI3D	137	
138	TPU4	TGI4A	138	138
139		TGI4B	139	
140	TPU5	TGI5A	140	140
141		TGI5B	141	
142	TPU6/MTU0	TGI6A/TGIA0	142	142
143		TGI6B/TGIB0	143	
144		TGI6C/TGIC0	144	
145		TGI6D/TGID0	145	
146		— / TGIE0	—	146
147		— / TGIF0		
148	TPU7/MTU1	TGI7A/TGIA1	148	148
149		TGI7B/TGIB1	149	
150	TPU8/MTU2	TGI8A/TGIA2	150	150
151		TGI8B/TGIB2	151	
152	TPU9/MTU3	TGI9A/TGIA3	152	152
153		TGI9B/TGIB3	153	
154		TGI9C/TGIC3	154	
155		TGI9D/TGID3	155	
156	TPU10/ MTU4	TGI10A/TGIA4	156	156
157		TGI10B/TGIB4	157	
158		— / TGIC4	158	
159		— / TGID4	159	
160		— / TGIV4	160	160

Table 2.11 Differences in Functions and Specifications (11)

Item		RX610 Group	RX630 Group
Interrupt controller	Vector table	• Vector table (3/4)	• Vector table (3/4)

No	Interrupt	Name	DTCER	IPR
161	TPU10	TGI10A	161	60
162		TGI10B	162	
163		(Reserved)	—	—
164		(Reserved)	—	—
165		TGI10V	—	61
166		TGI10U		
167	TPU11	TGI11A	167	62
168		TGI11B	168	
169		(Reserved)	—	—
170		TGI11V	—	63
171		TGI11U		
172	—	(Reserved)	—	—
173	—	(Reserved)	—	—
174	TMR0	CMIA0	174	68
175		CMIB0	175	
176		OVI0	—	
177	TMR1	CMIA1	177	69
178		CMIB1	178	
179		OVI1	—	
180	TMR2	CMIA2	180	6A
181		CMIB2	181	
182		OVI2	—	
183	TMR3	CMIA3	183	6B
184		CMIB3	184	
185		OVI3	—	
186	—	(Reserved)	—	—
187	—	(Reserved)	—	—
188	—	(Reserved)	—	—
189	—	(Reserved)	—	—
190	—	(Reserved)	—	—
191	—	(Reserved)	—	—
192	—	(Reserved)	—	—
193	—	(Reserved)	—	—
194	—	(Reserved)	—	—
195	—	(Reserved)	—	—
196	—	(Reserved)	—	—
197	—	(Reserved)	—	—
198	DMAC	DMTEND0	198	70
199		DMTEND1	199	71
200		DMTEND2	200	72
201		DMTEND3	201	73
214	SCI0	ERI0	—	80
215		RXI0	215	
216		TXI0	216	
217		TEI0	—	
218	SCI1	ERI1	—	81
219		RXI1	219	
220		TXI1	220	
221		TEI1	—	
222	SCI2	ERI2	—	82
223		RXI2	223	
224		TXI2	224	
225		TEI2	—	
226	SCI3	ERI3	—	83
227		RXI3	227	
228		TXI3	228	
229		TEI3	—	
230	SCI4	ERI4	—	84
231		RXI4	231	
232		TXI4	232	
233		TEI4	—	
234	SCI5	ERI5	—	85
235		RXI5	235	
236		TXI5	236	
237		TEI5	—	

No	Interrupt	Name	DTCER	IPR
161	TPU11/ MTU5	— / TGIU5	161	161
162		— / TGIV5	162	
163		— / TGIW5	163	
164		TGI11A / —	164	164
165		TGI11B / —	165	
166	POE	OEI0	—	166
167		OEI1		
168	—	(Reserved)	—	—
169	—	(Reserved)	—	—
170	TMR0	CMIA0	170	170
171		CMIB0	171	
172		OVI0	—	
173	TMR1	CMIA1	173	173
174		CMIB1	174	
175		OVI1	—	
176	TMR2	CMIA2	176	176
177		CMIB2	177	
178		OVI2	—	
179	TMR3	CMIA3	179	179
180		CMIB3	180	
181		OVI3	—	
182	RIIC0	EEI0	—	182
183		RXI0	183	183
184		TXI0	184	184
185		TEI0	—	185
186	RIIC1	EEI1	—	186
187		RXI1	187	187
188		TXI1	188	188
189		TEI1	—	189
190	RIIC2	EEI2	—	190
191		RXI2	191	191
192		TXI2	192	192
193		TEI2	—	193
194	RIIC3	EEI3	—	194
195		RXI3	195	195
196		TXI3	196	196
197		TEI3	—	197
198	DMAC	DMAC0I	198	198
199		DMAC1I	199	199
200		DMAC2I	200	200
201		DMAC3I	201	201
214	SCI0	RXI0	214	214
215		TXI0	215	
216		TEI0	—	
217	SCI1	RXI1	217	217
218		TXI1	218	
219		TEI1	—	
220	SCI2	RXI2	220	220
221		TXI2	221	
222		TEI2	—	
223	SCI3	RXI3	223	223
224		TXI3	224	
225		TEI3	—	
226	SCI4	RXI4	226	226
227		TXI4	227	
228		TEI4	—	
229	SCI5	RXI5	229	229
230		TXI5	230	
231		TEI5	—	
232	SCI6	RXI6	232	232
233		TXI6	233	
234		TEI6	—	
235	SCI7	RXI7	235	235
236		TXI7	236	
237		TEI7	—	

Table 2.12 Differences in Functions and Specifications (12)

<table>
<tr><th colspan="2">Item</th><th>RX610 Group</th><th>RX630 Group</th></tr>
<tr><td rowspan="5">Interrupt controller</td><td>Vector table</td><td>• Vector table (4/4)
<table>
<tr><th>NO</th><th>Interrupt</th><th>Name</th><th>DTCER</th><th>IPR</th></tr>
<tr><td>238</td><td>SCI6</td><td>ERI6</td><td>—</td><td>86</td></tr>
<tr><td>239</td><td></td><td>RXI6</td><td>239</td><td></td></tr>
<tr><td>240</td><td></td><td>TXI6</td><td>240</td><td></td></tr>
<tr><td>241</td><td></td><td>TEI6</td><td>—</td><td></td></tr>
<tr><td>242</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
<tr><td>243</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
<tr><td>244</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
<tr><td>245</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
<tr><td>246</td><td>RIIC0</td><td>ICEEI0</td><td>—</td><td>88</td></tr>
<tr><td>247</td><td></td><td>ICRXI0</td><td>247</td><td>89</td></tr>
<tr><td>248</td><td></td><td>ICTXI0</td><td>248</td><td>8A</td></tr>
<tr><td>249</td><td></td><td>ICTEI0</td><td>—</td><td>8B</td></tr>
<tr><td>250</td><td>RIIC1</td><td>ICEEI1</td><td>—</td><td>8C</td></tr>
<tr><td>251</td><td></td><td>ICRXI1</td><td>251</td><td>8D</td></tr>
<tr><td>252</td><td></td><td>ICTXI1</td><td>252</td><td>8E</td></tr>
<tr><td>253</td><td></td><td>ICTEI1</td><td>—</td><td>8F</td></tr>
</table></td><td>• Vector table (4/4)
<table>
<tr><th>No</th><th>Interrupt</th><th>Name</th><th>DTCER</th><th>IPR</th></tr>
<tr><td>238</td><td>SCI8</td><td>RXI8</td><td>238</td><td>238</td></tr>
<tr><td>239</td><td></td><td>TXI8</td><td>239</td><td></td></tr>
<tr><td>240</td><td></td><td>TEI8</td><td>—</td><td></td></tr>
<tr><td>241</td><td>SCI9</td><td>RXI9</td><td>241</td><td>241</td></tr>
<tr><td>242</td><td></td><td>TXI9</td><td>242</td><td></td></tr>
<tr><td>243</td><td></td><td>TEI9</td><td>—</td><td></td></tr>
<tr><td>244</td><td>SCI10</td><td>RXI10</td><td>244</td><td>244</td></tr>
<tr><td>245</td><td></td><td>TXI10</td><td>245</td><td></td></tr>
<tr><td>246</td><td></td><td>TEI10</td><td>—</td><td></td></tr>
<tr><td>247</td><td>SCI11</td><td>RXI11</td><td>247</td><td>247</td></tr>
<tr><td>248</td><td></td><td>TXI11</td><td>248</td><td></td></tr>
<tr><td>249</td><td></td><td>TEI11</td><td>—</td><td></td></tr>
<tr><td>250</td><td>SCI12</td><td>RXI12</td><td>250</td><td>250</td></tr>
<tr><td>251</td><td></td><td>TXI12</td><td>251</td><td></td></tr>
<tr><td>252</td><td></td><td>TEI12</td><td>—</td><td></td></tr>
<tr><td>253</td><td>IEB</td><td>IEBINT</td><td>—</td><td>253</td></tr>
</table></td></tr>
<tr><td>Registers/ bits</td><td>• Interrupt request destination setting register i (ISELRi)</td><td>—</td></tr>
<tr><td></td><td>• Interrupt source priority register i (IPRi)
<table>
<tr><td>b0
b2</td><td>IPR[2:0]</td><td>Interrupt priority level select bits</td></tr>
<tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr>
</table>
• IPR[2:0]
000b: Level 0
001b: Level 1
010b: Level 2
011b: Level 3
100b: Level 4
101b: Level 5
110b: Level 6
111b: Level 7</td><td>• Interrupt source priority register n (IPRn)
<table>
<tr><td>b0

b3</td><td>IPR[3:0]</td><td>Interrupt priority level select bits</td></tr>
</table>
• IPR[3:0]
0000b: Level 0
0001b: Level 1
0010b: Level 2
0011b: Level 3
0100b: Level 4
0101b: Level 5
0110b: Level 6
0111b: Level 7
1000b: Level 8
1001b: Level 9
1010b: Level 10
1011b: Level 11
1100b: Level 12
1101b: Level 13
1110b: Level 14
1111b: Level 15</td></tr>
<tr><td></td><td>—</td><td>• Software interrupt activation register (SWINTR)
• DTC activation enable register n (DTCERn)
• DMAC activation request select register m (DMRSRm)</td></tr>
<tr><td></td><td>• IRQ detection enable register n (IRQERn)</td><td>—</td></tr>
<tr><td></td><td>—</td><td>• IRQ control register i (IRQCRi)
• IRQ pin digital filter enable register 0 (IRQFLTE0)
• IRQ pin digital filter enable register 1 (IRQFLTE1)
• IRQ pin digital filter setting register 0 (IRQFLTC0)
• IRQ pin digital filter setting register 1 (IRQFLTC1)</td></tr>
</table>

Table 2.13 Differences in Functions and Specifications (13)

<table>
<tr><th colspan="2">Item</th><th>RX610 Group</th><th>RX630 Group</th></tr>
<tr><td rowspan="5">Interrupt controller</td><td rowspan="5">Registers/ bits</td><td>• Non-maskable interrupt enable register (NMIER)
<table><tr><td>b0</td><td>NMIEN</td><td>NMI enable bit</td></tr><tr><td>b1</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b2</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b4</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr></table></td><td>• Non-maskable interrupt enable register (NMIER)
<table><tr><td>b0</td><td>NMIEN</td><td>NMI pin interrupt enable bit</td></tr><tr><td>b1</td><td>OSTEN</td><td>Oscillation stop detection interrupt enable bit</td></tr><tr><td>b2</td><td>WDTEN</td><td>WDT underflow/refresh error enable bit</td></tr><tr><td>b3</td><td>IWDTEN</td><td>IWDT underflow/refresh error enable bit</td></tr><tr><td>b4</td><td>LVD1EN</td><td>Voltage-monitoring 1 interrupt enable bit</td></tr><tr><td>b5</td><td>LVD2EN</td><td>Voltage-monitoring 2 interrupt enable bit</td></tr></table></td></tr>
<tr><td>• Non-maskable interrupt status register (NMISR)
<table><tr><td>b0</td><td>NMIST</td><td>NMI status flag</td></tr><tr><td>b1</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b2</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b4</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr></table></td><td>• Non-maskable interrupt status register (NMISR)
<table><tr><td>b0</td><td>NMIST</td><td>NMI status flag</td></tr><tr><td>b1</td><td>OSTST</td><td>Oscillation stop detection interrupt status flag</td></tr><tr><td>b2</td><td>WDTST</td><td>WDT underflow/refresh error status flag</td></tr><tr><td>b3</td><td>IWDTST</td><td>IWDT underflow/refresh error status flag</td></tr><tr><td>b4</td><td>LVD1ST</td><td>Voltage-monitoring 1 interrupt status flag</td></tr><tr><td>b5</td><td>LVD2ST</td><td>Voltage-monitoring 2 interrupt status flag</td></tr></table></td></tr>
<tr><td>• Non-maskable interrupt clear register (NMICLR)
<table><tr><td>b0</td><td>NMICLR</td><td>NMI clear bit</td></tr><tr><td>b1</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b2</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b4</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr></table></td><td>• Non-maskable interrupt status clear register (NMICLR)
<table><tr><td>b0</td><td>NMICLR</td><td>NMI clear bit</td></tr><tr><td>b1</td><td>OSTCLR</td><td>OST clear bit</td></tr><tr><td>b2</td><td>WDTCLR</td><td>WDT clear bit</td></tr><tr><td>b3</td><td>IWDTCLR</td><td>IWDT clear bit</td></tr><tr><td>b4</td><td>LVD1CLR</td><td>LVD1 clear bit</td></tr><tr><td>b5</td><td>LVD2CLR</td><td>LVD2 clear bit</td></tr></table></td></tr>
<tr><td>—</td><td>• NMI pin digital filter enable register (NMIFLTE)
• NMI pin digital filter setting register (NMIFLTC)
• Group m interrupt source register (GRPm)
• Group m interrupt enable register (GENm)
• Group m interrupt clear register (GCRm)
• Unit selecting register (SEL)</td></tr>
<tr><td>• Software standby release IRQ enable register (SSIER)</td><td>—</td></tr>
<tr><td>Bus</td><td>Functions</td><td>• Bus configuration (on-chip peripheral buses)
<table><tr><td>On-chip peripheral bus 1</td><td>DMAC, interrupt controller, bus error monitoring section</td><td>ICLK</td></tr><tr><td>On-chip peripheral bus 2</td><td>Peripheral functions, on-chip ROM, data flash</td><td>PCLK</td></tr><tr><td>—</td><td>—</td><td>—</td></tr><tr><td>—</td><td>—</td><td>—</td></tr><tr><td>—</td><td>—</td><td>—</td></tr><tr><td>—</td><td>—</td><td>—</td></tr></table></td><td>• Bus configuration (on-chip peripheral buses)
<table><tr><td>On-chip peripheral bus 1</td><td>DTC, DMACA interrupt controller, bus error monitoring section</td><td>ICLK</td></tr><tr><td>On-chip peripheral bus 2</td><td>Peripheral functions</td><td>PCLKB</td></tr><tr><td>On-chip peripheral bus 3</td><td>USB</td><td>PCLKB</td></tr><tr><td>On-chip peripheral bus 4</td><td>—</td><td>—</td></tr><tr><td>On-chip peripheral bus 5</td><td>—</td><td>—</td></tr><tr><td>On-chip peripheral bus 6</td><td>ROM, E2 data flash, FCU-RAM</td><td>FCLK</td></tr></table></td></tr>
</table>

Table 2.14 Differences in Functions and Specifications (14)

<table>
<tr><th colspan="2">Item</th><th>RX610 Group</th><th>RX630 Group</th></tr>
<tr><td rowspan="11">Bus</td><td rowspan="11">Functions</td><td>• Bus error (illegal address access)
<table><tr><th rowspan="2">Address</th><th colspan="2">On-chip ROM mode</th></tr><tr><th>Enabled</th><th>Disabled</th></tr><tr><td>0000 0000h to 0007 FFFFh</td><td colspan="2">—</td></tr><tr><td>0008 0000h to 0000 8FFFh</td><td colspan="2">—</td></tr><tr><td>0009 0000h to 000F FFFFh</td><td colspan="2">○</td></tr><tr><td>0010 0000h to 0011 FFFFh</td><td>—</td><td rowspan="10">○</td></tr><tr><td>0012 0000h to 007F 7FFFh</td><td>○</td></tr><tr><td>007F 8000h to 007F 9FFFh</td><td>—</td></tr><tr><td>007F A000h to 007F BFFFh</td><td>○</td></tr><tr><td>007F C000h to 007F C4FFh</td><td>—</td></tr><tr><td>007F C500h to 007F FBFFh</td><td>○</td></tr><tr><td>007F FC00h to 007F FFFFh</td><td rowspan="3">—</td></tr><tr><td>0080 0000h to 00DF FFFFh</td></tr><tr><td>00E0 0000h to 00FF FFFFh</td></tr><tr><td>0100 0000h to 07FF FFFFh</td><td colspan="2">[IA]</td></tr><tr><td>0800 0000h to 7FFF FFFFh</td><td colspan="2">○</td></tr><tr><td>8000 0000h to FEFF FFFFh</td><td>—</td><td>○</td></tr><tr><td>FF00 0000h to FFFF FFFFh</td><td>—</td><td>[IA]</td></tr></table></td><td>• Bus error (illegal address access)
<table><tr><th rowspan="2">Address</th><th colspan="2">On-chip ROM mode</th></tr><tr><th>Enabled</th><th>Disabled</th></tr><tr><td>0000 0000h to 0007 FFFFh</td><td colspan="2">—</td></tr><tr><td>0008 0000h to 0008 7FFFh</td><td colspan="2">—</td></tr><tr><td>0008 8000h to 0009 FFFFh</td><td colspan="2">Δ</td></tr><tr><td>000A 0000h to 000B FFFFh</td><td colspan="2">Δ</td></tr><tr><td>000C 0000h to 000D FFFFh</td><td colspan="2">Δ</td></tr><tr><td>000E 0000h to 000F FFFFh</td><td colspan="2">—</td></tr><tr><td>0010 0000h to 00FF FFFFh</td><td>Δ</td><td>○</td></tr><tr><td>0100 0000h to 07FF FFFFh</td><td colspan="2">[IA]</td></tr><tr><td>0800 0000h to 7FFF FFFFh</td><td colspan="2">○</td></tr><tr><td>8000 0000h to FEFF FFFFh</td><td>—</td><td>○</td></tr><tr><td>FF00 0000h to FFFF FFFFh</td><td>—</td><td>[IA]</td></tr></table></td></tr>
<tr><td>—</td><td>• Multiplexed bus function</td></tr>
<tr><td>• CSi control register (CSnCNT)
<table><tr><td>b0</td><td>EXENB</td><td>Operation enable bit</td></tr><tr><td>b4
b5</td><td>BSIZE[1:0]</td><td>External bus width select bits</td></tr><tr><td>b8</td><td>EMODE</td><td>Endian mode bit</td></tr><tr><td>b12</td><td>—</td><td>(Reserved bit)</td></tr></table>• BSIZE[1:0]
00b: 16-bit bus space selected
01b: (Setting prohibited)
10b: 8-bit bus space selected
11b: (Setting prohibited)</td><td>• CSn control register (CSnCR)
<table><tr><td>b0</td><td>EXENB</td><td>Operation enable bit</td></tr><tr><td>b4
b5</td><td>BSIZE[1:0]</td><td>External bus width select bits</td></tr><tr><td>b8</td><td>EMODE</td><td>Endian mode bit</td></tr><tr><td>b12</td><td>MPXEN</td><td>Address/data multiplexed I/O interface select bit</td></tr></table>• BSIZE[1:0]
00b: 16-bit bus space selected
01b: 32-bit bus space selected
10b: 8-bit bus space selected
11b: (Setting prohibited)</td></tr>
<tr><td>—</td><td>• CS recovery cycle insertion enable register (CSRECEN)</td></tr>
<tr><td>• CSi wait control register 1 (CSiWCNT1)</td><td>• CSn wait control register 1 (CSnWCR1)</td></tr>
<tr><td>• CSi wait control register 2 (CSiWCNT2)
<table><tr><td>b0
b2</td><td>CSROFF [2:0]</td><td>Read-access CS extension cycle select bits</td></tr><tr><td>b4
b5</td><td>CSWOFF [2:0]</td><td>Write-access CS extension cycle select bits</td></tr><tr><td>b8
b10</td><td>WDOFF[2:0]</td><td>Write data output extension cycle select bits</td></tr><tr><td>b12
b13</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b16
b18</td><td>RDON[2:0]</td><td>RD assert wait select bits</td></tr><tr><td>b20
b22</td><td>WRON[2:0]</td><td>WR assert wait select bits</td></tr><tr><td>b24
b26</td><td>WDON[2:0]</td><td>Write data output wait select bits</td></tr><tr><td>b28
b30</td><td>CSON[2:0]</td><td>CS assert wait select bits</td></tr></table></td><td>• CSn wait control register 2 (CSnWCR2)
<table><tr><td>b0
b2</td><td>CSROFF [2:0]</td><td>Read-access CS extension cycle select bits</td></tr><tr><td>b4
b5</td><td>CSWOFF [2:0]</td><td>Write-access CS extension cycle select bits</td></tr><tr><td>b8
b10</td><td>WDOFF[2:0]</td><td>Write data output extension cycle select bits</td></tr><tr><td>b12
b13</td><td>AWAIT[1:0]</td><td>Address cycle wait select bits</td></tr><tr><td>b16
b18</td><td>RDON[2:0]</td><td>RD assert wait select bits</td></tr><tr><td>b20
b22</td><td>WRON[2:0]</td><td>WR assert wait select bits</td></tr><tr><td>b24
b26</td><td>WDON[2:0]</td><td>Write data output wait select bits</td></tr><tr><td>b28
b30</td><td>CSON[2:0]</td><td>CS assert wait select bits</td></tr></table></td></tr>
<tr><td>• Bus error source clear register (BERCLR)
<table><tr><td>b0</td><td>STSCLR</td><td>Bus error source clear bit</td></tr><tr><td>b1
b7</td><td>—</td><td>(Reserved bits)</td></tr></table></td><td>• Bus error status clear register (BERCLR)
<table><tr><td>b0</td><td>STSCLR</td><td>Status clear bit</td></tr><tr><td>b1
b3</td><td>—</td><td>(Reserved bits)</td></tr></table></td></tr>
<tr><td rowspan="3">—</td><td>• Bus error status register 1 (BERSR1)</td></tr>
<tr><td>• Bus error status register 2 (BERSR2)</td></tr>
<tr><td>• Bus priority control register (BUSPRI)</td></tr>
<tr><td>• Bus error interrupt enable register (BERIE)</td><td>—</td></tr>
</table>

Table 2.15 Differences in Functions and Specifications (15)

<table>
<tr><th colspan="2">Item</th><th>RX610 Group</th><th>RX630 Group</th></tr>
<tr><td>Memory-protection unit</td><td>Register</td><td>—</td><td>• Region-n start page number register (RSPAGEn) (n = 0 to 7)
• Region-n end page number register (REPAGEn) (n = 0 to 7)
• Memory-protection enable register (MPEN)
• Background access control register (MPBAC)
• Memory-protection error status-clearing register (MPECLR)
• Memory-protection error status register (MPESTS)
• Data memory-protection error address register (MPDEA)
• Region search address register (MPSA)
• Region search operation register (MPOPS)
• Region invalidation operation register (MPOPI)
• Instruction-hit region register (MHITI)
• Data-hit region register (MHITD)</td></tr>
<tr><td>DMA controller</td><td>Functions</td><td>• Specification overview
<table><tr><td>Transfer space</td><td>4 GB</td></tr><tr><td>Maximum transfer byte count</td><td>64 MB</td></tr><tr><td>Single operand</td><td>Data count: 1, 2, 4, 8, 16, 32, 64, 128</td></tr><tr><td rowspan="6">Transfer system</td><td>Single operand transfer</td></tr><tr><td>Consecutive operand transfer</td></tr><tr><td>Nonstop transfer</td></tr><tr><td>—</td></tr><tr><td>—</td></tr><tr><td>—</td></tr><tr><td>Selective function</td><td>Reload function</td></tr><tr><td></td><td>—</td></tr></table></td><td>• Specification overview
<table><tr><td>Transfer space</td><td>512 MB</td></tr><tr><td>Maximum transfer data count</td><td>1 MB</td></tr><tr><td>Block size</td><td>Data count: 1 to 1024</td></tr><tr><td rowspan="6">Transfer system</td><td>—</td></tr><tr><td>—</td></tr><tr><td>—</td></tr><tr><td>Normal transfer mode</td></tr><tr><td>Repeat transfer mode</td></tr><tr><td>Block transfer mode</td></tr><tr><td rowspan="2">Selective function</td><td>—</td></tr><tr><td>Extended repeat area function</td></tr></table></td></tr>
<tr><td></td><td>Registers/ bits</td><td>• DMA mode register (DMMOD)
—
• DMA control register A (DMCRA)
<table><tr><td>b0
b5</td><td>DCTG[5:0]</td><td>DMA activation source select bits</td></tr><tr><td>b6
b7</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b8</td><td>DRLOD</td><td>Transfer destination address reload function select bit</td></tr><tr><td>b9</td><td>SRLOD</td><td>Transfer source address reload function select bit</td></tr><tr><td>b10</td><td>BRLOD</td><td>Transfer byte count reload function select bit</td></tr><tr><td>b11
b23</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b24
b25</td><td>DSEL[1:0]</td><td>Transfer system select bits</td></tr></table>• DMA control register B (DMCRB)
<table><tr><td>b0</td><td>DSCLR</td><td>DMAC internal status clear bit</td></tr><tr><td>b1
b9</td><td>—</td><td>(Reserved bits)</td></tr></table></td><td>—
• DMA source address register (DMSAR)
• DMA destination address register (DMDAR)
• DMA transfer count register (DMCRA)
<table><tr><td>b0
b15</td><td>DMCRAL</td><td>Lower bits of transfer count</td></tr><tr><td>b16
b25</td><td>DMCRAH</td><td>Upper bits of transfer count</td></tr></table>• DMA block transfer count register (DMCRB)
<table><tr><td>b0
b9</td><td>—</td><td>—</td></tr></table></td></tr>
</table>

Table 2.16 Differences in Functions and Specifications (16)

<table>
<tr><th colspan="2">Item</th><th>RX610 Group</th><th>RX630 Group</th></tr>
<tr><td rowspan="15">DMA controller</td><td rowspan="15">Registers/ bits</td><td>• DMA control register C (DMCRC)</td><td rowspan="11">—</td></tr>
<tr><td>• DMA control register D (DMCRD)</td></tr>
<tr><td>• DMA control register E (DMCRE)</td></tr>
<tr><td>• DMA current transfer source address register (DMCSA)</td></tr>
<tr><td>• DMA current transfer destination address register (DMCDA)</td></tr>
<tr><td>• DMA current transfer byte count register (DMCBC)</td></tr>
<tr><td>• DMA reload transfer source address register (DMRSA)</td></tr>
<tr><td>• DMA reload transfer destination address register (DMRDA)</td></tr>
<tr><td>• DMA reload transfer byte count register (DMRBC)</td></tr>
<tr><td>• DMA interrupt control register (DMICNT)</td></tr>
<tr><td>• DMA start register (DMSCNT)</td></tr>
<tr><td>• DMA arbitration status register (DMASTS)</td></tr>
<tr><td>• DMA transfer end detect register (DMEDET)</td></tr>
<tr><td rowspan="4">—</td><td>• DMA transfer mode register (DMTMD)
• DMA interrupt setting register (DMINT)
• DMA address mode register (DMAMD)
• DMA offset register (DMOFR)
• DMA transfer enable register (DMCNT)
• DMA software start register (DMREQ)
• DMA status register (DMSTS)
• DMA activation source flag control register (DMCSL)
• DMAC module activation register (DMAST)</td></tr>
<tr><td rowspan="3">DTC controller</td><td>Functions</td><td>• Priority relative to DMAC
DMAC > DTC</td><td>• Priority relative to DMACA
DMACA = DTC
Note: DMACA > DTC when DMACA and DTC are operating simultaneously</td></tr>
<tr><td rowspan="2">Registers/ bits</td><td>• DTC control register (DTCCR)
<table><tr><td>b0</td><td>ERR</td><td>Transfer stop flag</td></tr><tr><td>b3</td><td>RCHNE</td><td>Chain transfer enable after DTC repeat transfer bit</td></tr><tr><td>b4</td><td>RRS</td><td>DTC transfer data read skip enable bit</td></tr></table></td><td>• DTC control register (DTCCR)
<table><tr><td>b0</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b4</td><td>RRS</td><td>DTC transfer data read skip enable bit</td></tr></table></td></tr>
<tr><td>• DTC vector base register (DTCVBR)
The value of the lower 12 bits (b11 to b0) is fixed at 0, and writing to them has no effect.</td><td>• DTC vector base register (DTCVBR)
The lower 12 bits (b11 to b0) are read as 0. The write value should be 0.</td></tr>
<tr><td>—</td><td>• DTC status register (DTCSTS)</td></tr>
<tr><td rowspan="10">I/O port</td><td rowspan="10">Registers/ bits</td><td>• Data direction register (DDR)</td><td>• Port direction register (PDR)</td></tr>
<tr><td>• Data register (DR)</td><td>• Port output data register (PODR)</td></tr>
<tr><td>• Port register (PORT)</td><td>• Port input data register (PIDR)</td></tr>
<tr><td>• Input buffer control register (ICR)</td><td>• Port mode register (PMR)</td></tr>
<tr><td>• Pull-up resistor control register (PCR)</td><td>• Pull-up control register (PCR)</td></tr>
<tr><td>• Data direction register (DDR)</td><td>• Port direction register (PDR)</td></tr>
<tr><td>• Open drain control register (ODR)
<table><tr><td>b0</td><td>B0</td><td>Pm0 output type select bit</td></tr><tr><td>b1</td><td>B1</td><td>Pm1 output type select bit</td></tr><tr><td>b2</td><td>B2</td><td>Pm2 output type select bit</td></tr><tr><td>b3</td><td>B3</td><td>Pm3 output type select bit</td></tr><tr><td>b4</td><td>B4</td><td>Pm4 output type select bit</td></tr><tr><td>b5</td><td>B5</td><td>Pm5 output type select bit</td></tr><tr><td>b6</td><td>B6</td><td>Pm6 output type select bit</td></tr><tr><td>b7</td><td>B7</td><td>Pm7 output type select bit</td></tr></table></td><td>• Open drain control register 0 (ODR0)
<table><tr><td>b0</td><td>B0</td><td>Pm0 output type select bit</td></tr><tr><td>b1</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b2</td><td>B2</td><td>Pm1 output type select bit</td></tr><tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b4</td><td>B4</td><td>Pm2 output type select bit</td></tr><tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b6</td><td>B6</td><td>Pm3 output type select bit</td></tr><tr><td>b7</td><td>—</td><td>(Reserved bit)</td></tr></table></td></tr>
</table>

Table 2.17 Differences in Functions and Specifications (17)

<table>
<tr><th colspan="2">Item</th><th>RX610 Group</th><th>RX630 Group</th></tr>
<tr><td rowspan="11">I/O port</td><td rowspan="11">Registers/ bits</td><td rowspan="2">—</td><td>• Open drain control register 1 (ODR1)
<table><tr><td>b0</td><td>B0</td><td>Pm4 output type select bit</td></tr><tr><td>b2</td><td>B2</td><td>Pm5 output type select bit</td></tr><tr><td>b4</td><td>B4</td><td>Pm6 output type select bit</td></tr><tr><td>b6</td><td>B6</td><td>Pm7 output type select bit</td></tr></table></td></tr>
<tr><td>• Driving ability control register (DSCR)</td></tr>
<tr><td>• Port function control register 0 (PFCR0)</td><td rowspan="10">—</td></tr>
<tr><td>• Port function control register 1 (PFCR1)</td></tr>
<tr><td>• Port function control register 2 (PFCR2)</td></tr>
<tr><td>• Port function control register 3 (PFCR3)</td></tr>
<tr><td>• Port function control register 4 (PFCR4)</td></tr>
<tr><td>• Port function control register 5 (PFCR5)</td></tr>
<tr><td>• Port function control register 6 (PFCR6)</td></tr>
<tr><td>• Port function control register 7 (PFCR7)</td></tr>
<tr><td>• Port function control register 8 (PFCR8)</td></tr>
<tr><td>• Port function control register 9 (PFCR9)</td></tr>
<tr><td>Multi-function pin controller</td><td>Registers/ bits</td><td>—</td><td>• Write-protect register (PWPR)
• P0n pin function control register (P0nPFS)
• P1n pin function control register (P1nPFS)
• P2n pin function control register (P2nPFS)
• P3n pin function control register (P3nPFS)
• P4n pin function control register (P4nPFS)
• P5n pin function control register (P5nPFS)
• P6n pin function control register (P6nPFS)
• P7n pin function control register (P7nPFS)
• P8n pin function control register (P8nPFS)
• P9n pin function control register (P9nPFS)
• Pan pin function control register (PAnPFS)
• PBn pin function control register (PBnPFS)
• PCn pin function control register (PCnPFS)
• PDn pin function control register (PDnPFS)
• PEn pin function control register (PEnPFS)
• PFn pin function control register (PFnPFS)
• PJ3 pin function control register (PJ3PFS)
• PKn pin function control register (PKnPFS)
• CS output enable register (PFCSE)
• CS output pin select register 0 (PFCSS0)
• CS output pin select register 1 (PFCSS1)
• Address output enable register 0 (PFAOE0)
• Address output enable register 1 (PFAOE1)
• External bus control register 0 (PFBCR0)
• External bus control register 1 (PFBCR1)
• USB0 control register (PFUSB0)</td></tr>
</table>

Table 2.18 Differences in Functions and Specifications (18)

Item		RX610 Group	RX630 Group
Multi-function timer pulse unit 2	Registers/ bits	—	• Timer control register (TCR) • Timer mode register (TMDR) • Timer I/O control register (TIOR) • Timer compare match clear register (TCNTCMPCLR) • Timer interrupt enable register (TIER) • Timer status register (TSR) • Timer buffer operation transfer mode register (TBTM) • Timer input capture control register (TICCR) • Timer A/D converter start request control register (TADCR) • Timer A/D converter start request cycle set registers A and B (TADCORA and TADCORB) • Timer A/D converter start request cycle set buffer registers A and B (TADCOBRA and TADCOBRB) • Timer counter (TCNT) • Timer general register (TGR) • Timer start register (TSTR) • Timer synchronous register (TSYR) • Timer read/write enable register (TRWER) • Timer output master enable register (TOER) • Timer output control register 1 (TOCR1) • Timer output control register 2 (TOCR2) • Timer output level buffer register (TOLBR) • Timer gate control register (TGCR) • Timer subcounter (TCNTS) • Timer dead time data register (TDDR) • Timer cycle data register (TCDR) • Timer cycle buffer register (TCBR) • Timer interrupt skipping set register (TITCR) • Timer interrupt skipping counter (TITCNT) • Timer buffer transfer set register (TBTER) • Timer dead time enable register (TDER) • Timer waveform control register (TWCR) • Noise filter control register (NFCR)

Table 2.19 Differences in Functions and Specifications (19)

<table>
<tr><th colspan="2">Item</th><th>RX610 Group</th><th>RX630 Group</th></tr>
<tr><td rowspan="6">Port output enable 2</td><td rowspan="6">Registers/ bits</td><td rowspan="6">—</td><td>• Input level control/status register 1 (ICSR1)</td></tr>
<tr><td>• Output level control/status register 1 (OCSR1)</td></tr>
<tr><td>• Input level control/status register 2 (ICSR2)</td></tr>
<tr><td>• Software port output enable register (SPOER)</td></tr>
<tr><td>• Port output enable control register 1 (POECR1)</td></tr>
<tr><td>• Port output enable control register 2 (POECR2)</td></tr>
<tr><td rowspan="4">16-bit timer pulse unit</td><td>Functions</td><td>• Specification overview<table><tr><td>Pulse input/output</td><td>Max. 16</td></tr><tr><td>Channels 0, 3</td><td>Support for buffer operation setting</td></tr><tr><td>Channels 1, 2, 4, and 5</td><td>Support for independent setting of phase counting mode</td></tr><tr><td>Interrupt sources</td><td>26</td></tr></table></td><td>• Specification overview<table><tr><td>Pulse input/output</td><td>Max. 32 Unit 0: 16
Unit 1: 16</td></tr><tr><td>Channels 0, 3, 6, and 9</td><td>Support for buffer operation setting</td></tr><tr><td>Channels 1, 2, 4, 5, 7, 8, 10, and 11</td><td>Support for independent setting of phase counting mode</td></tr><tr><td>Interrupt sources</td><td>52 Unit 0: 26
Unit 1: 26</td></tr></table></td></tr>
<tr><td rowspan="3">Registers/ bits</td><td>• Timer status register (TSR)<table><tr><td>b0</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b1</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b2</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b4</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b7</td><td>TCFD</td><td>Count direction flag</td></tr></table></td><td>• Timer status register (TSR)<table><tr><td>b0</td><td>TGFA</td><td>Input capture/output compare flag A</td></tr><tr><td>b1</td><td>TGFB</td><td>Input capture/output compare flag B</td></tr><tr><td>b2</td><td>TGFC</td><td>Input capture/output compare flag C</td></tr><tr><td>b3</td><td>TGFD</td><td>Input capture/output compare flag D</td></tr><tr><td>b4</td><td>TCFV</td><td>Overflow flag</td></tr><tr><td>b5</td><td>TCFU</td><td>Underflow flag</td></tr><tr><td>b7</td><td>TCFD</td><td>Count direction flag</td></tr></table></td></tr>
<tr><td>• Timer start register (TSTRA, TSTRB)</td><td>• Timer start register (TSTR)</td></tr>
<tr><td>• Timer synchronous register (TSYRA, TSYRB)</td><td>• Timer synchronous register (TSYR)</td></tr>
<tr><td>—</td><td>• Noise filter control register (NFCR)</td></tr>
</table>

Table 2.20 Differences in Functions and Specifications (20)

Item		RX610 Group	RX630 Group
Programmable pulse generator	Registers/ bits	• PPG trigger select register (PTRSLR) • PTRSL 0: PPG1 trigger channels are TPU0 to TPU3. 1: PPG1 trigger channels are TPU6 to TPU9.	• PPG trigger select register (PTRSLR) • PTRSL 0: PPG1 trigger channels are MTU0 to MTU3 1: PPG1 trigger channels are TPU0 to TPU3
		• PPG output control register (PCR) PPG0.PCR • PCR.G0CMS[1:0] to G3CMS[1:0] 00b: Compare match in TPU0 01b: Compare match in TPU1 10b: Compare match in TPU2 11b: Compare match in TPU3 PPG1.PCR • PCR.G0CMS[1:0] to G3CMS[1:0] Value of PTRSL bit in PPG1.PTRSLR is 0. 00b: Compare match in TPU0 01b: Compare match in TPU1 10b: Compare match in TPU2 11b: Compare match in TPU3 Value of PTRSL bit in PPG1.PTRSLR is 1. 00b: Compare match in TPU6 01b: Compare match in TPU7 10b: Compare match in TPU8 11b: Compare match in TPU9	• PPG output control register (PCR) PPG0.PCR • PCR.G0CMS[1:0] to G3CMS[1:0] 00b: Compare match in MTU0 01b: Compare match in MTU1 10b: Compare match in MTU2 11b: Compare match in MTU3 PPG1.PCR • PCR.G0CMS[1:0] to G3CMS[1:0] Value of PTRSL bit in PPG1.PTRSLR is 0. 00b: Compare match in MTU0 01b: Compare match in MTU1 10b: Compare match in MTU2 11b: Compare match in MTU3 Value of PTRSL bit in PPG1.PTRSLR is 1. 00b: Compare match in TPU0 01b: Compare match in TPU1 10b: Compare match in TPU2 11b: Compare match in TPU3
		• PPG output mode register (PMR) PPG0.PMR • PMR.G0NOV to G3NOV 0: Normal operation (Output values updated on compare match A in the selected TPUm) 1: Non-overlapping operation (Output values updated on compare match A or B in the selected TPUm) PPG1.PMR • PMR.G0NOV to G3NOV 0: Normal operation (Output values updated on compare match A in the selected TPUm) 1: Non-overlapping operation (Output values updated on compare match A or B in the selected TPUm)	• PPG output mode register (PMR) PPG0.PMR • PMR.G0NOV to G3NOV 0: Normal operation (Output values updated on compare match A in the selected MTUn) 1: Non-overlapping operation (Output values updated on compare match A or B in the selected MTUn) PPG1.PMR • PMR.G0NOV to G3NOV Value of PTRSL bit in PPG1.PTRSLR is 0. 0: Normal operation (Output values updated on compare match A in the selected MTUn) 1: Non-overlapping operation (Output values updated on compare match A or B in the selected MTUn) Value of PTRSL bit in PPG1.PTRSLR is 1. 0: Normal operation (Output values updated on compare match A in the selected TPUn) 1: Non-overlapping operation (Output values updated on compare match A or B in the selected TPUn)

Table 2.21 Differences in Functions and Specifications (21)

<table>
<tr><th colspan="2">Item</th><th>RX610 Group</th><th>RX630 Group</th></tr>
<tr><td rowspan="27">Realtime clock</td><td rowspan="27">Registers/ bits</td><td rowspan="27">—</td><td>• 64 Hz Counter (R64CNT)</td></tr>
<tr><td>• Second counter (RSECCNT)</td></tr>
<tr><td>• Minute counter (RMINCNT)</td></tr>
<tr><td>• Hour counter (RHRCNT)</td></tr>
<tr><td>• Day-of-week counter (RWKCNT)</td></tr>
<tr><td>• Date counter (RDAYCNT)</td></tr>
<tr><td>• Month counter (RMONCNT)</td></tr>
<tr><td>• Year counter (RYRCNT)</td></tr>
<tr><td>• Second alarm register (RSECAR)</td></tr>
<tr><td>• Minute alarm register (RMINAR)</td></tr>
<tr><td>• Hour alarm register (RHRAR)</td></tr>
<tr><td>• Day-of-week alarm register (RWKAR)</td></tr>
<tr><td>• Date alarm register (RDAYAR)</td></tr>
<tr><td>• Month alarm register (RMONAR)</td></tr>
<tr><td>• Year alarm register (RYRAR)</td></tr>
<tr><td>• Year alarm enable register (RYRAREN)</td></tr>
<tr><td>• RTC control register 1 (RCR1)</td></tr>
<tr><td>• RTC control register 2 (RCR2)</td></tr>
<tr><td>• RTC control register 3 (RCR3)</td></tr>
<tr><td>• RTC control register 4 (RCR4)</td></tr>
<tr><td>• Frequency register H/L (RFRH/L)</td></tr>
<tr><td>• Time error adjustment register (RADJ)</td></tr>
<tr><td>• Time capture control register y (RTCCRy)</td></tr>
<tr><td>• Second capture register y (RSECCPy)</td></tr>
<tr><td>• Minute capture register y (RMINCPy)</td></tr>
<tr><td>• Hour capture register y (RHRCPy)</td></tr>
<tr><td>• Date capture register y (RDAYCPy)</td></tr>
<tr><td>• Month capture register y (RMONCPy)</td></tr>
<tr><td rowspan="12">Watchdog timer</td><td>Functions</td><td>• Specification overview<table><tr><td>Number of bits</td><td>8</td></tr><tr><td>Operating modes</td><td>Watchdog timer mode</td></tr><tr><td></td><td>Interval timer mode</td></tr><tr><td>Operation start mode</td><td>—</td></tr><tr><td></td><td>Register start mode</td></tr><tr><td>—</td><td>—</td></tr><tr><td>Output signals</td><td>WDTOVF# signal output (external)</td></tr><tr><td></td><td>Reset signal (internal)</td></tr><tr><td></td><td>Interval timer interrupt</td></tr></table></td><td>• Specification overview<table><tr><td>Number of bits</td><td>14</td></tr><tr><td>Operating modes</td><td>Watchdog timer mode</td></tr><tr><td></td><td>—</td></tr><tr><td>Operation start mode</td><td>Auto-start mode</td></tr><tr><td></td><td>Register start mode</td></tr><tr><td>Window function</td><td>Support for setting window start and end positions</td></tr><tr><td>Output signals</td><td>—</td></tr><tr><td></td><td>Reset signal (internal)</td></tr><tr><td></td><td>Interrupt request signal</td></tr></table></td></tr>
<tr><td rowspan="11">Registers/ bits</td><td>• Timer counter (TCNT)</td><td rowspan="5">—</td></tr>
<tr><td>• Timer control/status register (TCSR)</td></tr>
<tr><td>• Reset control/status register (RSTCSR)</td></tr>
<tr><td>• Write window A register (WINA)</td></tr>
<tr><td>• Write window B register (WINB)</td></tr>
<tr><td rowspan="6">—</td><td>• WDT refresh register (WDTRR)</td></tr>
<tr><td>• WDT control register (WDTCR)</td></tr>
<tr><td>• WDT status register (WDTSR)</td></tr>
<tr><td>• WDT reset control register (WDTRCR)</td></tr>
<tr><td rowspan="5">Independent watchdog timer</td><td rowspan="5">Registers/ bits</td><td rowspan="5">—</td><td>• IWDT refresh register (IWDTRR)</td></tr>
<tr><td>• IWDT control register (IWDTCR)</td></tr>
<tr><td>• IWDT status register (IWDTSR)</td></tr>
<tr><td>• IWDT reset control register (IWDTRCR)</td></tr>
<tr><td>• IWDT count stop control register (IWDTCSTPR)</td></tr>
</table>

Table 2.22 Differences in Functions and Specifications (22)

Item		RX610 Group	RX630 Group
USB 2.0 function module	Registers/ bits	—	• System configuration control register (SYSCFG) • System configuration status register 0 (SYSSTS0) • Device state control register 0 (DVSTCTR0) • CFIFO port register (CFIFO) • D0FIFO port register (D0FIFO) • D1FIFO port register (D1FIFO) • CFIFO port select register (CFIFOSEL) • D0FIFO port select register (D0FIFOSEL) • D1FIFO port select register (D1FIFOSEL) • CFIFO port control register (CFIFOCTR) • D0FIFO port control register (D0FIFOCTR) • D1FIFO port control register (D1FIFOCTR) • Interrupt enable register 0 (INTENB0) • BRDY interrupt enable register (BRDYENB) • NRDY interrupt enable register (NRDYENB) • BEMP interrupt enable register (BEMPENB) • SOF output configuration register (SOFCFG) • Interrupt status register 0 (INTSTS0) • BRDY interrupt status register (BRDYSTS) • NRDY interrupt status register (NRDYSTS) • BEMP interrupt status register (BEMPSTS) • Frame number register (FRMNUM) • Device state changing register (DVCHGR) • USB address register (USBADDR) • USB request type register (USBREQ) • USB request value register (USBVAL) • USB request index register (USBINDX) • USB request length register (USBLENG) • DCP maximum packet size register (DCPMAXP) • DCP control register (DCPCTR) • Pipe window select register (PIPESEL) • Pipe configuration register (PIPECFG) • Pipe maximum packet size register (PIPEMAXP) • Pipe cycle control register (PIPEPERI) • PIPEn control register (PIPEnCTR) • PIPEn transaction counter enable register (PIPEnTRE) • PIPEn transaction counter register (PIPEnTRN) • Deep standby USB transceiver control/pin monitor register (DPUSR0R) • Deep standby USB suspend/resume interrupt register (DPUSR1R)

Table 2.23 Differences in Functions and Specifications (23)

<table>
<tr><th colspan="2">Item</th><th>RX610 Group</th><th>RX630 Group</th></tr>
<tr><td rowspan="5">Serial communications interface</td><td>Functions</td><td>• SCI
<table><tr><td rowspan="6">Serial communication modes</td><td>Asynchronous</td></tr><tr><td>Clock synchronous</td></tr><tr><td>Smart card interface</td></tr><tr><td>—</td></tr><tr><td>—</td></tr><tr><td>TMR clock input</td></tr></table></td><td>• SCIc
<table><tr><td rowspan="6">Serial communication modes</td><td>Asynchronous</td></tr><tr><td>Clock synchronous</td></tr><tr><td>Smart card interface</td></tr><tr><td>Simple I²C bus</td></tr><tr><td>Simple SPI bus</td></tr><tr><td>TMR clock input</td></tr><tr><td rowspan="2">Hardware flow control</td><td>Asynchronous</td></tr><tr><td>Clock synchronous</td></tr></table>• SCId
<table><tr><td rowspan="6">Serial communication modes</td><td>Asynchronous</td></tr><tr><td>Clock synchronous</td></tr><tr><td>Smart card interface</td></tr><tr><td>Simple I²C bus</td></tr><tr><td>Simple SPI bus</td></tr><tr><td>TMR clock input</td></tr><tr><td rowspan="2">Hardware flow control</td><td>Asynchronous</td></tr><tr><td>Clock synchronous</td></tr><tr><td>Extended serial mode</td><td>Start frame transmission/reception</td></tr></table></td></tr>
<tr><td>Registers/ bits</td><td>• Serial mode register (SMR)
<table><tr><td>b0
b1</td><td>CKS[1:0]</td><td>Clock select bits</td></tr><tr><td>b2</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b3</td><td>STOP</td><td>Stop bit length select bit</td></tr><tr><td>b4</td><td>PM</td><td>Parity mode bit</td></tr><tr><td>b5</td><td>PE</td><td>Parity enable bit</td></tr><tr><td>b6</td><td>CHR</td><td>Character length bit</td></tr><tr><td>b7</td><td>CM</td><td>Communications mode bit</td></tr></table></td><td>• Serial mode register (SMR)
<table><tr><td>b0
b1</td><td>CKS[1:0]</td><td>Clock select bits</td></tr><tr><td>b2</td><td>MP</td><td>Multi-processor mode bit</td></tr><tr><td>b3</td><td>STOP</td><td>Stop bit length bit</td></tr><tr><td>b4</td><td>PM</td><td>Parity mode bit</td></tr><tr><td>b5</td><td>PE</td><td>Parity enable bit</td></tr><tr><td>b6</td><td>CHR</td><td>Character length bit</td></tr><tr><td>b7</td><td>CM</td><td>Communications mode bit</td></tr></table></td></tr>
<tr><td></td><td>• Serial control register (SCR)
<table><tr><td>b0
b1</td><td>CKE[1:0]</td><td>Clock enable bits</td></tr><tr><td>b2</td><td>TEIE</td><td>Transmit end interrupt enable bit</td></tr><tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b4</td><td>RE</td><td>Receive enable bit</td></tr><tr><td>b5</td><td>TE</td><td>Transmit enable bit</td></tr><tr><td>b6</td><td>RIE</td><td>Receive interrupt enable bit</td></tr><tr><td>b7</td><td>TIE</td><td>Transmit end interrupt enable bit</td></tr></table></td><td>• Serial control register (SCR)
<table><tr><td>b0
b1</td><td>CKE[1:0]</td><td>Clock enable bits</td></tr><tr><td>b2</td><td>TEIE</td><td>Transmit end interrupt enable bit</td></tr><tr><td>b3</td><td>MPIE</td><td>Multi-processor interrupt enable bit</td></tr><tr><td>b4</td><td>RE</td><td>Receive enable bit</td></tr><tr><td>b5</td><td>TE</td><td>Transmit enable bit</td></tr><tr><td>b6</td><td>RIE</td><td>Receive interrupt enable bit</td></tr><tr><td>b7</td><td>TIE</td><td>Transmit interrupt enable bit</td></tr></table></td></tr>
<tr><td></td><td>• Serial status register (SSR)
<table><tr><td>b0</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b1</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b2</td><td>TEND</td><td>Transmit end flag</td></tr><tr><td>b3</td><td>PER</td><td>Parity error flag</td></tr><tr><td>b4</td><td>FER</td><td>Framing error flag</td></tr><tr><td>b5</td><td>ORER</td><td>Overrun error flag</td></tr><tr><td>b6</td><td>RDRF</td><td>Receive data full flag</td></tr><tr><td>b7</td><td>TDRE</td><td>Transmit data empty flag</td></tr></table></td><td>• Serial status register (SSR)
<table><tr><td>b0</td><td>MPBT</td><td>Multi-processor bit transfer bit</td></tr><tr><td>b1</td><td>MPB</td><td>Multi-processor bit</td></tr><tr><td>b2</td><td>TEND</td><td>Transmit end flag</td></tr><tr><td>b3</td><td>PER</td><td>Parity error flag</td></tr><tr><td>b4</td><td>FER</td><td>Framing error flag</td></tr><tr><td>b5</td><td>ORER</td><td>Overrun error flag</td></tr><tr><td>b6</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b7</td><td>—</td><td>(Reserved bit)</td></tr></table></td></tr>
<tr><td></td><td>• Smart card mode register (SCMR)
<table><tr><td>b0</td><td>SMIF</td><td>Smart card interface mode select bit</td></tr><tr><td>b2</td><td>SINV</td><td>Transmitted/received data invert bit</td></tr><tr><td>b3</td><td>SDIR</td><td>Transmitted/received data transfer direction bit</td></tr><tr><td>b7</td><td>BCP2</td><td>Base clock pulse bit 2</td></tr></table></td><td>• Smart card mode register (SCMR)
<table><tr><td>b0</td><td>SMIF</td><td>Smart card interface mode select bit</td></tr><tr><td>b2</td><td>SINV</td><td>Smart card data invert bit</td></tr><tr><td>b3</td><td>SDIR</td><td>Bit order select bit</td></tr><tr><td>b7</td><td>BCP2</td><td>Base clock pulse bit 2</td></tr></table></td></tr>
<tr><td></td><td>• Serial extended mode register (SEMR)
<table><tr><td>b0</td><td>ACS0</td><td>Asynchronous mode clock source select bit</td></tr><tr><td>b4</td><td>ABCS</td><td>Asynchronous mode base clock select bit</td></tr><tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr></table></td><td>• Serial extended mode register (SEMR)
<table><tr><td>b0</td><td>ACS0</td><td>Asynchronous mode clock source select bit</td></tr><tr><td>b4</td><td>ABCS</td><td>Asynchronous mode base clock select bit</td></tr><tr><td>b5</td><td>NFEN</td><td>Digital noise filter function enable bit</td></tr></table></td></tr>
</table>

Table 2.24 Differences in Functions and Specifications (24)

<table>
<tr><th colspan="2">Item</th><th>RX610 Group</th><th>RX630 Group</th></tr>
<tr><td>Serial communications interface</td><td>Registers/ bits</td><td>—</td><td>• Noise filter setting register (SNFR)
• I²C mode register 1 (SIMR1)
• I²C mode register 2 (SIMR2)
• I²C mode register 3 (SIMR3)
• I²C status mode register (SISR)
• SPI mode register (SPMR)
• Extended serial module enable register (ESMER)
• Control register 0 (CR0)
• Control register 1 (CR1)
• Control register 2 (CR2)
• Control register 3 (CR3)
• Port control register (PCR)
• Interrupt control register (ICR)
• Status register (STR)
• Status clear register (STCR)
• Control field 0 data register (CF0DR)
• Control field 0 compare enable register (CF0CR)
• Control field 0 receive data register (CF0RR)
• Primary control field 1 data register (PCF1DR)
• Secondary control field 1 data register (SCF1DR)
• Control field 1 compare enable register (CF1CR)
• Control field 1 receive data register (CF1RR)
• Timer control register (TCR)
• Timer mode register (TMR)
• Timer prescaler register (TPRE)
• Timer count register (TCNT)</td></tr>
<tr><td rowspan="2">I²C bus interface</td><td>Functions</td><td>• Specification overview<table><tr><td>Usage notes</td><td>Setting input buffer control register</td></tr><tr><td></td><td>Timings for writing and outputting of transmit acknowledge bit</td></tr><tr><td></td><td>Restrictions on timings for stop condition issuance request and transmit data writing in master transmitter mode</td></tr><tr><td></td><td>Notes when communication is restarted with the NACK reception in master mode</td></tr><tr><td></td><td>Notes on the RDRF flag set timing selection bit (RDRFS)</td></tr><tr><td></td><td>—</td></tr></table></td><td>• Specification overview<table><tr><td>Usage notes</td><td>—</td></tr><tr><td></td><td>—</td></tr><tr><td></td><td>—</td></tr><tr><td></td><td>—</td></tr><tr><td></td><td>—</td></tr><tr><td></td><td>Points to note on starting transfer</td></tr></table></td></tr>
<tr><td>Registers/ bits</td><td>• I²C bus mode register 3 (ICMR3)<table><tr><td>b0
b1</td><td>NF[1:0]</td><td>Noise filter stage selection bits</td></tr><tr><td>b2</td><td>ACKBR</td><td>Receive acknowledge bit</td></tr><tr><td>b3</td><td>ACKBT</td><td>Transmit acknowledge bit</td></tr><tr><td>b4</td><td>ACKWP</td><td>ACKBT write protect bit</td></tr><tr><td>b5</td><td>RDRFS</td><td>RDRF flag set timing selection bit</td></tr><tr><td>b6</td><td>WAIT</td><td>Wait bit</td></tr><tr><td>b7</td><td>SMBS</td><td>SMBus/I²C bus selection bit</td></tr></table>• NF[1:0]
00b: Noise up to 1-PCLK is filtered out.
01b: Noise up to 2-PCLK is filtered out.
10b: Noise up to 3-PCLK is filtered out.
11b: Noise up to 4-PCLK is filtered out.</td><td>• I²C bus mode register 3 (ICMR3)<table><tr><td>b0
b1</td><td>NF[1:0]</td><td>Noise filter stage selection bits</td></tr><tr><td>b2</td><td>ACKBR</td><td>Receive acknowledge bit</td></tr><tr><td>b3</td><td>ACKBT</td><td>Transmit acknowledge bit</td></tr><tr><td>b4</td><td>ACKWP</td><td>ACKBT write protect bit</td></tr><tr><td>b5</td><td>RDRFS</td><td>RDRF flag set timing selection bit</td></tr><tr><td>b6</td><td>WAIT</td><td>Wait bit</td></tr><tr><td>b7</td><td>SMBS</td><td>SMBus/I²C bus selection bit</td></tr></table>• NF[1:0]
00b: Noise up to 1-IICϕ is filtered out.
01b: Noise up to 2-IICϕ is filtered out.
10b: Noise up to 3-IICϕ is filtered out.
11b: Noise up to 4-IICϕ is filtered out.</td></tr>
</table>

Table 2.25 Differences in Functions and Specifications (25)

Item		RX610 Group	RX630 Group
CAN module	Registers/ bits	—	• Control register (CTLR) • Bit configuration register (BCR) • Mask register k (MKRk) • FIFO received ID compare registers 0 and 1 (FIDCR0 and FIDCR1) • Mask invalid register (MKIVLR) • Mailbox register j (MBj) • Mailbox interrupt enable register (MIER) • Message control register j (MCTLj) • Receive FIFO control register (RFCR) • Receive FIFO pointer control register (RFPCR) • Transmit FIFO control register (TFCR) • Transmit FIFO pointer control register (TFPCR) • Status register (STR) • Mailbox search mode register (MSMR) • Mailbox search status register (MSSR) • Channel search support register (CSSR) • Acceptance filter support register (AFSR) • Error interrupt enable register (EIER) • Error interrupt factor judge register (EIFR) • Receive error count register (RECR) • Transmit error count register (TECR) • Error code store register (ECSR) • Time stamp register (TSR) • Test control register (TCR)
Serial peripheral interface	Registers/ bits	—	• RSPI control register (SPCR) • RSPI slave select polarity register (SSLP) • RSPI pin control register (SPPCR) • RSPI status register (SPSR) • RSPI data register (SPDR) • RSPI sequence control register (SPSCR) • RSPI sequence status register (SPSSR) • RSPI bit rate register (SPBR) • RSPI data control register (SPDCR) • RSPI clock delay register (SPCKD) • RSPI slave select negation delay register (SSLND) • RSPI next-access delay register (SPND) • RSPI control register 2 (SPCR2) • RSPI command registers 0 to 7 (SPCMD0 to SPCMD7)

Table 2.26 Differences in Functions and Specifications (26)

Item		RX610 Group	RX630 Group
IEBus™ controller	Registers/ bits	—	• IEBus control register (IECTR)
			• IEBus command register (IECMR)
			• IEBus master control register (IEMCR)
			• IEBus master unit address register 1 (IEAR1)
			• IEBus master unit address register 2 (IEAR2)
			• IEBus slave address setting register 1 (IESA1)
			• IEBus slave address setting register 2 (IESA2)
			• IEBus transmit message length register (IETBFL)
			• IEBus reception master address register 1 (IEMA1)
			• IEBus reception master address register 2 (IEMA2)
			• IEBus receive control field register (IERCTL)
			• IEBus receive message length register (IERBFL)
			• IEBus lock address register 1 (IELA1)
			• IEBus lock address register 2 (IELA2)
			• IEBus general flag register (IEFLG)
			• IEBus transmit status register (IETSR)
			• IEBus transmit interrupt enable register (IEIET)
			• IEBus receive status register (IERSR)
			• IEBus receive interrupt enable register (IEIER)
			• IEBus clock selection register (IECKSR)
			• IEBus transmit data buffer registers 001 to 032 (IETB001 to IETB032)
			• IEBus receive data buffer registers 001 to 032 (IERB001 to IERB032)
12-bit A/D converter	Registers/ bits	—	• A/D control register (ADCSR)
			• A/D channel select register 0 (ADANS0)
			• A/D channel select register 1 (ADANS1)
			• A/D-converted value addition mode select register 0 (ADADS0)
			• A/D-converted value addition mode select register 1 (ADADS1)
			• A/D-converted value addition count select register (ADADC)
			• A/D control extended register (ADCER)
			• A/D start trigger select register (ADSTRGR)
			• A/D-converted extended input control register (ADEXICR)
			• A/D temperature sensor data register (ADTSDR)
			• A/D internal reference voltage data register (ADOCDR)
			• A/D data register y (ADDRy)
			• A/D sampling state register 01 (ADSSTR01)
			• A/D sampling state register 23 (ADSSTR23)

Table 2.27 Differences in Functions and Specifications (27)

<table>
<tr><th colspan="2">Item</th><th>RX610 Group</th><th>RX630 Group</th></tr>
<tr><td rowspan="2">10-bit A/D converter</td><td>Functions</td><td>• Specification overview
<table>
<tr><td>Input channels</td><td>(1 unit × 4 channels) × 4</td></tr>
<tr><td rowspan="8">Start triggers</td><td>Software trigger</td></tr>
<tr><td>TPU</td></tr>
<tr><td>—</td></tr>
<tr><td>TMR</td></tr>
<tr><td>External trigger (ADTRG0# pin)</td></tr>
<tr><td>External trigger (ADTRG1# pin)</td></tr>
<tr><td>External trigger (ADTRG2# pin)</td></tr>
<tr><td>External trigger (ADTRG3# pin)</td></tr>
<tr><td rowspan="3">Functions</td><td>Sample-and-hold function</td></tr>
<tr><td>Adjustable number of sampling states</td></tr>
<tr><td>—</td></tr>
</table></td><td>• Specification overview
<table>
<tr><td>Input channels</td><td>1 unit × 8 channels + 1 extended channel</td></tr>
<tr><td rowspan="8">Start triggers</td><td>Software trigger</td></tr>
<tr><td>TPU</td></tr>
<tr><td>MTU</td></tr>
<tr><td>TMR</td></tr>
<tr><td>External trigger (ADTRG# pin)</td></tr>
<tr><td>—</td></tr>
<tr><td>—</td></tr>
<tr><td>—</td></tr>
<tr><td rowspan="3">Functions</td><td>Sample-and-hold function</td></tr>
<tr><td>Adjustable number of sampling states</td></tr>
<tr><td>10-bit A/D converter self-diagnostic function</td></tr>
</table></td></tr>
<tr><td>Registers/ bits</td><td>• A/D data register A to D (ADDRA to ADDRD)
—
• A/D control / status register (ADCSR)
<table>
<tr><td>b0
b3</td><td>CH[3:0]</td><td>Channel select bits</td></tr>
<tr><td>b5</td><td>ADST</td><td>A/D start bit</td></tr>
<tr><td>b6</td><td>ADIE</td><td>A/D interrupt enable bit</td></tr>
</table>
• AD0.ADCSR.CH[3:0]
0000b: AN0 (single mode) / AN0 (scan mode)
0001b: AN1 (single mode) / AN0 and AN1 (scan mode)
0010b: AN2 (single mode) / AN0 to AN2 (scan mode)
0011b: AN3 (single mode) / AN0 to AN3 (scan mode)
• AD1.ADCSR.CH[3:0]
0000b: AN4 (single mode) / AN4 (scan mode)
0001b: AN5 (single mode) / AN4 and AN5 (scan mode)
0010b: AN6 (single mode) / AN4 to AN6 (scan mode)
0011b: AN7 (single mode) / AN4 to AN7 (scan mode)
• AD2.ADCSR.CH[3:0]
0000b: AN8 (single mode) / AN8 (scan mode)
0001b: AN9 (single mode) / AN8 and AN9 (scan mode)
0010b: AN10 (single mode) / AN8 to AN10 (scan mode)
0011b: AN11 (single mode) / AN8 to AN11 (scan mode)
• AD3.ADCSR.CH[3:0]
0000b: AN12 (single mode) / AN12 (scan mode)
0001b: AN13 (single mode) / AN12 and AN13 (scan mode)
0010b: AN14 (single mode) / AN12 to AN14 (scan mode)
0011b: AN15 (single mode) / AN12 to AN15 (scan mode)</td><td>• A/D data register A to D (ADDRA to ADDRD)
• A/D data register E to H (ADDRE to ADDRH)
• A/D control / status register (ADCSR)
<table>
<tr><td>b0
b2</td><td>CH[2:0]</td><td>Channel select bits</td></tr>
<tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b5</td><td>ADST</td><td>A/D start bit</td></tr>
<tr><td>b6</td><td>ADIE</td><td>A/D interrupt enable bit</td></tr>
</table>
• ADCSR.CH[2:0]
000b: AN0 (single mode) / AN0 (scan mode)
001b: AN1 (single mode) / AN0 and AN1 (scan mode)
010b: AN2 (single mode) / AN0 to AN2 (scan mode)
011b: AN3 (single mode) / AN0 to AN3 (scan mode)
100b: AN4 (single mode) / AN0 to AN4 (scan mode)
101b: AN5 (single mode) / AN0 to AN5 (scan mode)
110b: AN6 (single mode) / AN0 to AN6 (scan mode)
111b: AN7 (single mode) / AN0 to AN7 (scan mode)</td></tr>
</table>

Table 2.28 Differences in Functions and Specifications (28)

<table>
<tr><th colspan="2">Item</th><th>RX610 Group</th><th>RX630 Group</th></tr>
<tr><td rowspan="4">10-bit A/D converter</td><td rowspan="4">Registers/ bits</td><td>• A/D control register (ADCR)
<table><tr><td>b0
b1</td><td>MODE[1:0]</td><td>Operation mode select bits</td></tr><tr><td>b2
b3</td><td>CKS[1:0]</td><td>Clock select bits</td></tr><tr><td>b5
b7</td><td>TRGS[2:0]</td><td>Trigger select bits</td></tr></table>• AD0.ADCR.TGRS[2:0]
000b: Software trigger
001b: Compare-match/input-capture A signals from TPU0 to TPU5
010b: Compare-match A signal from TMR0
011b: A/D conversion start trigger pin (ADTRG0# pin)
100b: Compare-match/input-capture A signal from TPU0
101b: Compare-match/input-capture A signals from TPU6 to TPU11
110b: (Setting prohibited)
111b: (Setting prohibited)
• AD1.ADCR.TGRS[2:0]
000b: Software trigger
001b: Compare-match/input-capture A signals from TPU0 to TPU5
010b: Compare-match A signal from TMR0
011b: A/D conversion start trigger pin (ADTRG1# pin)
100b: Compare-match/input-capture B signal from TPU0
101b: Compare-match/input-capture A signals from TPU6 to TPU11
110b: (Setting prohibited)
111b: A/D conversion start trigger pin (ADTRG0# pin)
• AD2.ADCR.TGRS[2:0]
000b: Software trigger
001b: Compare-match/input-capture A signals from TPU0 to TPU5
010b: Compare-match A signal from TMR2
011b: A/D conversion start trigger pin (ADTRG2# pin)
100b: Compare-match/input-capture C signal from TPU0
101b: Compare-match/input-capture A signals from TPU6 to TPU11
110b: (Setting prohibited)
111b: (Setting prohibited)
• AD3.ADCR.TGRS[2:0]
000b: Software trigger
001b: Compare-match/input-capture A signals from TPU0 to TPU5
010b: Compare-match A signal from TMR2
011b: A/D conversion start trigger pin (ADTRG3# pin)
100b: Compare-match/input-capture D signal from TPU0
101b: Compare-match/input-capture A signals from TPU6 to TPU11
110b: (Setting prohibited)
111b: A/D conversion start trigger pin (ADTRG2# pin)</td><td>• A/D control register (ADCR)
<table><tr><td>b0
b1</td><td>MODE[1:0]</td><td>Operation mode select bits</td></tr><tr><td>b2
b3</td><td>CKS[1:0]</td><td>Clock select bits</td></tr><tr><td>b5
b7</td><td>TRGS[2:0]</td><td>Trigger select bits</td></tr></table>• ADCR.TRGS[2:0]
000b: Software trigger
001b: Compare-match/input-capture A signals from MTU0 to MTU4
010b: Compare-match signal from TMR0
011b: A/D conversion start trigger pin (ADTRG# pin)
100b: Compare-match/input-capture A signal from MTU0
101b: Compare-match/input-capture A signals from TPU0 to TPU4
110b: Compare-match signal from MTU4
111b: Compare-match/input-capture A signal from TPUA0</td></tr>
<tr><td>• ADDRy format select register (ADDPR)
<table><tr><td>b4
b5</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b6</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b7</td><td>DPSEL</td><td>ADDRy format select bit</td></tr></table></td><td>• A/D control register 2 (ADCR2)
<table><tr><td>b4
b5</td><td>EXSEL[1:0]</td><td>Extended analog input select bits</td></tr><tr><td>b6</td><td>EXOEN</td><td>Extended analog output control bit</td></tr><tr><td>b7</td><td>DPSEL</td><td>ADDRy format select bit</td></tr></table></td></tr>
<tr><td>—</td><td>• A/D self-diagnostic register (ADDIAGR)</td></tr>
<tr><td rowspan="2">D/A converter</td><td>Functions</td><td>• Specification overview
<table><tr><td>—</td><td>—</td></tr></table></td><td>• Specification overview
<table><tr><td>Countermeasure against interference from analog modules</td><td>Countermeasure against interference between D/A and A/D converters*</td></tr></table>Note: This function is not implemented in products with on-chip ROM capacity of 1.5 MB or more or with 176 pins or more.</td></tr>
<tr><td>Registers/ bits</td><td>—</td><td>• D/A A/D synchronous start control register (DAADSCR)</td></tr>
<tr><td>Temperature sensor</td><td>Registers/ bits</td><td>—</td><td>• Temperature sensor control register (TSCR)</td></tr>
</table>

Table 2.29 Differences in Functions and Specifications (29)

<table>
<tr><th colspan="2">Item</th><th>RX610 Group</th><th>RX630 Group</th></tr>
<tr><td rowspan="3">Flash memory for code storage</td><td>Functions</td><td>• Specification overview<table><tr><td>Write unit</td><td>256-byte units</td></tr><tr><td rowspan="6">Block structure</td><td>—</td></tr><tr><td>8 KB × 8 blocks</td></tr><tr><td>—</td></tr><tr><td>—</td></tr><tr><td>64 KB × 9 blocks</td></tr><tr><td>128 KB × 11 blocks (max)</td></tr><tr><td>BG0 (background operation) function</td><td>• Programs located in the ROM area can be executed during data flash program or erase operations.
• The CPU can execute programs located in areas other than the ROM or data flash areas during ROM program or erase operations.</td></tr><tr><td rowspan="4">On-board programming</td><td>Boot mode</td></tr><tr><td>—</td></tr><tr><td>User boot mode</td></tr><tr><td>User program</td></tr><tr><td>Off-board programming</td><td>The user MAT and user boot MAT areas can be programmed using a PROM writer.</td></tr><tr><td>Protection functions</td><td>Error protection</td></tr></table></td><td>• Specification overview<table><tr><td>Program unit</td><td>128-byte units</td></tr><tr><td rowspan="6">Block structure</td><td>4 KB × 8 blocks</td></tr><tr><td>—</td></tr><tr><td>16 KB × 30 blocks (max)</td></tr><tr><td>32 KB × 16 blocks (max)</td></tr><tr><td>64 KB × 16 blocks (max)</td></tr><tr><td>—</td></tr><tr><td>BG0 (background operation) function</td><td>The CPU can execute programs in the ROM area during E2 data flash P/E operations.</td></tr><tr><td rowspan="4">On-board programming</td><td>Boot mode</td></tr><tr><td>USB boot mode</td></tr><tr><td>User boot mode</td></tr><tr><td>User program</td></tr><tr><td>Off-board programming</td><td>The user area and the user boot area can be programmed using a Flash programmer.</td></tr><tr><td>Protection functions</td><td>Command-locked state</td></tr></table></td></tr>
<tr><td>Registers/ bits</td><td>• Flash status register 1 (FSTATR1)
• b1 to b0: Reserved bits
The read value is undefined. Writing to these bits has no effect.
• b7: FCU error bit</td><td>• Flash status register 1 (FSTATR1)
• b1 to b0: Reserved bits
These bits are read as 0. Writing to them has no effect.
• b7: FCU error flag</td></tr>
<tr><td>• Flash P/E mode entry register (FENTRYR)<table><tr><td>b0</td><td>FENTRY0</td><td>ROM P/E mode entry bit 0</td></tr><tr><td>b1</td><td>FENTRY1</td><td>ROM P/E mode entry bit 1</td></tr><tr><td>b2</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b7</td><td>FENTRYD</td><td>E2 data flash P/E mode entry bit</td></tr><tr><td>b8
b15</td><td>FEKEY[7:0]</td><td>Key code</td></tr></table>• FENTRYR.FENTRY1
FENTRY1: 2 MB / 1.5 MB</td><td>• Flash P/E mode entry register (FENTRYR)<table><tr><td>b0</td><td>FENTRY0</td><td>ROM P/E mode entry bit 0</td></tr><tr><td>b1</td><td>FENTRY1</td><td>ROM P/E mode entry bit 1</td></tr><tr><td>b2</td><td>FENTRY2</td><td>ROM P/E mode entry bit 2</td></tr><tr><td>b3</td><td>FENTRY3</td><td>ROM P/E mode entry bit 3</td></tr><tr><td>b7</td><td>FENTRYD</td><td>E2 data flash P/E mode entry bit</td></tr><tr><td>b8
b15</td><td>FEKEY[7:0]</td><td>Key code</td></tr></table>• FENTRYR.FENTRY0 to 3
FENTRY0: 2 MB / 1.5 MB / 1.0 MB / 768 kB / 512 kB / 384 kB
FENTRY1: 2 MB / 1.5 MB / 1.0 MB / 768 kB
FENTRY2: 2 MB / 1.5 MB
FENTRY3: 2 MB</td></tr>
<tr><td>• Peripheral clock notification register (PCKAR)
These bits are used to set the peripheral clock (PCLK) at the programming/erasure of ROM/data flash.</td><td>• Peripheral clock notification register (PCKAR)
These bits are used to set the FlashIF clock (FCLK) at the programming/erasure of the ROM/E2 data flash.</td></tr>
<tr><td>Flash memory for data storage</td><td>Functions</td><td>• Specification overview<table><tr><td>Reading via the peripheral bus</td><td>A read operation takes three cycles of PCLK3 in words or bytes.</td></tr><tr><td>Write unit</td><td>8-byte or 128-byte units</td></tr><tr><td>Programming command</td><td>2nd cycle data: 04h (8 bytes)
40h (128 bytes)</td></tr><tr><td>Block structure</td><td>8 KB × 4 blocks</td></tr><tr><td>Blank check unit</td><td>8 KB/8-byte units</td></tr><tr><td>BG0 (background operation) function</td><td>• The CPU can execute programs located in areas other than the ROM or data flash areas during ROM program or erase operations.
• Programs located in the ROM area can be executed during data flash program or erase operations.</td></tr><tr><td rowspan="4">On-board programming</td><td>Boot mode</td></tr><tr><td>—</td></tr><tr><td>User boot mode</td></tr><tr><td>User program</td></tr></table></td><td>• Specification overview<table><tr><td>Reading via the peripheral bus</td><td>A read operation takes three cycles of FCLK6 in words or bytes.</td></tr><tr><td>Program unit</td><td>2-byte units</td></tr><tr><td>Programming command</td><td>2nd cycle data: 01h (2 bytes)</td></tr><tr><td>Block structure</td><td>32 byte × 1024 blocks</td></tr><tr><td>Blank check unit</td><td>2 KB/2-byte units</td></tr><tr><td>BG0 (background operation) function</td><td>The CPU can execute programs in the ROM area during E2 data flash P/E operations.</td></tr><tr><td rowspan="4">On-board programming</td><td>Boot mode</td></tr><tr><td>USB boot mode</td></tr><tr><td>User boot mode</td></tr><tr><td>User program</td></tr></table></td></tr>
</table>

Table 2.30 Differences in Functions and Specifications (30)

<table>
<tr><th colspan="2">Item</th><th>RX610 Group</th><th>RX630 Group</th></tr>
<tr><td>Flash memory for data storage</td><td>Registers/ bits</td><td>
• Data flash read enable register (DFLRE)
<table>
<tr><td>b0</td><td>DBRE0</td><td>DB0 block read enable bit</td></tr>
<tr><td>b1</td><td>DBRE1</td><td>DB1 block read enable bit</td></tr>
<tr><td>b2</td><td>DBRE2</td><td>DB2 block read enable bit</td></tr>
<tr><td>b3</td><td>DBRE3</td><td>DB3 block read enable bit</td></tr>
<tr><td>b4</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b6</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b7</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b8
b15</td><td>KEY[7:0]</td><td>Key code</td></tr>
</table>
</td><td>
• E2 data flash read enable register 0 (DFLRE0)
<table>
<tr><td>b0</td><td>DBRE00</td><td>DB0000-DB0063 (2 KB) block read enable bit</td></tr>
<tr><td>b1</td><td>DBRE01</td><td>DB0064-DB0127 (2 KB) block read enable bit</td></tr>
<tr><td>b2</td><td>DBRE02</td><td>DB0128-DB0191 (2 KB) block read enable bit</td></tr>
<tr><td>b3</td><td>DBRE03</td><td>DB0192-DB0255 (2 KB) block read enable bit</td></tr>
<tr><td>b4</td><td>DBRE04</td><td>DB0256-DB0319 (2 KB) block read enable bit</td></tr>
<tr><td>b5</td><td>DBRE05</td><td>DB0320-DB0383 (2 KB) block read enable bit</td></tr>
<tr><td>b6</td><td>DBRE06</td><td>DB0384-DB0447 (2 KB) block read enable bit</td></tr>
<tr><td>b7</td><td>DBRE07</td><td>DB0448-DB0511 (2 KB) block read enable bit</td></tr>
<tr><td>b8
b15</td><td>KEY[7:0]</td><td>Key code</td></tr>
</table>
</td></tr>
<tr><td></td><td></td><td>—</td><td>
• E2 data flash read enable register 1 (DFLRE1)
</td></tr>
<tr><td></td><td></td><td>
• Data flash programming/erasure enable register (DFLWE)
<table>
<tr><td>b0</td><td>DBWE0</td><td>DB0 block programming/erasure enable bit</td></tr>
<tr><td>b1</td><td>DBWE1</td><td>DB1 block programming/erasure enable bit</td></tr>
<tr><td>b2</td><td>DBWE2</td><td>DB2 block programming/erasure enable bit</td></tr>
<tr><td>b3</td><td>DBWE3</td><td>DB3 block programming/erasure enable bit</td></tr>
<tr><td>b4</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b6</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b7</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b8
b15</td><td>KEY[7:0]</td><td>Key code</td></tr>
</table>
</td><td>
• E2 data flash programming/erasure enable register 0 (DFLWE0)
<table>
<tr><td>b0</td><td>DBWE00</td><td>DB0000-DB0063 (2 KB) block programming/erasure enable bit</td></tr>
<tr><td>b1</td><td>DBWE01</td><td>DB0064-DB0127 (2 KB) block programming/erasure enable bit</td></tr>
<tr><td>b2</td><td>DBWE02</td><td>DB0128-DB0191 (2 KB) block programming/erasure enable bit</td></tr>
<tr><td>b3</td><td>DBWE03</td><td>DB0192-DB0255 (2 KB) block programming/erasure enable bit</td></tr>
<tr><td>b4</td><td>DBWE04</td><td>DB0256-DB0319 (2 KB) block programming/erasure enable bit</td></tr>
<tr><td>b5</td><td>DBWE05</td><td>DB0320-DB0383 (2 KB) block programming/erasure enable bit</td></tr>
<tr><td>b6</td><td>DBWE06</td><td>DB0384-DB0447 (2 KB) block programming/erasure enable bit</td></tr>
<tr><td>b7</td><td>DBWE07</td><td>DB0448-DB0511 (2 KB) block programming/erasure enable bit</td></tr>
<tr><td>b8
b15</td><td>KEY[7:0]</td><td>Key code</td></tr>
</table>
</td></tr>
<tr><td></td><td></td><td>—</td><td>
• E2 data flash programming/erasure enable register 1 (DFLWE1)
</td></tr>
<tr><td></td><td></td><td>
• Flash P/E mode entry register (FENTRYR)
<table>
<tr><td>b0</td><td>FENTRY0</td><td>ROM P/E mode entry bit 0</td></tr>
<tr><td>b1</td><td>FENTRY1</td><td>ROM P/E mode entry bit 1</td></tr>
<tr><td>b2</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b7</td><td>FENTRYD</td><td>Data flash P/E mode entry bit</td></tr>
<tr><td>b8
b15</td><td>FEKEY[7:0]</td><td>Key code</td></tr>
</table>
• FENTRYR.FENTRY1
FENTRY1: 2 MB / 1.5 MB
</td><td>
• Flash P/E mode entry register (FENTRYR)
<table>
<tr><td>b0</td><td>FENTRY0</td><td>ROM P/E mode entry bit 0</td></tr>
<tr><td>b1</td><td>FENTRY1</td><td>ROM P/E mode entry bit 1</td></tr>
<tr><td>b2</td><td>FENTRY2</td><td>ROM P/E mode entry bit 2</td></tr>
<tr><td>b3</td><td>FENTRY3</td><td>ROM P/E mode entry bit 3</td></tr>
<tr><td>b7</td><td>FENTRYD</td><td>E2 data flash P/E mode entry bit</td></tr>
<tr><td>b8
b15</td><td>FEKEY[7:0]</td><td>Key code</td></tr>
</table>
• FENTRYR.FENTRY0 to 3
FENTRY0: 2 MB / 1.5 MB / 1.0 MB / 768 kB / 512 kB / 384 kB
FENTRY1: 2 MB / 1.5 MB / 1.0 MB / 768 kB
FENTRY2: 2 MB / 1.5 MB
FENTRY3: 2 MB
</td></tr>
</table>

Table 2.31 Differences in Functions and Specifications (31)

<table>
<tr><th colspan="2">Item</th><th>RX610 Group</th><th>RX630 Group</th></tr>
<tr><td>Boundary scan</td><td>Registers/ bits</td><td>• Data flash blank check control register (DFLBCCNT)
<table><tr><td>b0</td><td>BCSIZE</td><td>Blank check size setting bit</td></tr><tr><td>b1</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b2</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b3

b12</td><td>BCADR[9:0]</td><td>Blank check address setting bits</td></tr><tr><td>b15</td><td>—</td><td>(Reserved bit)</td></tr></table>• BCSIZE
0: The size of the area to be blank-checked is 8 bytes.
1: The size of the area to be blank-checked is 8 KB.</td><td>• E2 data flash blank check control register (DFLBCCNT)
<table><tr><td>b0

b10</td><td>BCADR [10:0]</td><td>Blank check address setting bits</td></tr><tr><td>b11</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b12</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b15</td><td>BCSIZE</td><td>Blank check size setting bit</td></tr></table>• BCSIZE
0: The size of the area to be blank-checked is 2 bytes.
1: The size of the area to be blank-checked is 2 KB.</td></tr>
<tr><td></td><td></td><td>• Instruction register (JTIR)
<table><tr><td>b0

b3</td><td>TS[3:0]</td><td>Test bit set</td></tr></table>• TS[3:0]
0000b: EXTEST
0001b: SAMPLE/PRELOAD
0100b: IDCODE (Initial value)
0110b: CLAMP
0111b: HIGHZ
1111b: BYPASS
Other than above: Reserved</td><td>• Instruction register (JTIR)
<table><tr><td>b0

b7</td><td>TS[7:0]</td><td>Test bit set</td></tr></table>• TS[7:0]
00000000b: EXTEST
01000000b: SAMPLE/PRELOAD
01010101b: IDCODE (Initial value)
11010000b: CLAMP
10000000b: HIGHZ
11111111b: BYPASS
Other than above: Reserved</td></tr>
<tr><td></td><td></td><td>• IDCODE register (JTIDR)
0000 1000 0000 1001 1001 0100 0100 0111</td><td>• ID code register (JTIDR)
0000 1000 0000 1011 1011 0100 0100 0111</td></tr>
</table>

3. Reference Documents

User's Manual: Hardware

RX610 Group User's Manual: Hardware Rev.1.20

RX630 Group User's Manual: Hardware Rev.1.50

The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

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REVISION HISTORY	RX610 Group, RX630 Group Application Note Differences between RX610 Group and RX630 Group

Rev.	Date	Description	
		Page	Summary
1.00	Feb. 08, 2013	—	First edition issued

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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