RX210, RX21A, and RX220 Groups

Asynchronous SCIc Transmission/Reception Using DTCa

R01AN1201EJ0101
Rev. 1.01
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Abstract

This application note describes how to perform asynchronous transmission/reception using the serial communications interface (SCI) with the data transfer controller (DTC) in the RX210, RX21A, and RX220 Groups.

Products

RX210, RX21A, and RX220 Groups

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

This document describes performing asynchronous serial communication using the SCI.

Transmit data is prestored in the transmit data storage area in the RAM and transmitted using the DTC. Receive data is stored in the RAM's receive data storage area using the DTC.

Serial transmission/reception starts when a falling edge is detected on the IRQ1 interrupt request pin.

- Bit rate: 38400 bps
- Data length: 8-bit, LSB first
- Stop bit: 1 bit
- Parity: None
- Hardware flow control: None

Table 1.1 lists the Peripheral Functions and Their Applications and Figure 1.1 shows a Block Diagram.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	Application
SCI channel 1 (SCI1)	Asynchronous serial transmission/reception
DTCa (DTC)	Transfer data received by SCI1 to the RAM Transfer transmit data in the RAM to SCI1
IRQ1	Start trigger for serial transmission/reception

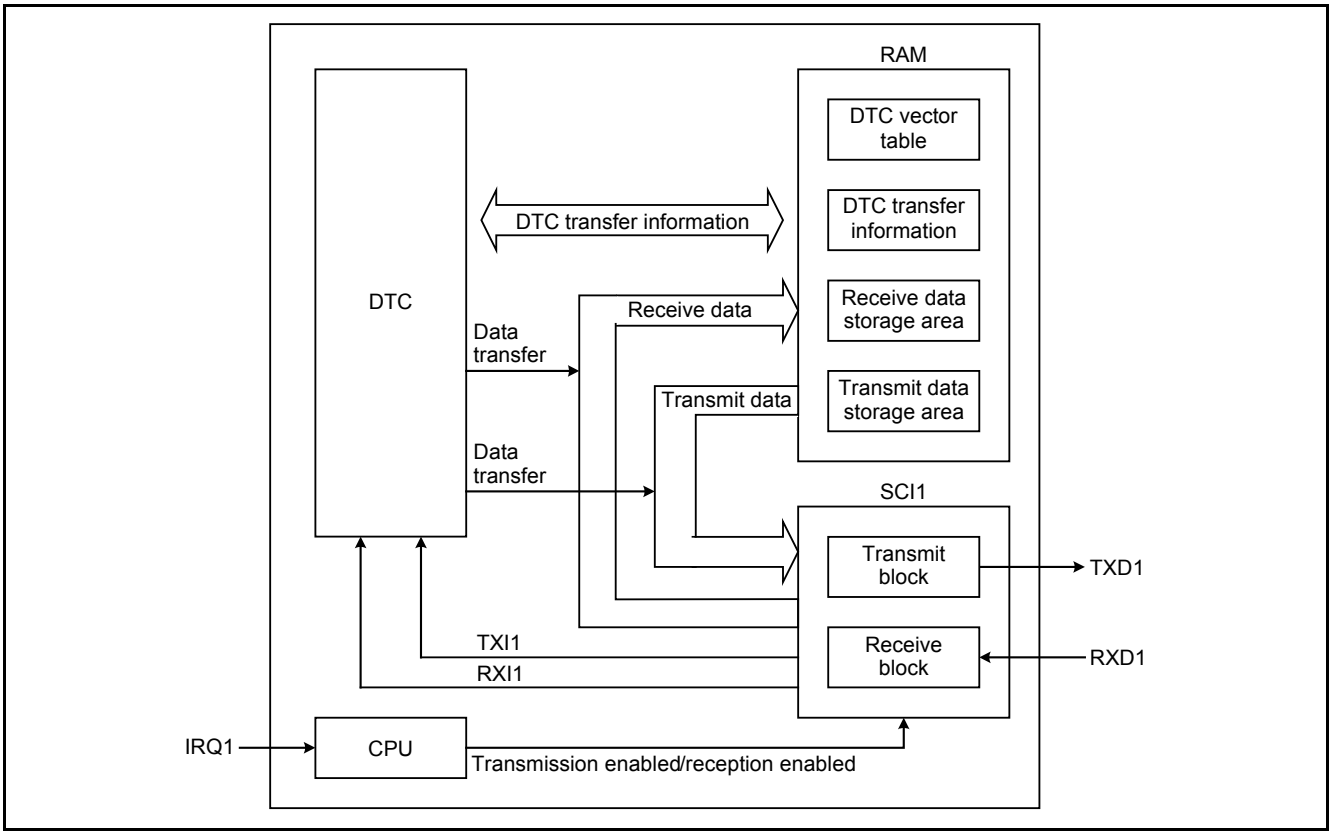


Figure 1.1 Block Diagram

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	R5F52108ADFP (RX210 Group)
Operating frequency	- Main clock: 20 MHz - PLL: 100 MHz (main clock divided by 2 and multiplied by 10) - System clock (ICLK): 50 MHz (PLL divided by 2) - Peripheral module clock B (PCLKB): 25 MHz (PLL divided by 4)
Operating voltage	5.0 V
Integrated development environment	Renesas Electronics Corporation High-performance Embedded Workshop Version 4.09.01
C compiler	Renesas Electronics Corporation C/C++ Compiler Package for RX Family V.1.02 Release 01
	Compile options -cpu=rx200 -output=obj="$(CONFIGDIR)\$(FILELEAF).obj" -debug -nologo The integrated development environment default settings are used.
iodefine.h version	Version 1.2A
Endian	Little endian
Operating mode	Single-chip mode
Processor mode	Supervisor mode
Sample code version	Version 1.00
Board used	Renesas Starter Kit for RX210 (product part number: R0K505210C000BE)

3. Reference Application Notes

For additional information associated with this document, refer to the following application notes.

- RX210 Group Initial Setting Rev. 2.00 (R01AN1002EJ)
- RX21A Group Initial Setting Rev. 1.10 (R01AN1486EJ)
- RX220 Group Initial Setting Rev. 1.10 (R01AN1494EJ)

The initial setting functions in the reference application notes are used in the sample code in this application note. The revision numbers of the reference application note are current as of when this application note was made. However the latest version is always recommended. Visit the Renesas Electronics Corporation website to check and download the latest version.

4. Hardware

4.1 Hardware Configuration

Figure 4.1 shows a Connection Example.

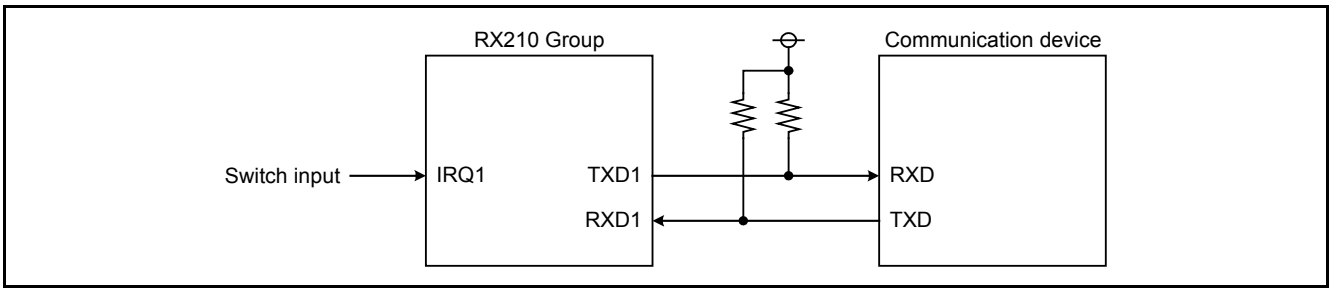


Figure 4.1 Connection Example

4.2 Pins Used

Table 4.1 lists the Pins Used and Their Functions.

Table 4.1 Pins Used and Their Functions

Pin Name	I/O	Function
P31/IRQ1	Input	Switch input to start transmission and reception
P15/RXD1	Input	Receive data input to SCI1
P16/TXD1	Output	Transmit data output from SCI1

5. Software

In the sample code, DTC is used for automatically processing SCI1 data transmission and reception. SCI1 data transmission and reception are started by pressing a switch.

When data transmission is enabled, a TXI1 interrupt request is generated, and this becomes the DTC activation source. The DTC is used to transmit data from the transmit data storage area to the TDR register, and then the data is transmitted from a pin.

When data reception is completed, an RXI1 interrupt request is generated, and this becomes the DTC activation source. The DTC is used to transfer receive data to the receive data storage area.

After transmit data has been transferred 256 times, a TXI1 interrupt occurs. At this point, the TXI1 interrupt is disabled and the TEI1 interrupt is enabled.

After receive data has been transferred 256 times, an RXI1 interrupt occurs. At this point, SCI1 reception and the RXI1 interrupt are disabled, and the receive end flag becomes 1.

After 256 bytes of data have been transmitted, a TEI1 interrupt occurs. At this point, SCI1 transmission and the TEI1 interrupt are disabled, and the transmit end flag becomes 1.

Settings for the peripheral functions used are listed below.

SCI1

- Serial communication mode: Asynchronous mode
- Transfer rate: 38400 bps
- Clock source: PCLKB
- Data length: 8 bits
- Stop bit: 1 bit
- Parity: None
- Data transfer direction: LSB first
- Interrupts used: Receive error interrupt (ERI1), receive data full interrupt (RXI1), transmit data empty interrupt (TXI1), transmit end interrupt (TEI1)

DTC

- Activation source: TXI1 or RXI1 interrupt request
- DTC address mode: Full-address mode

Setting of DTC transfer triggered by the TXI1 interrupt request

- Transfer mode: Normal transfer
- Transfer source addressing mode: Increment the SAR register after transfer
- Transfer source address: RAM (start address of the transmit data storage area)
- Transfer destination addressing mode: Address in the DAR register is fixed
- Transfer destination address: SCI1.TDR register
- Data transfer size: 8 bits
- Number of transfer operations: 256
- Chain transfer: Disabled
- Interrupts: When data transfers have been completed for the specified number of times, an interrupt request to the CPU is generated

Setting of DTC transfer triggered by the RXI1 interrupt request

- Transfer mode: Normal transfer
- Transfer source addressing mode: Address in the SAR register is fixed
- Transfer source address: SCI1.RDR register
- Transfer destination addressing mode: Increment the DAR register after transfer
- Transfer destination address: RAM (start address of the receive data storage area)
- Data transfer size: 8 bits
- Number of transfer operations: 256
- Chain transfer: Disabled
- Interrupts: When data transfers have been completed for the specified number of times, an interrupt request to the CPU is generated

IRQ1 input pin

- Detection method: Falling edge
- Digital filter: Disabled
- Interrupts: Not used

5.1 Operation Overview

5.1.1 Transmit Operation

1. Initialization
   After initialization, wait for input from a switch to start transmission/reception.
2. Detecting input from a switch to start transmission/reception
   When input from a switch to start transmission/reception is detected, set the IR flag for the IRQ1 interrupt to 0. Read the transmit end flag and receive end flag. If transmission and reception have both ended, then set the transmit end flag to 0 (transmitting). Set the transfer source address and the number of transfer operations for the DTC, and enable DTC activation. Set the SCI1.SCR.TEIE, TIE, RIE, TE, and RE bits to 1 at the same time to enable transmission and reception. By setting the SCI1.SCR.TIE and TE bits to 1 at the same time, the IR flag for the TXI1 interrupt becomes 1.
3. Starting data transfer
   After the TXI1 interrupt is enabled, the DTC is activated and the IR flag for the TXI1 interrupt becomes 0. The first byte of transmit data is transferred from the transmit data storage area in the RAM to the SCI1.TDR register.
4. Starting data transmission
   The data is transferred from the SCI1.TDR register to the SCI1.TSR register, the IR flag for the TXI1 interrupt becomes 1, and the first byte of transmit data is output from the TXD1 pin. The DTC is activated by a TXI1 interrupt request, and the second byte of transmit data is transferred.
5. TXI1 interrupt
   After the 256th data transfer has ended, the CPU accepts a TXI1 interrupt request. In the TXI1 interrupt handling, disable the TXI1 interrupt and enable the TEI1 interrupt.
6. TEI1 interrupt
   When the last bit of the 256th byte is transmitted, the SCI1.TDR register is not updated, so a TEI1 interrupt request is generated. In the TEI1 interrupt handling, disable transmission and the TEI1 interrupt, and set the transmit end flag to 1 (transmission ended). Operation is repeated from step 2 above.

Figure 5.1 shows the Timing Diagram of the Transmit Operation.

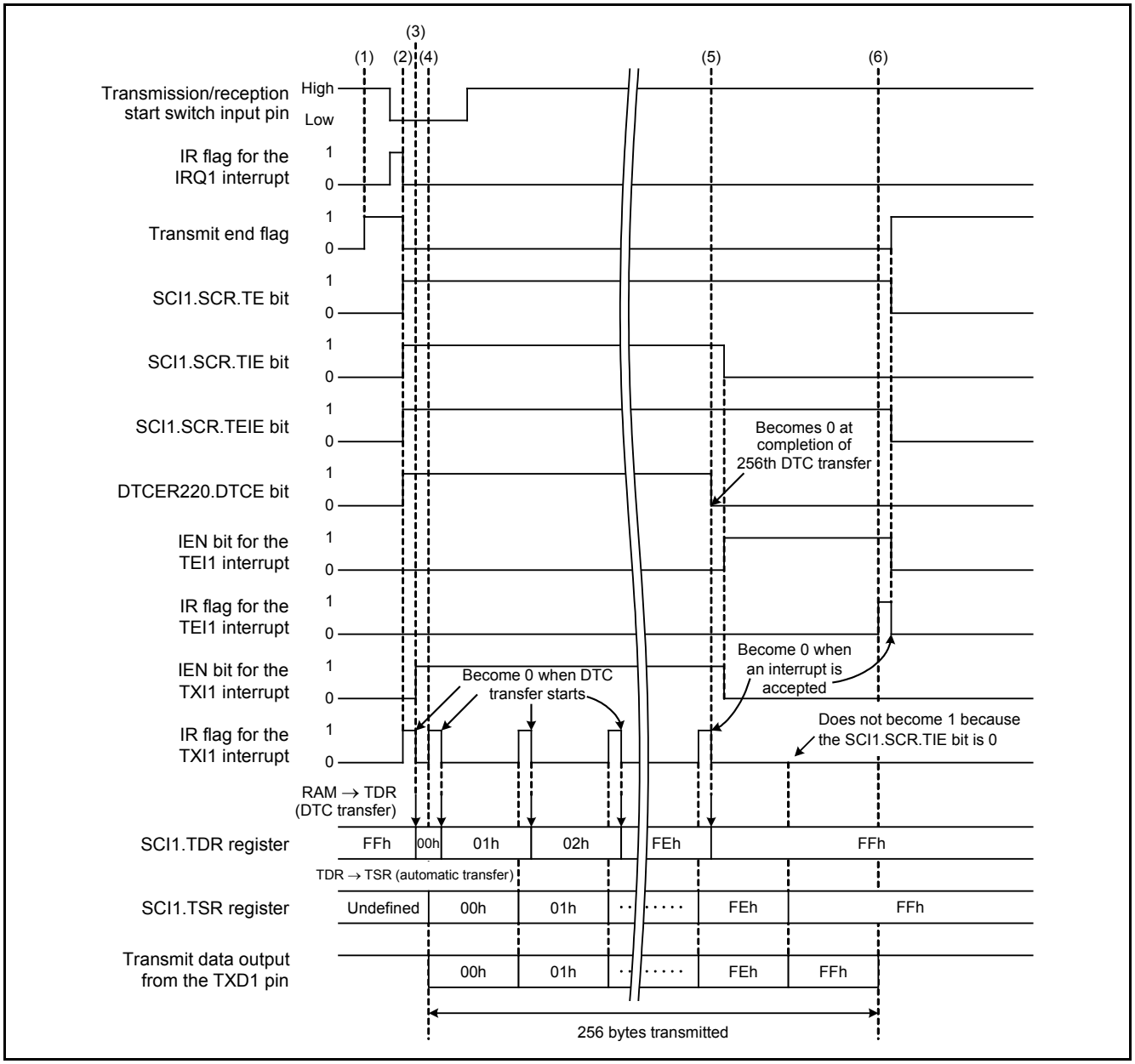


Figure 5.1 Timing Diagram of the Transmit Operation

5.1.2 Receive Operation

1. Initialization
   After initialization, wait for input from a switch to start transmission/reception.
2. Detecting input from a switch to start transmission/reception
   When input from a switch to start transmission/reception is detected, set the IR flag for the IRQ1 interrupt to 0. Read the transmit end flag and receive end flag. If transmission and reception have both ended, then set the receive end flag to 0 (receiving). Set the transfer destination address and the number of transfer operations for the DTC, and enable DTC activation. Set the SCI1.SCR.TEIE, TIE, RIE, TE, and RE bits to 1 at the same time to enable transmission and reception, and enable the RXI1 interrupt.
3. Data reception end
   After the first byte of data is received, transfer the data from the SCI1.RSR register to the SCI1.RDR register, and the IR flag for the RXI1 interrupt becomes 1.
4. Starting data transfer
   The DTC is activated by an RXI1 interrupt request, and the IR flag for the RXI1 interrupt becomes 0. Then transfer the first byte of receive data from the SCI1.RDR register to the RAM's receive data storage area.
5. RXI1 interrupt
   After the 256th data transfer has ended, the CPU accepts an RXI1 interrupt request. In the RXI1 interrupt handling, disable reception and the RXI1 interrupt, and set the receive end flag to 1 (reception ended). Operation is repeated from step 2 above.

Figure 5.2 shows the Timing Diagram of the Receive Operation.

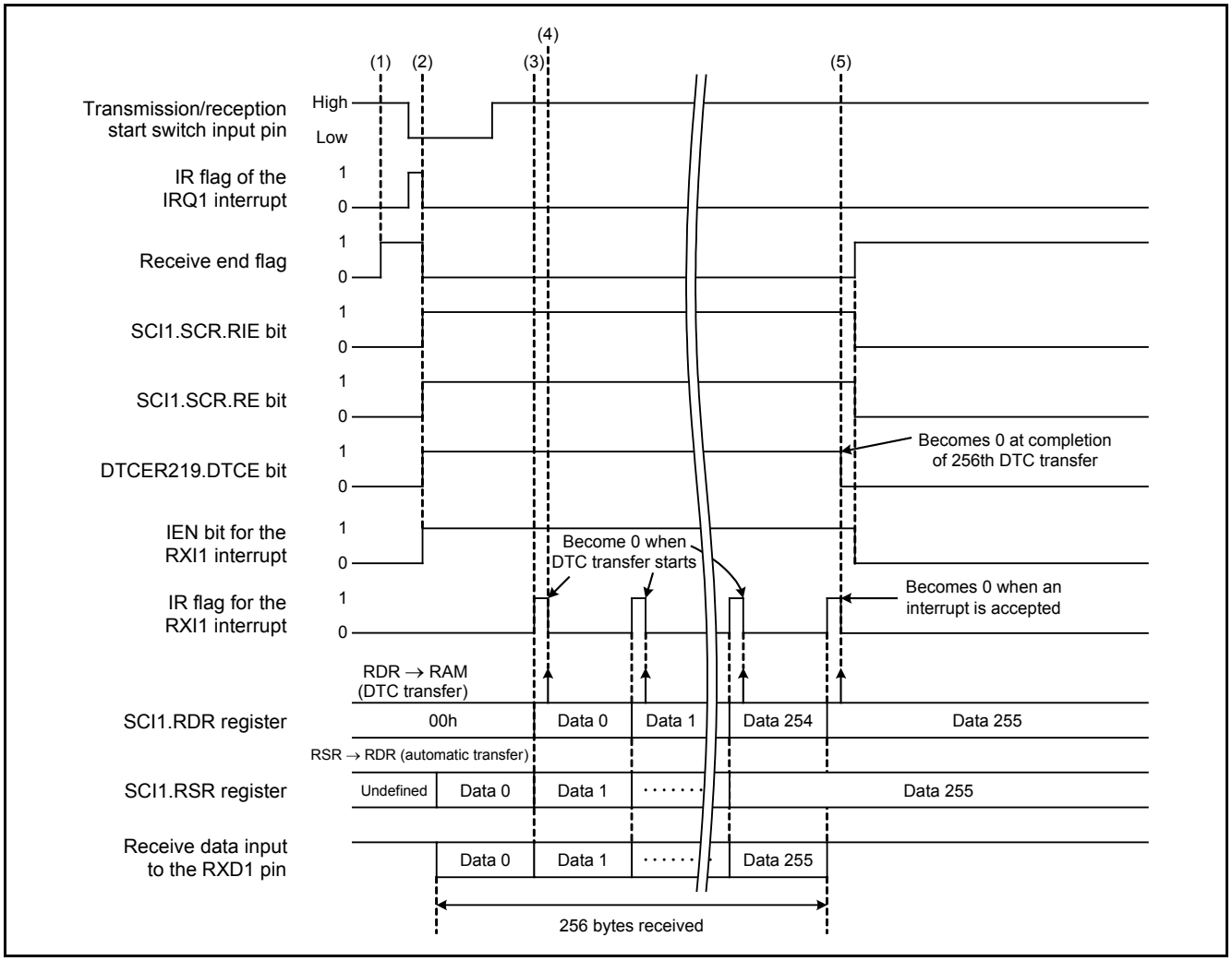


Figure 5.2 Timing Diagram of the Receive Operation

Notes on Implementing the Sample Code Into the User System

Note that the following may occur when implementing the sample code accompanying this application note into the user system.

- When user defined interrupt handling makes the interrupts defined in the sample code wait for a lengthy amount of time, the sample code may operate erroneously.

5.2 Section Composition

Table 5.1 lists the section information that is changed in the sample code.

For details on adding/changing or deleting sections, refer to the latest RX Family, C/C++ Compiler Package User's Manual.

Table 5.1 Section Information Changed in the Sample Code

Section Name	Change	Address	Content
DTC_SECTION	Addition	0000 3000h	DTC vector table

5.3 File Composition

Table 5.2 lists the Files Used in the Sample Code. Files generated by the integrated development environment should not be listed in this table.

Table 5.2 Files Used in the Sample Code

File Name	Outline
main.c	Main processing
r_init_stop_module.c	Stop processing for active peripheral functions after a reset
r_init_stop_module.h	Header file for r_init_stop_module.c
r_init_non_existent_port_init.c	Nonexistent port initialization
r_init_non_existent_port_init.h	Header file for r_init_non_existent_port_init.c
r_init_clock.c	Clock initialization
r_init_clock.h	Header file for r_init_clock.c

5.4 Option-Setting Memory

Table 5.3 lists the Option-Setting Memory Configured in the Sample Code. When necessary, set a value suited to the user system.

Table 5.3 Option-Setting Memory Configured in the Sample Code

Symbol	Address	Setting Value	Contents
OFS0	FFFF FF8Fh to FFFF FF8Ch	FFFF FFFFh	The IWDT is stopped after a reset. The WDT is stopped after a reset.
OFS1	FFFF FF8Bh to FFFF FF88h	FFFF FFFFh	The voltage monitor 0 reset is disabled after a reset. HOCO oscillation is disabled after a reset.
MDES	FFFF FF83h to FFFF FF80h	FFFF FFFFh	Little endian

5.5 Constants

Table 5.4 lists the Constants Used in the Sample Code.

Table 5.4 Constants Used in the Sample Code

Constant Name	Setting Value	Contents
BUF_SIZE	256	Size of the transmit data or receive data storage area
DTC_CNT	BUF_SIZE	Number of DTC transfers

5.6 Structure/Union List

Figure 5.3 shows the Structure/Union Used in the Sample Code.

```
/* **** DTC transfer information **** */
#pragma bit_order     left          /* Bit field order: The bit field members are allocated from upper bits */
#pragma unpack                      /* Boundary alignment value for structure members: Alignment by member type */
struct st_dtc_full
{
    union
    {
        unsigned long LONG;
        struct
        {
            unsigned long MRA_MD     :2;
            unsigned long MRA_SZ     :2;
            unsigned long MRA_SM     :2;
            unsigned long            :2;
            unsigned long MRB_CHNE   :1;
            unsigned long MRB_CHNS   :1;
            unsigned long MRB_DISEL  :1;
            unsigned long MRB_DTS    :1;
            unsigned long MRB_DM     :2;
            unsigned long            :2;
            unsigned long            :16;
        } BIT;
    } MR;
    void * SAR;
    void * DAR;
    struct
    {
        unsigned long CRA:16;
        unsigned long CRB:16;
    } CR;
};
#pragma packoption                  /* End of specification for the boundary alignment value for structure members */
#pragma bit_order                   /* End of specification for the bit field order */
```

Figure 5.3 Structure/Union Used in the Sample Code

5.7 Variables

Table 5.5 lists the Global Variables.

Table 5.5 Global Variables

Type	Variable Name	Contents	Function Used
unsigned char	trn_end_flag	Transmit end flag 0: Transmitting 1: Transmission ended	main, Excep_SCI1_TEI1
unsigned char	rcv_end_flag	Receive end flag 0: Receiving 1: Reception ended	main, Excep_SCI1_RXI1
unsigned char	trnbuf[BUF_SIZE]	Transmit data storage area	main, dtc_init, sci1_start
unsigned char	rcvbuf[BUF_SIZE]	Receive data storage area	dtc_init, sci1_start
struct st_dtc_full	dtc_info_rxi1	DTC transfer information for RXI1	dtc_init, sci1_start
struct st_dtc_full	dtc_info_txi1	DTC transfer information for TXI1	dtc_init, sci1_start
void *	dtc_vect_table[256]	DTC vector table	dtc_init

5.8 Functions

Table 5.6 lists the Functions.

Table 5.6 Functions

Function Name	Outline
main	Main processing
port_init	Port initialization
R_INIT_StopModule	Stop processing for active peripheral functions after a reset
R_INIT_NonExistentPort	Nonexistent port initialization
R_INIT_Clock	Clock initialization
peripheral_init	Peripheral function initialization
sci1_init	SCI1 initialization
dtc_init	DTC initialization
irq_init	IRQ initialization
sci1_start	SCI1 transmission/reception start processing
Excep_SCI1_RXI1	SCI1 receive data full interrupt handling
Excep_SCI1_TXI1	SCI1 transmit data empty interrupt handling
Excep_SCI1_TEI1	SCI1 transmit end interrupt handling
Excep_SCI1_ERI1	SCI1 receive error interrupt handling

5.9 Function Specifications

The following tables list the sample code function specifications.

main	
Overview	Main processing
Header	None
Declaration	void main(void)
Description	After initialization, SCI1 transmission/reception starts when the transmit/receive start switch input is detected.
Arguments	None
Return values	None

port_init	
Overview	Port initialization
Header	None
Declaration	void port_init(void)
Description	Ports are initialized.
Arguments	None
Return values	None

R_INIT_StopModule	
Overview	Stop processing for active peripheral functions after a reset
Header	r_init_stop_module.h
Declaration	void R_INIT_StopModule(void)
Description	Performs settings to enter the module stop state.
Arguments	None
Return values	None
Remarks	Transition to the module stop state is not performed in the sample code. For details on this function, refer to the Initial Setting application note for the product used.

R_INIT_NonExistentPort	
Overview	Nonexistent port initialization
Header	non_existent_port_init.h
Declaration	void R_INIT_NonExistentPort (void)
Description	Initializes port direction registers for ports that do not exist in products with less than 100 pins.
Arguments	None
Return values	None
Remarks	The number of pins in the sample code is set for the 100-pin package (PIN_SIZE=100). After this function is called, when writing in byte units to the PDR and PODR registers which have nonexistent ports, set the corresponding bits for nonexistent ports as follows: set the I/O select bits in the PDR registers to 1 and set the output data store bits in the PODR registers to 0. For details on this function, refer to the Initial Setting application note for the product used.

R_INIT_Clock	
Overview	Clock initialization
Header	r_init_clock.h
Declaration	void R_INIT_Clock(void)
Description	Initializes clocks.
Arguments	None
Return values	None
Remarks	In the sample code, processing is performed so the system clock is used as the PLL clock, and the sub-clock is not used. For details on this function, refer to the Initial Setting application note for the product used.

peripheral_init	
Overview	Peripheral function initialization
Header	None
Declaration	void peripheral_init (void)
Description	Initializes peripherals functions that are used.
Arguments	None
Return values	None

sci1_init	
Overview	SCI1 initialization
Header	None
Declaration	void sci1_init(void)
Description	Initializes SCI1.
Arguments	None
Return values	None

dtc_init	
Overview	DTC initialization
Header	None
Declaration	void dtc_init(void)
Description	Initializes the DTC.
Arguments	None
Return values	None

irq_init	
Overview	IRQ initialization
Header	None
Declaration	void irq_init(void)
Description	Initializes IRQ1.
Arguments	None
Return values	None

sci1_start	
Overview	SCI1 transmission/reception start processing
Header	None
Declaration	void sci1_start(void)
Description	Starts SCI1 transmission/reception.
Arguments	None
Return values	None

Excep_SCI1_RXI1	
Overview	SCI1 receive data full interrupt handling
Header	None
Declaration	void Excep_SCI1_RXI1(void)
Description	Reception is disabled, the RXI1 interrupt is disabled, and the receive end flag is set.
Arguments	None
Return values	None

Excep_SCI1_TXI1	
Overview	SCI1 transmit data empty interrupt handling
Header	None
Declaration	void Excep_SCI1_TXI1(void)
Description	Disables the TXI1 interrupt and enables the TEI1 interrupt.
Arguments	None
Return values	None

Excep_SCI1_TEI1	
Overview	SCI1 transmit end interrupt handling
Header	None
Declaration	void Excep_SCI1_TEI1(void)
Description	Transmission is disabled, the TEI1 interrupt is disabled, and the transmit end flag is set.
Arguments	None
Return values	None

Excep_SCI1_ERI1	
Overview	SCI1 receive error interrupt handling
Header	None
Declaration	void Excep_SCI1_ERI1(void)
Description	Performs SCI1 reception error processing.
Arguments	None
Return values	None
Remarks	SCI1 reception error processing is not performed in the sample code (infinite loop). Add processing as needed.

5.10 Flowcharts

5.10.1 Main Processing

Figure 5.4 shows the Main Processing.

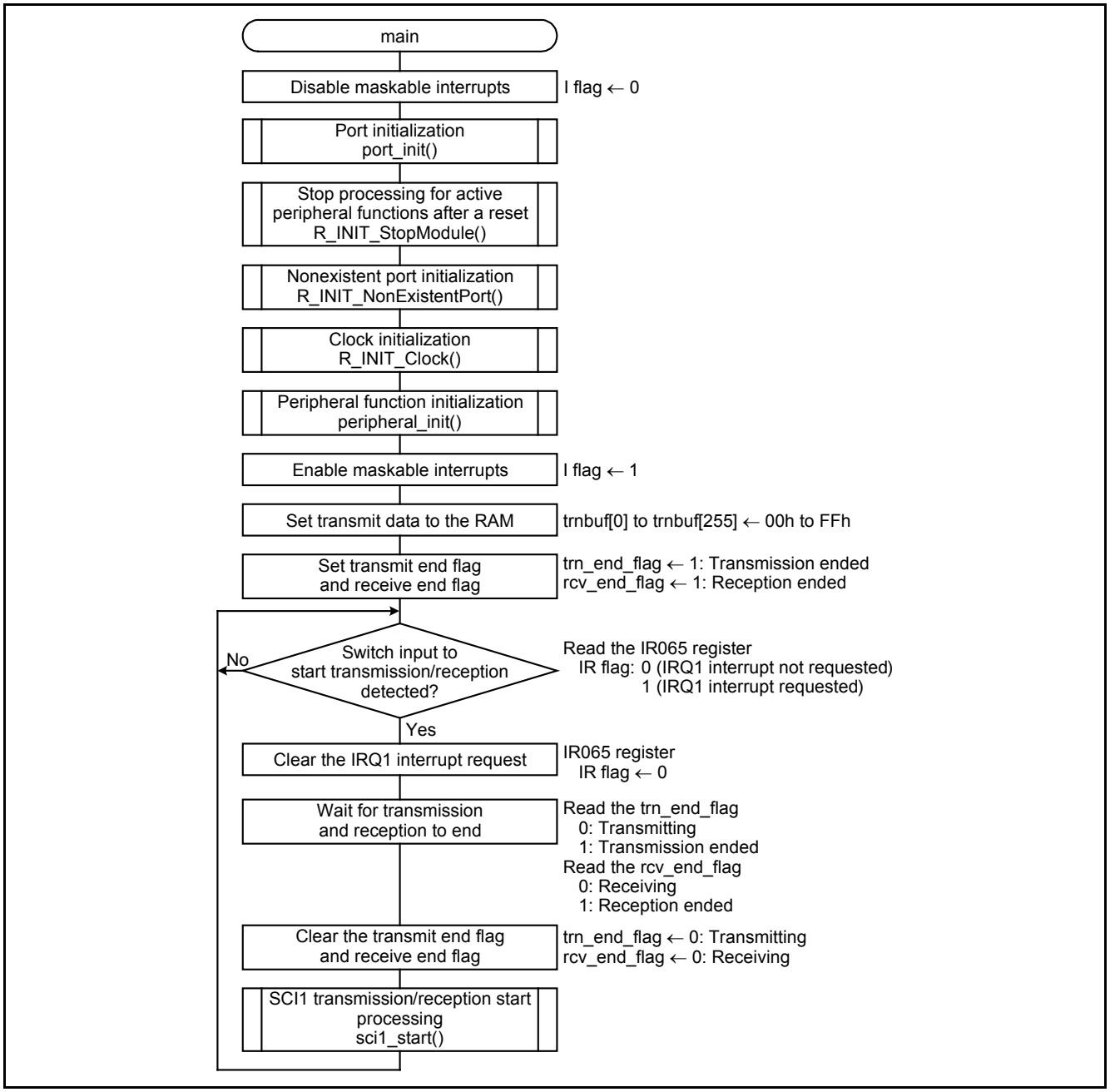


Figure 5.4 Main Processing

5.10.2 Port Initialization

Figure 5.5 shows the Port Initialization.

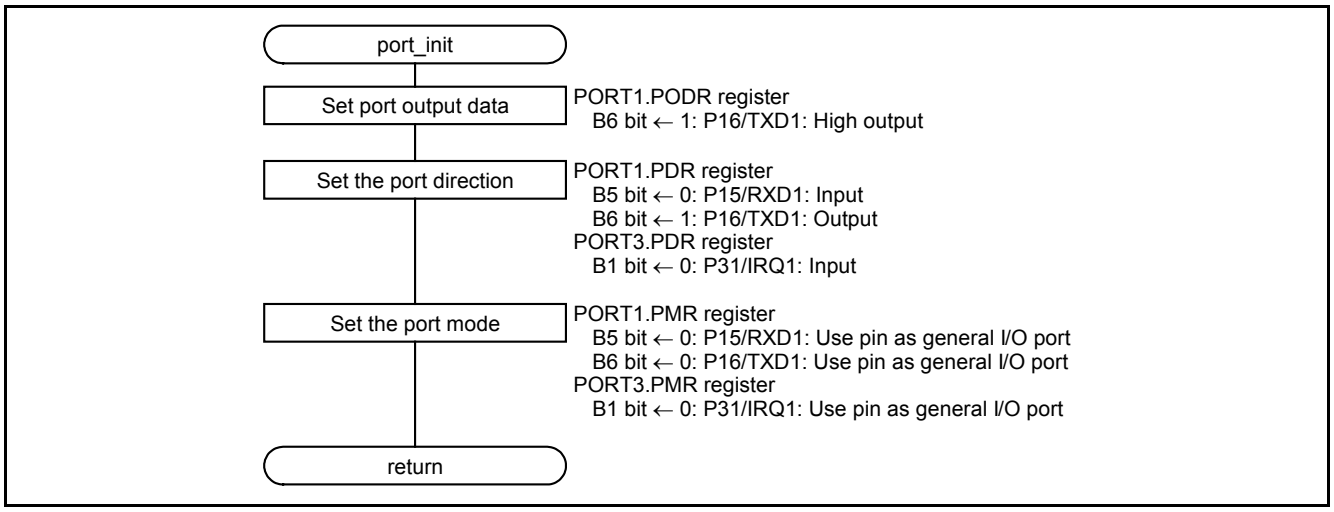


Figure 5.5 Port Initialization

5.10.3 Peripheral Function Initialization

Figure 5.6 shows the Peripheral Function Initialization.

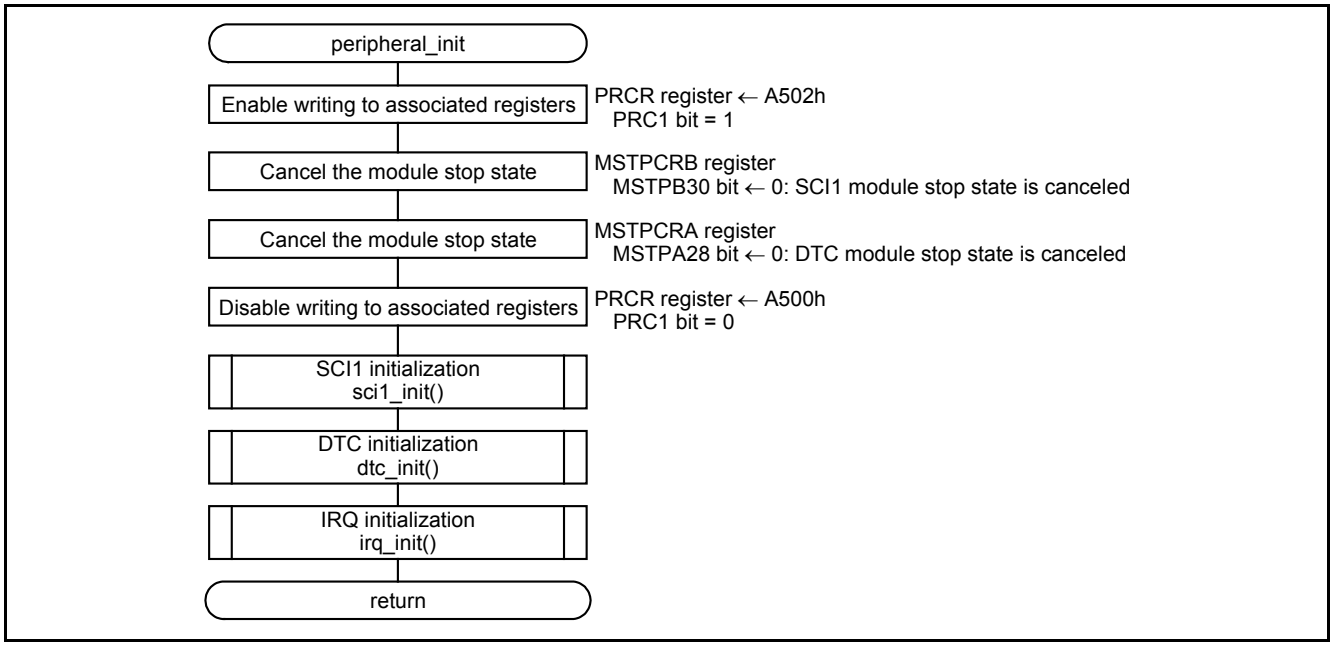
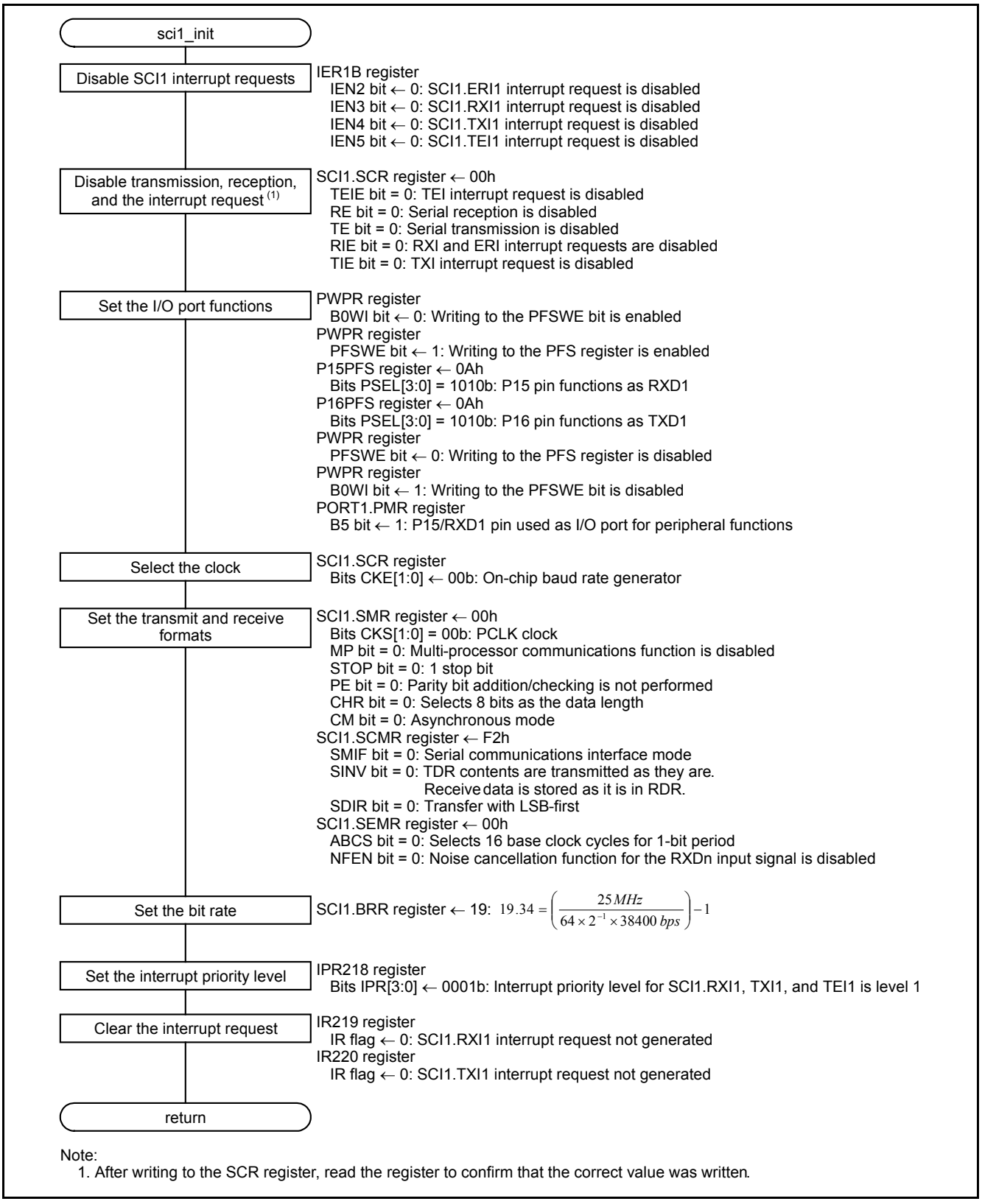


Figure 5.6 Peripheral Function Initialization

5.10.4 SCI1 Initialization

Figure 5.7 shows the SCI1 Initialization.



Note:
1. After writing to the SCR register, read the register to confirm that the correct value was written.

Figure 5.7 SCI1 Initialization

5.10.5 DTC Initialization

Figure 5.8 shows the DTC Initialization.

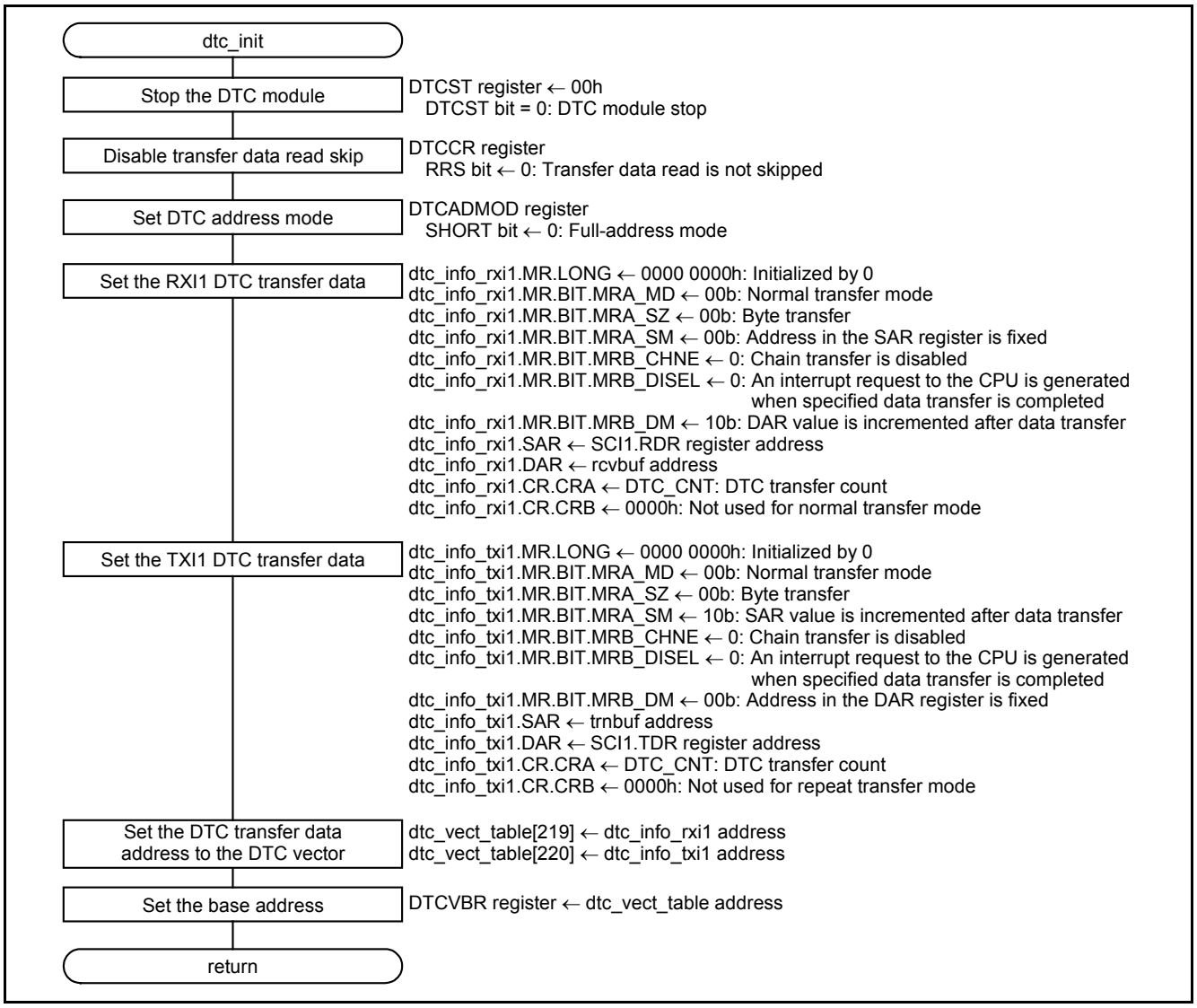


Figure 5.8 DTC Initialization

5.10.6 IRQ Initialization

Figure 5.9 shows the IRQ Initialization.

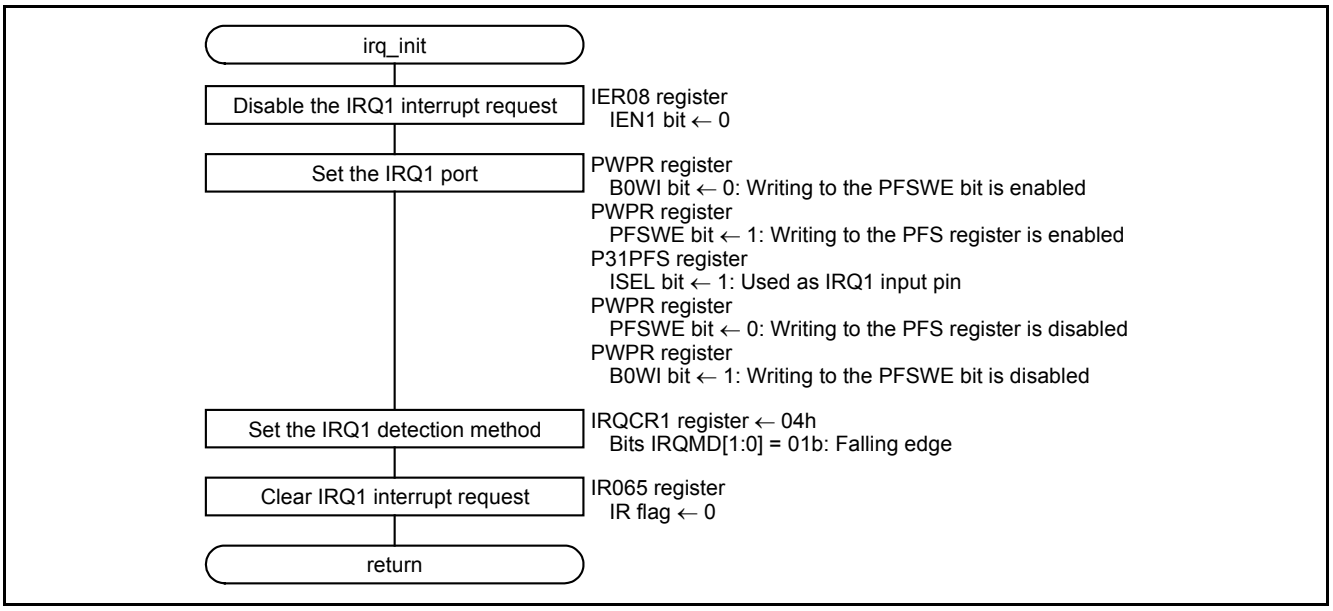


Figure 5.9 IRQ Initialization

5.10.7 SCI1 Transmission/Reception Start Processing

Figure 5.10 shows the SCI1 Transmission/Reception Start Processing.

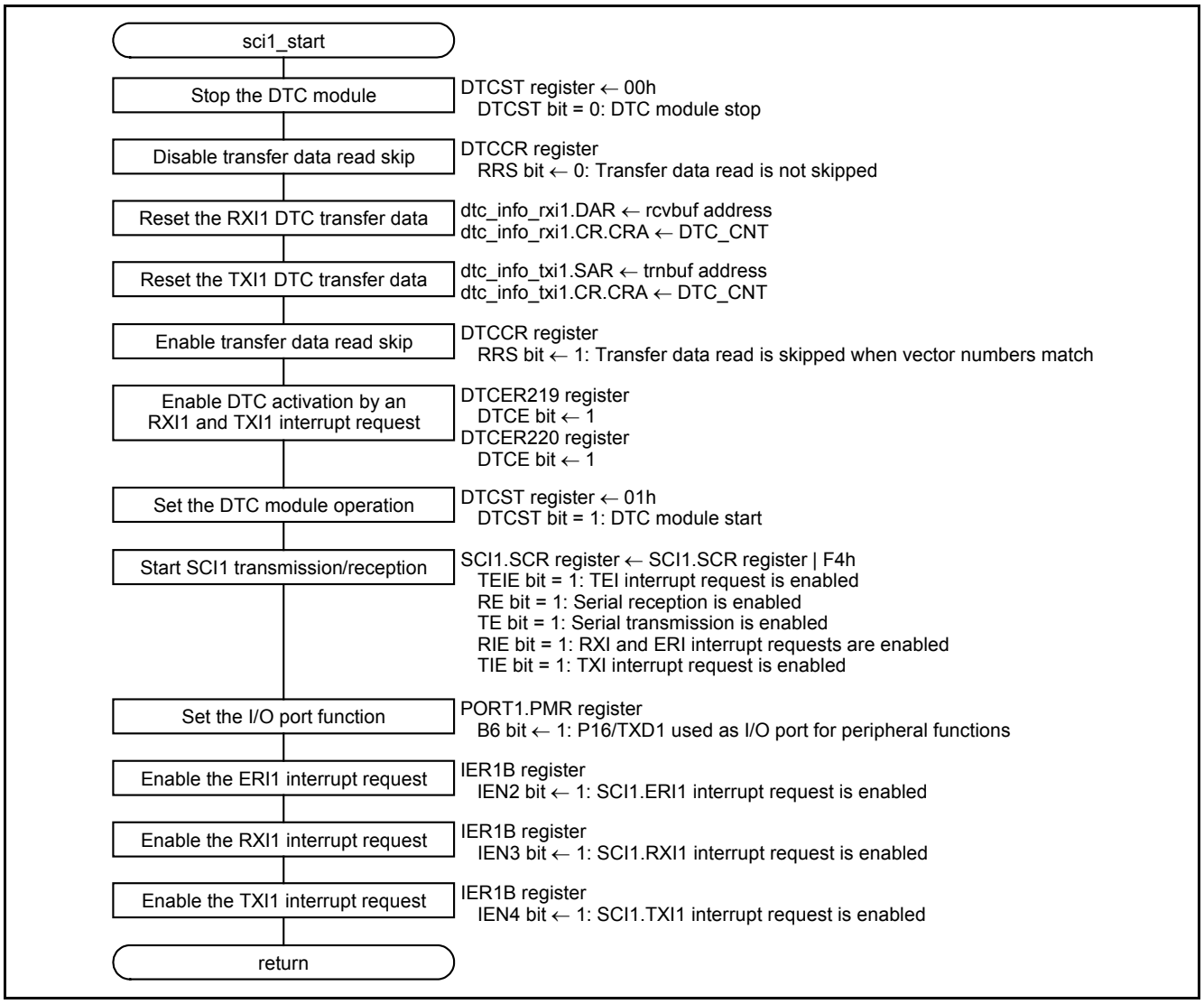


Figure 5.10 SCI1 Transmission/Reception Start Processing

5.10.8 SCI1 Receive Data Full Interrupt Handling

Figure 5.11 shows the SCI1 Receive Data Full Interrupt Handling.

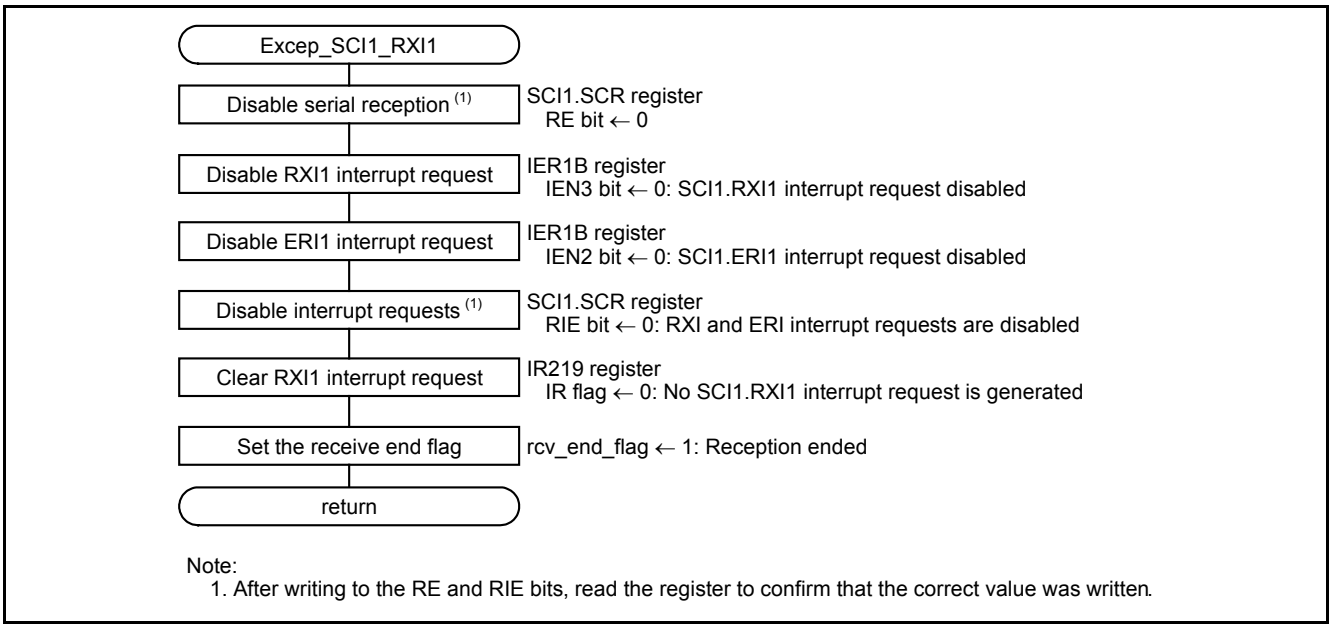


Figure 5.11 SCI1 Receive Data Full Interrupt Handling

5.10.9 SCI1 Transmit Data Empty Interrupt Handling

Figure 5.12 shows the SCI1 Transmit Data Empty Interrupt Handling.

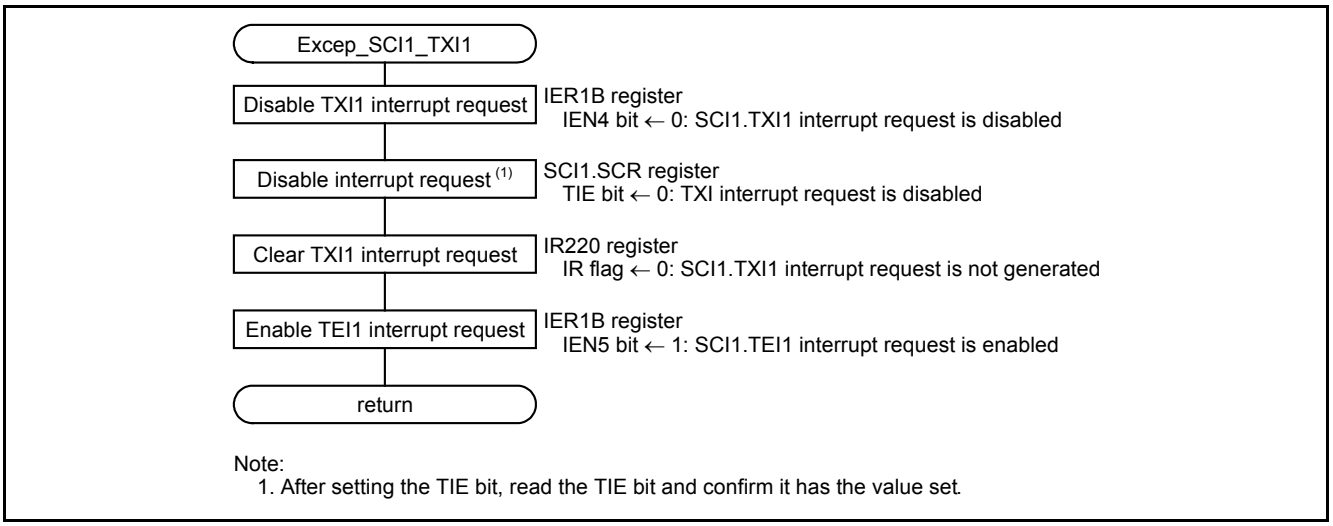


Figure 5.12 SCI1 Transmit Data Empty Interrupt Handling

5.10.10 SCI1 Transmit End Interrupt Handling

Figure 5.13 shows the SCI1 Transmit End Interrupt Handling.

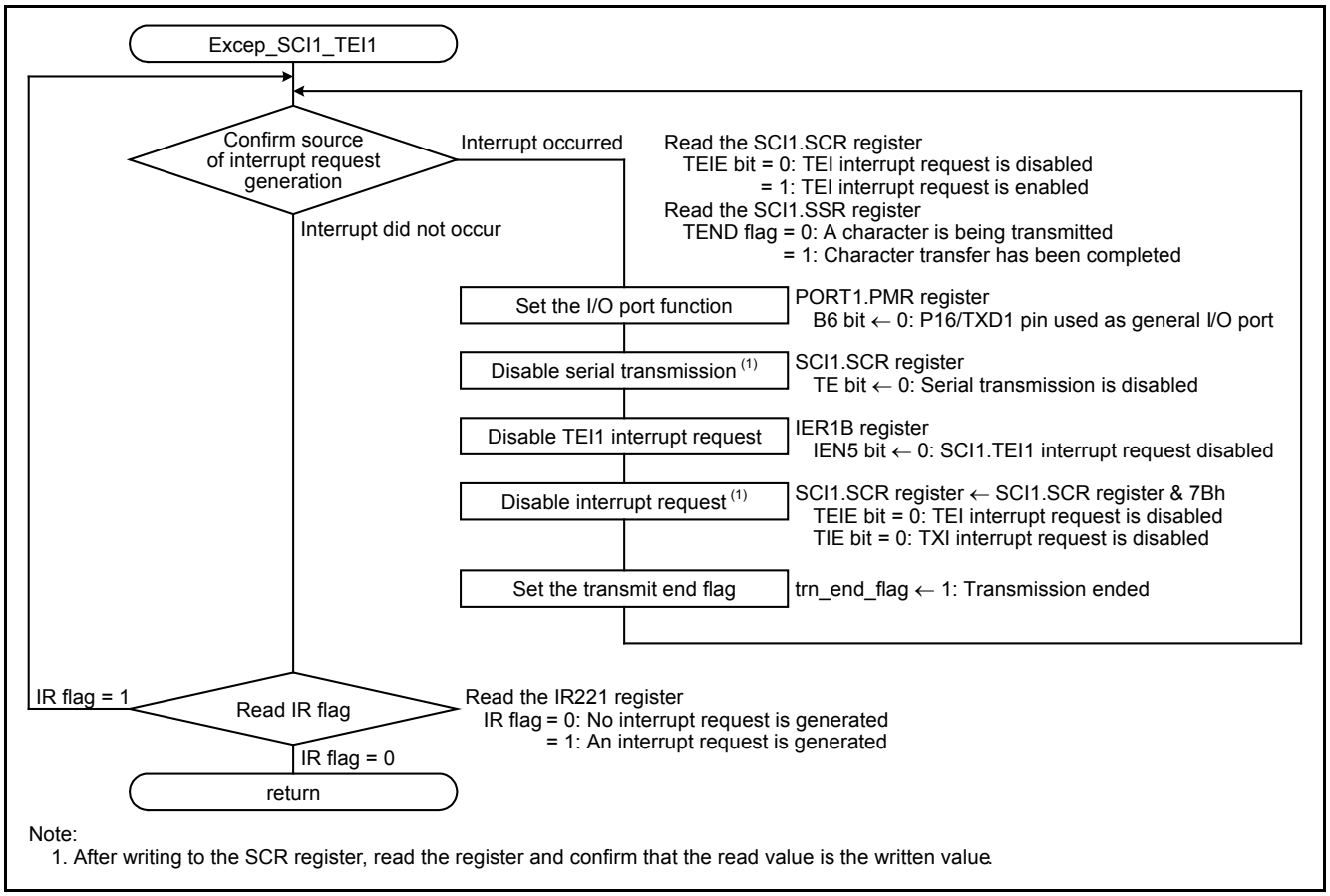


Figure 5.13 SCI1 Transmit End Interrupt Handling

5.10.11 SCI1 Receive Error Interrupt Handling

Figure 5.14 shows the SCI1 Receive Error Interrupt Handling.

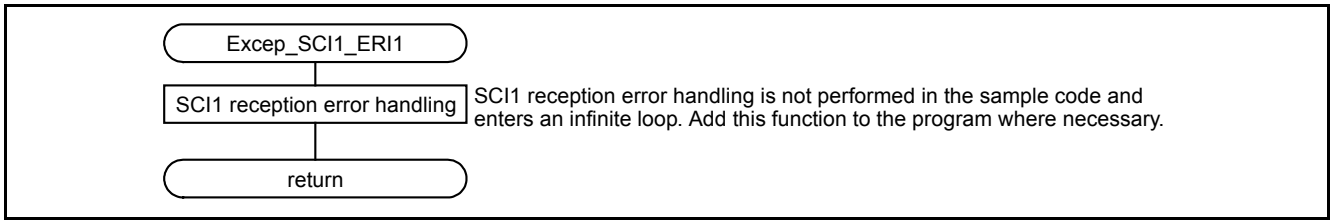


Figure 5.14 SCI1 Receive Error Interrupt Handling

6. Applying This Application Note to the RX21A or RX220 Group

The sample code accompanying this application note has been confirmed to operate with the RX210 Group. To make the sample code operate with the RX21A or RX220 Group, use this application note in conjunction with the Initial Setting application note for each group.

For details on using this application note with the RX21A and RX220 Groups, refer to “5. Applying the RX210 Group Application Note to the RX21A Group” in the RX21A Group Initial Setting application note, and “4. Applying the RX210 Group Application Note to the RX220 Group” in the RX220 Group Initial Setting application note.

Note: • When using the RX21A Group, SCI0 and SCI12 are not available. Use SCI1, SCI5, SCI6, SCI8, or SCI9.
When using the RX220 Group, SCI0, SCI8, and SCI12 are not available. Use SCI1, SCI5, SCI6, or SCI9.

7. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

8. Reference Documents

User's Manual: Hardware
RX210 Group User's Manual: Hardware Rev.1.50 (R01UH0037EJ)
RX21A Group User's Manual: Hardware Rev.1.00 (R01UH0251EJ)
RX220 Group User's Manual: Hardware Rev.1.10 (R01UH0292EJ)
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

User's Manual: Development Tools
RX Family C/C++ Compiler Package V.1.01 User's Manual Rev.1.00 (R20UT0570EJ)
The latest version can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website
http://www.renesas.com

Inquiries
http://www.renesas.com/contact/

REVISION HISTORY	RX210, RX21A, and RX220 Groups Application Note Asynchronous SCIc Transmission/Reception Using DTCa

Rev.	Date	Description	
		Page	Summary
1.00	June 14, 2013	—	First edition issued
1.01	July 1, 2014	1	Products: Added the RX21A and RX220 Groups.
		4	3. Reference Application Notes: Added the Initial Setting application notes for the RX21A and RX220 Groups.
		14,15	Modified the description of reference application note in the following functions: R_INIT_StopModule, R_INIT_NonExistentPort, and R_INIT_Clock.
		25	6. Applying This Application Note to the RX21A or RX220 Group: Added.
		26	8. Reference Documents: Added the User's Manual: Hardware for the RX21A and RX220 Groups.

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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