

# RL78/G23

## Voltage Detection Circuits

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### Introduction

This application note explains how to use the two voltage detection circuits (LVDs) incorporated into the RL78/G23 microcontroller.

### Target device

RL78/G23

When applying this application note to another model of microcontroller, make the appropriate changes according to the microcontroller specifications and evaluate its operation extensively.

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## 1. Overview of LVDs

The RL78/G23 microcontroller incorporates two voltage detection circuits, designated 0 (LVD0) and 1 (LVD1).

LVD0 and LVD1 compare the power supply voltage ( $V_{DD}$ ) with a detection voltage ( $V_{LVD0}$  and  $V_{LVD1}$ ) and generate an internal reset or interrupt request signal.

During supply voltage rise, you must use LVD0 or an external reset signal to maintain a reset state until the power supply voltage reaches the working voltage range described in the AC characteristics subcategory of the electrical characteristics. During supply voltage fall, the microcontroller must either transition to STOP mode or use LVD0 or an external reset signal to enter a reset state before  $V_{DD}$  falls below the working voltage range.

### 1.1 LVD0

#### 1.1.1 Setup method

Use the option byte (000C1H) to set the operation mode and detection voltage ( $V_{LVD0}$ ) for LVD0.

#### 1.1.2 Functionality

LVD0 compares the supply voltage ( $V_{DD}$ ) with the detection voltage ( $V_{LVD0}$ ) and generates an internal reset or interrupt request signal (INTLVI). You can select one of six detection voltages ( $V_{LVD0}$ ).

In reset mode, LVD0 keeps the microcontroller in reset status until LVD0 detects  $V_{DD} \geq V_{LVD0}$  during supply voltage rise. LVD0 generates an internal reset signal if it detects  $V_{DD} < V_{LVD0}$  at supply voltage fall, and then keeps the microcontroller in reset status until  $V_{DD} \geq V_{LVD0}$  is detected.

In interrupt mode, LVD0 keeps the microcontroller in reset status until  $V_{DD} \geq V_{LVD0}$  is detected during supply voltage rise. After releasing reset status, LVD0 generates an interrupt request signal (INTLVI) upon detecting  $V_{DD} < V_{LVD0}$  or  $V_{DD} \geq V_{LVD0}$ .

**Note:** At supply voltage fall, LVD0 requires a detection delay of 500  $\mu$ s before detecting  $V_{DD} < V_{LVD0}$  after the supply voltage ( $V_{DD}$ ) falls below the detection voltage ( $V_{LVD0}$ ). If the detection voltage ( $V_{LVD0}$ ) is set to the lower limit of the working voltage range, the RL78/G23 unit will operate outside the working voltage range during the detection delay period. To avoid this issue, consider the amount of supply voltage fall that occurs during the detection delay period and set a detection voltage ( $V_{LVD0}$ ) such that the RL78/G23 unit always operates within its working voltage range.

## 1.2 LVD1

### 1.2.1 Setup method

LVD1 is inactive when the microcontroller exits reset status. To activate LVD1, you must use a user program to set the operation mode and detection voltage ( $V_{LVD1}$ ) in the voltage detection level register (LVIS).

The LVIS register cannot be rewritten after the microcontroller exits reset status. Use the following procedure to permit rewriting of the LVIS register and enable LVD1. Note that **you can rewrite the LVD1 detection voltage ( $V_{LVD1}$ ) only once** after exiting reset status.

To allow the LVIS register to be set from a user program, you must use LVD0 or an external reset signal to keep the microcontroller in reset status until the supply voltage reaches the working voltage range described in the AC characteristics subcategory of the electrical characteristics.

- (1) Assign 1 to the LVISEN bit of the voltage detection register (LVIM).
- (2) Assign 1 to the LVD1EN bit of the voltage detection level register (LVIS) and set the LVD1SEL and LVD1V4-0 bits.
- (3) Assign 0 to the LVISEN bit of the voltage detection register (LVIM).
- (4) LVD1 becomes active after the stabilization time (500  $\mu$ s or longer) has elapsed.

### 1.2.2 Functionality

LVD1 compares the supply voltage ( $V_{DD}$ ) to the detection voltage ( $V_{LVD1}$ ) and generates an internal reset or interrupt request signal. You can select one of eighteen detection voltages ( $V_{LVD1}$ ).

When LVD1 is activated in reset mode, LVD1 detects  $V_{DD} < V_{LVD1}$  and generates an internal reset. The reset initializes the voltage detection level register (LVIS) and stops LVD1 operation. If LVD1 is activated while  $V_{DD} < V_{LVD1}$ , then the microcontroller alternates between reset status (CPU stopped) and non-reset status (CPU operational) until  $V_{DD} \geq V_{LVD1}$ .

When LVD1 is activated in interrupt mode, LVD1 detects  $V_{DD} < V_{LVD1}$  and generates an interrupt request signal (INTLVI).

After the first detection, LVD1 detects  $V_{DD} < V_{LVD1}$  or  $V_{DD} \geq V_{LVD1}$  and generates an interrupt request signal (INTLVI).

At power-on, normal operation (CPU operation) begins after the voltage stabilization time (typically 4 ms) and reset processing time have elapsed. Therefore, if normal operation starts while  $V_{DD} \geq V_{LVD1}$ , the above-described alternation between reset status and non-reset status does not occur, and no interrupt request signal (INTLVI) is generated at supply voltage rise. When starting normal operation while  $V_{DD} < V_{LVD1}$ , take the precautionary measures explained in 3.5 Voltage fluctuation during supply voltage rise.

## 2. Selecting the LVD Operation Mode

### When storing data at supply voltage fall

Use interrupt mode. Consider the amount of supply voltage fall that occurs during data storage processing and during the detection delay period and set a detection voltage such that the RL78/G23 unit always operates within its working voltage range.

- LVD0: Interrupt mode <sup>Note</sup>, LVD1: Off
- LVD0: Interrupt mode <sup>Note</sup>, LVD1: Interrupt mode (Condition:  $V_{LVD0} < V_{LVD1}$ )
- LVD0: Reset mode, LVD1: Interrupt mode (Condition:  $V_{LVD0} < V_{LVD1}$ )

Note: You must use LVD0 or an external reset signal to maintain a reset state until the supply voltage reaches the working voltage range described in the AC characteristics subcategory of the electrical characteristics. LVD0 can be used to release the initial internal reset after power-on.

Caution: When LVD0 is set to interrupt mode with the condition  $V_{LVD0} > V_{LVD1}$ , LVD0 becomes undefined from the point when LVD1 is set after exiting reset status.

### When not using external reset

You must set up the LVD in such a way that the RL78/G23 always operates within the working voltage range. Consider the amount of supply voltage fall that occurs during the detection delay period and set a detection voltage that keeps the RL78/G23 within the working voltage range. Set the LVD to reset mode. If none of the six detection voltages ( $V_{LVD0}$ ) for LVD0 are suitable, you can use LVD0 and LVD1 in combination.

- LVD0: Reset mode, LVD1: Off
- LVD0: Reset mode, LVD1: Reset mode (Condition:  $V_{LVD0} < V_{LVD1}$ )

The following settings are prohibited:

- LVD0: Reset mode, LVD1: Interrupt mode (Condition:  $V_{LVD0} > V_{LVD1}$ )
- LVD0: Reset mode, LVD1: Reset mode (Condition:  $V_{LVD0} > V_{LVD1}$ )

### 3. LVD Operation

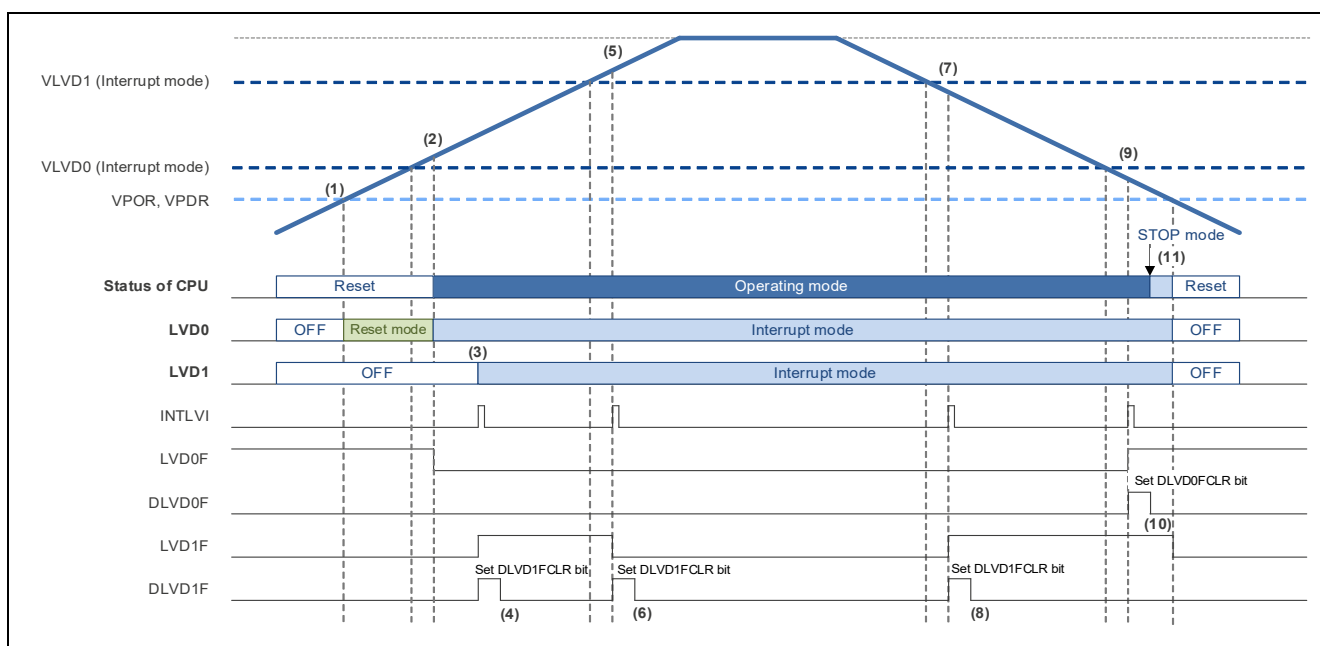
This section explains how LVD0 and LVD1 work in combination.

#### 3.1 LVD0: Interrupt mode, LVD1: Interrupt mode

Figure 3-1 shows the operation of the LVDs when LVD0 and LVD1 are both set to interrupt mode with the condition  $V_{LVD0} < V_{LVD1}$ .

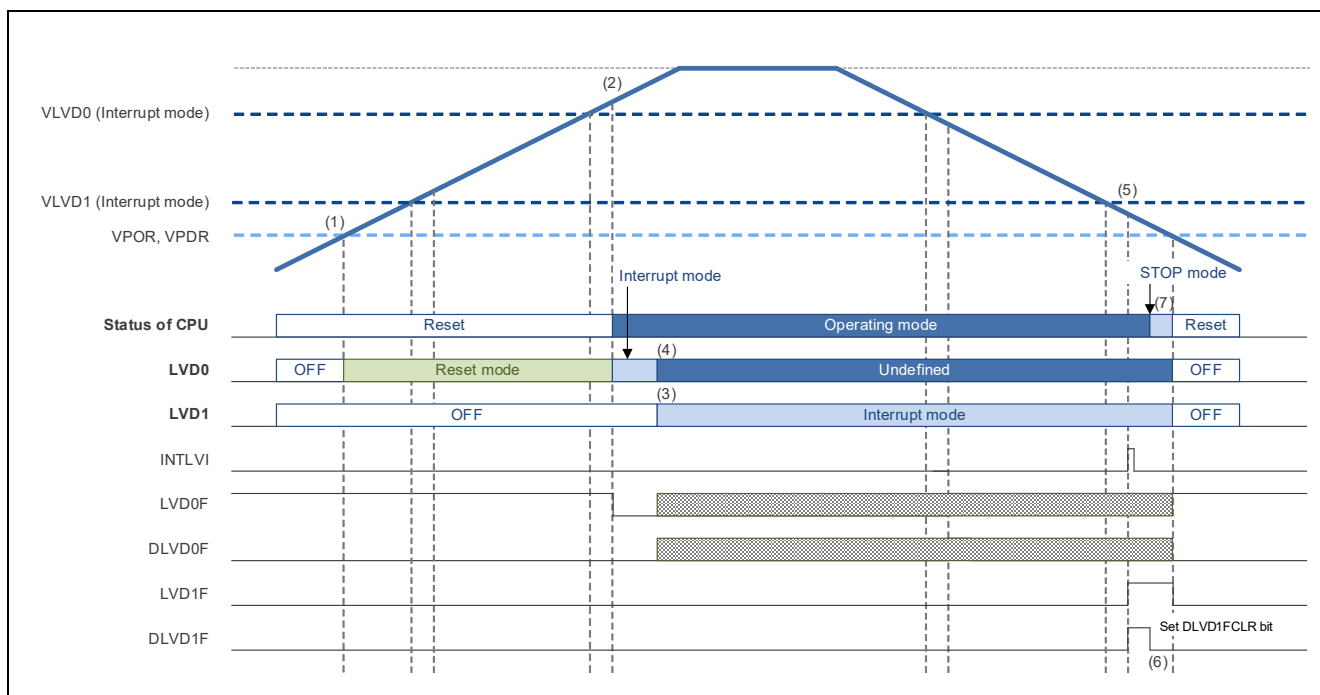
Figure 3-2 shows the operation of the LVDs when LVD0 and LVD1 are both set to interrupt mode with the condition  $V_{LVD0} > V_{LVD1}$ .

Figure 3-1 LVD operation when LVD0 and LVD1 are in interrupt mode with the condition  $V_{LVD0} < V_{LVD1}$



- (1) LVD0 keeps the CPU in reset status.
- (2) LVD0 detects  $V_{DD} \geq V_{LVD0}$  and releases reset status.
- (3) LVD1 is activated by a user program. When the stabilization time has elapsed, LVD1 becomes active, detects  $V_{DD} < V_{LVD1}$ , and issues an interrupt request signal (INTLVD).
- (4) A user program sets the DLVD1FCLR bit of the LVDFCLR register and clears the DLVD1F flag. The user program continues running as long as  $V_{LVD0} \leq V_{DD} < V_{LVD1}$ .
- (5) LVD1 detects  $V_{DD} \geq V_{LVD1}$  and issues an interrupt request signal (INTLVD).
- (6) A user program sets the DLVD1FCLR bit of the LVDFCLR register and clears the DLVD1F flag. The user program continues running as long as  $V_{DD} \geq V_{LVD1}$ .
- (7) LVD1 detects  $V_{DD} < V_{LVD1}$  and issues an interrupt request signal (INTLVD).
- (8) A user program sets the DLVD1FCLR bit of the LVDFCLR register and clears the DLVD1F flag. The user program continues running as long as  $V_{LVD0} \leq V_{DD} < V_{LVD1}$ .
- (9) LVD0 detects  $V_{DD} < V_{LVD0}$  and issues an interrupt request signal (INTLVD).
- (10) A user program sets the DLVD0FCLR bit of the LVDFCLR register and clears the DLVD0F flag. The user program continues running as long as  $V_{DD} < V_{LVD0}$ .
- (11) After executing the processing in (10), the CPU enters STOP mode.

Note: If LVD1 is set while  $V_{DD} \geq V_{LVD1}$ , no interrupt request signal is issued in steps (3) and (5), making steps (4) and (6) unnecessary.

Figure 3-2 LVD operation when LVD0 and LVD1 are in interrupt mode with the condition  $V_{LVD0} > V_{LVD1}$ 

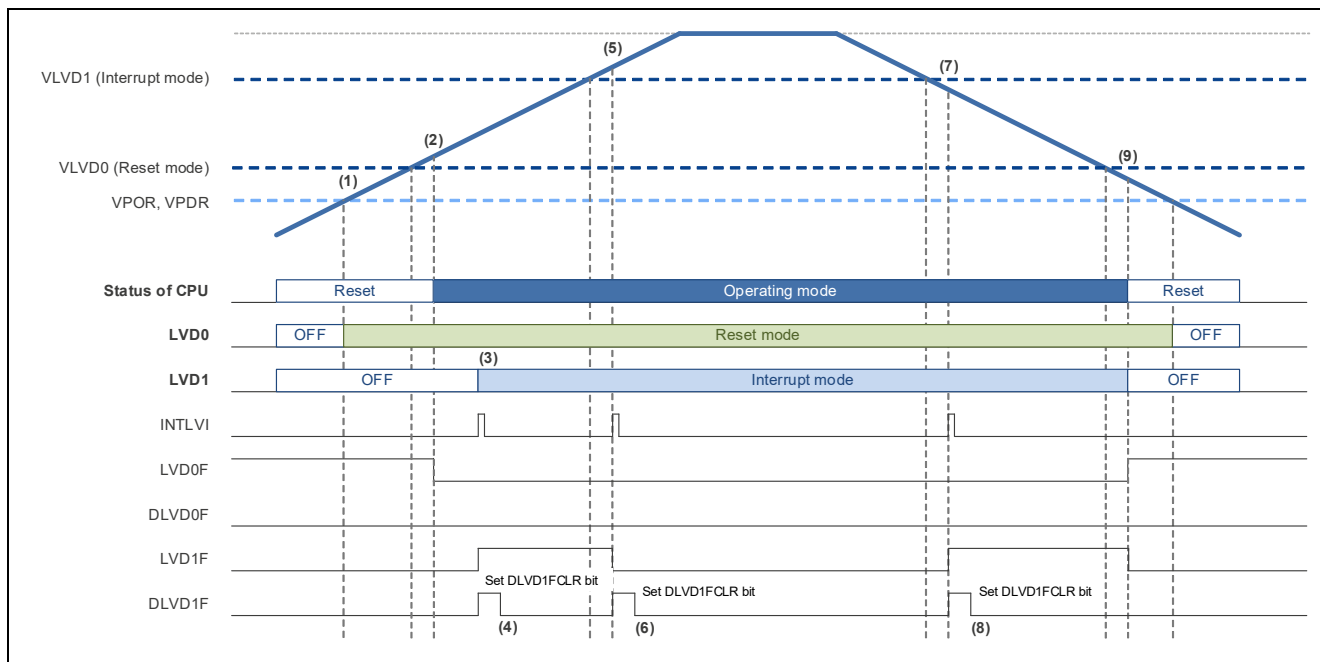
- (1) LVD0 keeps the CPU in reset status.
- (2) LVD0 detects  $V_{DD} \geq V_{LVD0}$  and releases reset status.
- (3) LVD1 is activated by a user program. When the stabilization time has elapsed, LVD1 becomes active. LVD1 does not issue an interrupt request signal (INTLVD) until  $V_{DD} < V_{LVD1}$  is detected.
- (4) LVD0 is undefined. Do not use an interrupt request signal (INTLVD) issued by LVD0 during this undefined period.
- (5) LVD1 detects  $V_{DD} < V_{LVD1}$  and issues an interrupt request signal (INTLVD).
- (6) A user program sets the DLVD1FCLR bit of the LVDFCLR register and clears the DLVD1F flag. The user program continues running as long as  $V_{DD} < V_{LVD1}$ .
- (7) After executing the processing in (6), the CPU enters STOP mode.

### 3.2 LVD0: Reset mode, LVD1: Interrupt mode

Figure 3-3 shows the operation of the LVDs when LVD0 is set to reset mode and LVD1 is set to interrupt mode with the condition  $V_{LVD0} < V_{LVD1}$ .

Note that you cannot set LVD0 to reset mode and LVD1 to interrupt mode with the condition  $V_{LVD0} > V_{LVD1}$ .

Figure 3-3 LVD operation with LVD0 in reset mode and LVD1 in interrupt mode with the condition  $V_{LVD0} < V_{LVD1}$



- (1) LVD0 keeps the CPU in reset status.
- (2) LVD0 detects  $V_{DD} \geq V_{LVD0}$  and releases reset status.
- (3) LVD1 is activated by a user program. When the stabilization time has elapsed, LVD1 becomes active, detects  $V_{DD} < V_{LVD1}$ , and issues an interrupt request signal (INTLVD).
- (4) A user program sets the DLVD1FCLR bit of the LVDFCLR register and clears the DLVD1F flag. The user program continues running as long as  $V_{LVD0} \leq V_{DD} < V_{LVD1}$ .
- (5) LVD1 detects  $V_{DD} \geq V_{LVD1}$  and issues an interrupt request signal (INTLVD).
- (6) A user program sets the DLVD1FCLR bit of the LVDFCLR register and clears the DLVD1F flag. The user program continues running as long as  $V_{DD} \geq V_{LVD1}$ .
- (7) LVD1 detects  $V_{DD} < V_{LVD1}$  and issues an interrupt request signal (INTLVD).
- (8) A user program sets the DLVD1FCLR bit of the LVDFCLR register and clears the DLVD1F flag. The user program continues running as long as  $V_{LVD0} \leq V_{DD} < V_{LVD1}$ .
- (9) LVD0 detects  $V_{DD} < V_{LVD0}$  and generates an internal reset. LVD0 maintains a reset state until  $V_{DD} \geq V_{LVD0}$ .

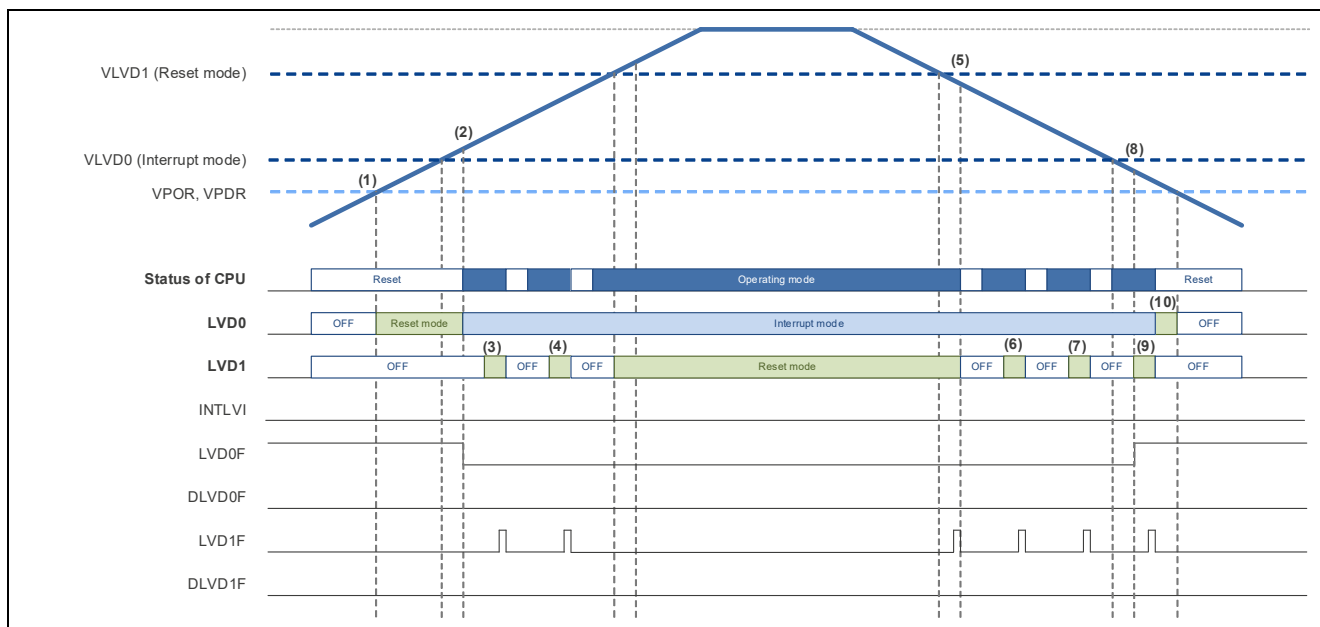
Note: If LVD1 is set while  $V_{DD} \geq V_{LVD1}$ , no interrupt request signal is issued in steps (3) and (5), making steps (4) and (6) unnecessary.

### 3.3 LVD0: Interrupt mode, LVD1: Reset mode

Figure 3-4 shows the operation of the LVDs when LVD0 is set to interrupt mode and LVD1 is set to reset mode with the condition  $V_{LVD0} < V_{LVD1}$ .

Figure 3-5 shows the operation of the LVDs when LVD0 is set to interrupt mode and LVD1 is set to reset mode with the condition  $V_{LVD0} > V_{LVD1}$ .

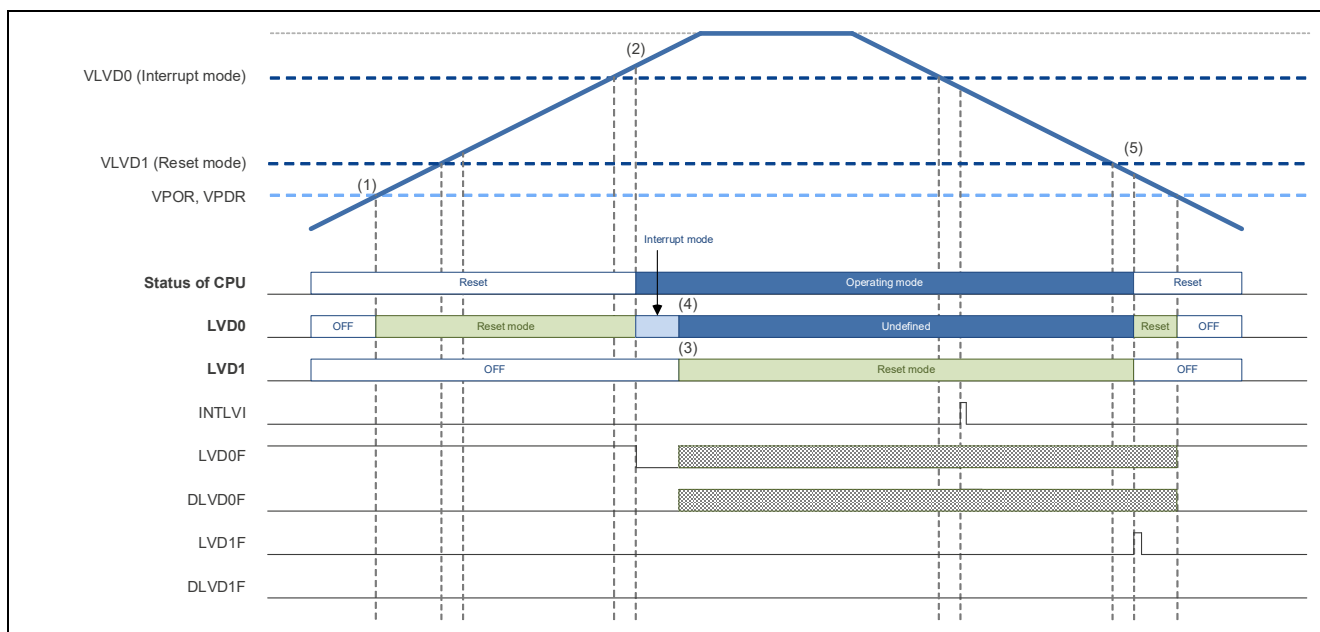
Figure 3-4 LVD operation with LVD0 in interrupt mode and LVD1 in reset mode with the condition  $V_{LVD0} < V_{LVD1}$



- (1) LVD0 keeps the CPU in reset status.
- (2) LVD0 detects  $V_{DD} \geq V_{LVD0}$  and releases reset status.
- (3) LVD1 is activated by a user program. When the stabilization time has elapsed, LVD1 becomes active, detects  $V_{DD} < V_{LVD1}$ , and generates an internal reset.
- (4) Step (3) repeats until LVD1 detects  $V_{DD} \geq V_{LVD1}$ .
- (5) LVD1 detects  $V_{DD} < V_{LVD1}$  and generates an internal reset.
- (6) LVD1 is activated by a user program. When the stabilization time has elapsed, LVD1 becomes active, detects  $V_{DD} < V_{LVD1}$ , and generates an internal reset.
- (7) Step (6) repeats until LVD0 detects  $V_{DD} < V_{LVD0}$ .
- (8) LVD0 detects  $V_{DD} < V_{LVD0}$  and issues an interrupt request signal (INTLVD).
- (9) LVD1 detects  $V_{DD} < V_{LVD1}$  and generates an internal reset.
- (10) The reset causes LVD0 to change from interrupt mode to reset mode. LVD0 maintains a reset state until  $V_{DD} \geq V_{LVD0}$ .

Note: If LVD1 is set while  $V_{DD} \geq V_{LVD1}$ , no internal reset is generated in step (3). In this case, the processing in step (3) does not repeat in step (4).

Figure 3-5 LVD operation with LVD0 in interrupt mode and LVD1 in reset mode with the condition  $V_{LVD0} > V_{LVD1}$



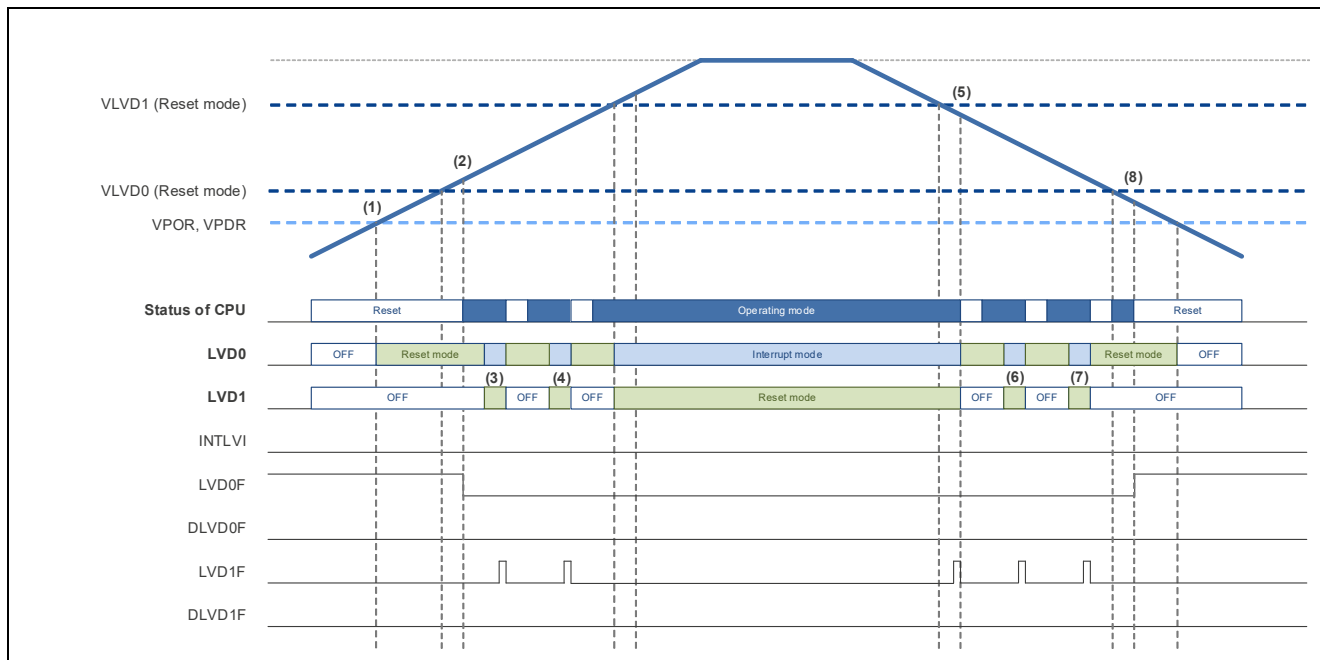
- (1) LVD0 keeps the CPU in reset status.
- (2) LVD0 detects  $V_{DD} \geq V_{LVD0}$  and releases reset status.
- (3) LVD1 is activated by a user program. LVD1 becomes active when the stabilization time has elapsed.
- (4) LVD0 is undefined. Do not use an interrupt request signal (INTLVD) issued by LVD0 during this undefined period.
- (5) LVD1 detects  $V_{DD} < V_{LVD1}$  and generates a reset.

### 3.4 LVD0: Reset mode, LVD1: Reset mode

Figure 3-6 shows the operation of the LVDs when LVD0 and LVD1 are both set to reset mode with the condition  $V_{LVD0} < V_{LVD1}$ .

Note that you cannot set LVD0 and LVD1 to reset mode with the condition  $V_{LVD0} > V_{LVD1}$ .

Figure 3-6 LVD operation with LVD0 and LVD1 in reset mode with the condition  $V_{LVD0} < V_{LVD1}$



- (1) LVD0 keeps the CPU in reset status.
- (2) LVD0 detects  $V_{DD} \geq V_{LVD0}$  and releases reset status.
- (3) LVD1 is activated by a user program. When the stabilization time has elapsed, LVD1 becomes active, detects  $V_{DD} < V_{LVD1}$ , and generates an internal reset.
- (4) Step (3) repeats until LVD1 detects  $V_{DD} \geq V_{LVD1}$ .
- (5) LVD1 detects  $V_{DD} < V_{LVD1}$  and generates an internal reset.
- (6) LVD1 is activated by a user program. When the stabilization time has elapsed, LVD1 becomes active, detects  $V_{DD} < V_{LVD1}$ , and generates an internal reset.
- (7) Step (6) repeats until LVD0 detects  $V_{DD} < V_{LVD0}$ .
- (8) LVD0 detects  $V_{DD} < V_{LVD0}$  and generates an internal reset. LVD0 maintains a reset state until  $V_{DD} \geq V_{LVD0}$ .

Note: If LVD1 is set while  $V_{DD} \geq V_{LVD1}$ , no internal reset is generated in step (3). In this case, the processing in step (3) does not repeat in step (4).

### 3.5 Voltage fluctuation during supply voltage rise

Systems that exhibit a degree of fluctuation in the vicinity of the detection voltages of LVD0 and LVD1 ( $V_{LVD0}$  and  $V_{LVD1}$ ) might repeatedly enter and exit reset status. By taking the following steps, you can set an arbitrary time that must elapse after exiting reset status before the RL78/G23 unit begins operation. Measure in advance the time the power supply voltage takes to reach  $V_{DD} \geq V_{LVD0}$  or  $V_{DD} \geq V_{LVD1}$ , and use the results to determine the time until RL78/G23 operation.

- (1) The CPU exits reset mode.
- (2) Check the RESF register and PORSR register to determine the cause of the reset.  
If the cause of the reset is POR or LVD, execute the processing in steps (3) and (4). If the cause of the reset is another internal reset, execute the processing from step (5) onward.
- (3) Set the timer array unit to interval timer mode and start the counting process.
- (4) Wait until the timer array unit issues an interrupt request signal. If a reset occurs while waiting, return to step (1).
- (5) LVD1 is activated by a user program.
- (6) Wait until the stabilization wait time of LVD1 (500  $\mu$ s) elapses as in steps (3) and (4).
- (7) Start the initialization of ports and peripheral functions.
- (8) Run the user program.

### 3.6 LVD interrupt processing

LVD0 and LVD1 share an interrupt vector (INTLVI). For this reason, if you use LVD0 and LVD1 in interrupt mode, interrupt processing must include determining the cause of the interrupt. Run user programs for tasks such as data storage processing after determining the cause of the interrupt.

- (1) Read the interrupt detection flag of LVD0 (DLVD0F bits).
- (2) If the interrupt is determined to be generated by LVD0, read the voltage detection flag (LVD0F bit) and check the relationship between the power supply voltage and  $V_{LVD0}$ .
- (3) Read the LVD1 interrupt detection flag (DLVD1F bit).
- (4) If a LVD1 interrupt is detected, read the voltage detection flag (LVD1F bit) and check the relationship between the power supply voltage and  $V_{LVD1}$ .
- (5) Set the DLVD0FCLR and DLVD1FCLR bits of the LVD detection to 1, and clear the interrupt detection flags of LVD0 and LVD1 (the DLVD0F and DLVD1F bits).
- (6) Run a user program such as data storage processing according to the results of steps (1) to (4).

#### 4. Reference Documents

RL78/G23 User's Manual: Hardware (R01UH0896J)

RL78 family user's manual software (R01US0015J)

The latest versions can be downloaded from the Renesas Electronics website.

Technical update

The latest versions can be downloaded from the Renesas Electronics website.

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Nov. 19. 21	—	First Edition

# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

## 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

## 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

## 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

## 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

## 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

## 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

## 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

## 8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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