# RL78/G14, R8C/36M Group

## Migration Guide from R8C to RL78: Data Transfer Controller

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### Abstract

This document describes how to migrate from the R8C/36M Group data transfer controller (DTC) to the RL78/G14 data transfer controller (DTC).

### Products

RL78/G14, R8C/36M Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

## Contents

## 1. Differences Between the R8C/36M Group and RL78/G14

Table 1.1 lists the differences between the R8C/36M Group DTC and RL78/G14 DTC.

**Table 1.1 Differences**

| Item | R8C/36M Group | RL78/G14 |
|---|---|---|
| Activation sources | 39 | • 31 (Note 1)<br>• 39 (Note 2) |
| Transferable address space | 64 Kbytes (00000h to 0FFFFh) | 64 Kbytes (00000h to 0FFFFh, excluding general-purpose registers) |
| Maximum size of block to be transferred | • Normal mode: 256 bytes<br>• Repeat mode: 255 bytes | • Normal mode (8-bit transfer): 256 bytes<br>• Normal mode (16-bit transfer): 512 bytes |
| Unit of transfers | Byte | 8 bits/16 bits |
| Power control/DTC operation in standby mode | • Wait mode: DTC activation sources are not generated before entering wait mode or during wait mode<br>• Stop mode: DTC activation sources are not generated before entering stop mode or during stop mode | • HALT mode: Enabled (Note 3)<br>• STOP mode: Enabled<br>• SNOOZE mode: Disabled (Note 4) |
| DTC control area, DTC vector table area | Fixed | Relocatable (RAM address set by the DTCBAR register) |

Note: 1. For 30-, 32-, 36-, 40-, 44-, 48-, 52-, and 64-pin packages only.
2. For 80 and 100-pin packages only.
3. RTC operation is disabled in low power consumption RTC mode (the RTCLPC bit in the OSMC register is 1).
4. DTC activation sources can be accepted.

## 2. Register Compatibility

Register compatibility between the R8C/36M Group DTC and RL78/G14 DTC is listed in Table 2.1.

**Table 2.1 Register Compatibility**

| Item | R8C/36M Group | RL78/G14 |
|---|---|---|
| Data block size setting | • DTBLSj register | • DTBLSj register (Note) |
| DTC activation enable register | • DTCENi register (i = 0 to 6) | • DTCENi register (i = 0 to 4) |
| Non-maskable interrupt generate | • DTCTL register<br>NMIF bit | N/A |
| Data size select | N/A | • DTCCRj register<br>SZ bit |
| DTC base address register | N/A | • DTCBAR register |

j = 0 to 23
Note: For 8-bit transfer, 1 to 256 bytes can be specified. For 16-bit transfer, 2 to 512 bytes can be specified.

# 3. Comparison of DTC Settings

## 3.1 DTC Activation Enable

Set the DTCENi register to enable or disable DTC activations by interrupt sources (R8C/36M Group: i = 0 to 6, RL78/G14: i = 0 to 4). Interrupt sources selected by setting bits DTCENi0 to DTCENi7 in the DTCENi register differ for the R8C/36M Group and RL78/G14.

Table 3.1 lists the compatibility between R8C/36M Group interrupt sources and bits DTCENi0 to DTCENi7. Table 3.2 lists the compatibility between RL78/G14 interrupt sources and bits DTCENi0 to DTCENi7.

**Table 3.1 Correspondences Between Bits DTCENi0 to DTCENi7 (i = 0 to 6) and Interrupt Sources**

| Register | DTCENi7 Bit | DTCENi6 Bit | DTCENi5 Bit | DTCENi4 Bit | DTCENi3 Bit | DTCENi2 Bit | DTCENi1 Bit | DTCENi0 Bit |
|---|---|---|---|---|---|---|---|---|
| DTCEN0 | $\overline{INT0}$ | $\overline{INT1}$ | $\overline{INT2}$ | $\overline{INT3}$ | $\overline{INT4}$ | N/A | N/A | N/A |
| DTCEN1 | Key input | A/D conversion | UART0 reception | UART0 transmission | UART1 reception | UART1 transmission | UART2 reception | UART2 transmission |
| DTCEN2 | SSU/$I^2C$ bus receive data full | SSU/$I^2C$ bus transmit data empty | Voltage Monitor 2/comparator A2 | Voltage Monitor 1/comparator A1 | N/A | N/A | Timer RC input-capture/ compare-match A | Timer RC input-capture/ compare-match B |
| DTCEN3 | Timer RC input-capture/ compare-match C | Timer RC input-capture/ compare-match D | Timer RD0 input-capture/ compare-match A | Timer RD0 input-capture/ compare-match B | Timer RD0 input-capture/ compare-match C | Timer RD0 input-capture/ compare-match D | Timer RD1 input-capture/ compare-match A | Timer RD1 input-capture/ compare-match B |
| DTCEN4 | Timer RD1 input-capture/ compare-match C | Timer RD1 input-capture/ compare-match D | N/A | N/A | N/A | N/A | N/A | N/A |
| DTCEN5 | N/A | N/A | Timer RE | Timer RF | Timer RF compare-match 0 | Timer RF compare-match 1 | Timer RF capture | Timer RG input-capture/ compare-match A |
| DTCEN6 | Timer RG input-capture/ compare-match B | Timer RA | N/A | Timer RB | Flash ready status | N/A | N/A | N/A |

**Table 3.2 Correspondences Between Interrupt Sources and Bits DTCENi0 to DTCENi7**

| Register | DTCENi7 Bit | DTCENi6 Bit | DTCENi5 Bit | DTCENi4 Bit | DTCENi3 Bit | DTCENi2 Bit | DTCENi1 Bit | DTCENi0 Bit |
|---|---|---|---|---|---|---|---|---|
| DTCEN0 | Reserved | INTP0 | INTP1 | INTP2 | INTP3 | INTP4 | INTP5 | INTP6 |
| DTCEN1 | INTP7 | Key input | A/D conversion end | UART0 reception transfer end/ CSI01 transfer end or buffer empty/ IIC01 transfer end | UART0 transmission transfer end/ CSI00 transfer end or buffer empty/ IIC00 transfer end | UART1 reception transfer end/ CSI11 transfer end or buffer empty/ IIC11 transfer end | UART1 transmission transfer end/ CSI10 transfer end or buffer empty/ IIC10 transfer end | UART2 reception transfer end/ CSI21 transfer end or buffer empty/ IIC21 transfer end |
| DTCEN2 | UART2 transmission transfer end/CSI20 transfer end or buffer empty/ IIC20 transfer end | UART3 reception transfer end/ CSI31 transfer end or buffer empty/ IIC31 transfer end (Note 1) | UART3 transmission transfer end/ CSI30 transfer end or buffer empty/ IIC30 transfer end (Note 1) | End of channel 0 of timer array unit 0 count or capture | End of channel 1 of timer array unit 0 count or capture | End of channel 2 of timer array unit 0 count or capture | End of channel 3 of timer array unit 0 count or capture | End of channel 0 of timer array unit 1 count or capture |
| DTCEN3 | End of channel 1 of timer array unit 1 count or capture (Note 1) | End of channel 2 of timer array unit 1 count or capture (Note 1) | End of channel 3 of timer array unit 1 count or capture (Note 1) | Timer RD compare match A0 | Timer RD compare match B0 | Timer RD compare match C0 | Timer RD compare match D0 | Timer RD compare match A1 |
| DTCEN4 | Timer RD compare match B1 | Timer RD compare match C1 | Timer RD compare match D1 | Timer RG compare match A | Timer RG compare match B | Timer RJ0 underflow | Comparator detection 0 (Note 2) | Comparator detection 1 (Note 2) |

i = 0 to 4

Notes: 1. For 80 and 100-pin packages only.
2. Only applicable for MCUs with a code flash memory of 96 KB or more.

## 3.2 Transfer Size

In RL78/G14 normal mode, transfer size can be specified as 8-bit transfer or 16-bit transfer. Set the SZ bit in the DTCCRj register (j = 0 to 23) to specify the transfer size. Table 3.3 lists the functions of the SZ bit.

**Table 3.3 SZ Bit Functions**

| SZ Bit | Transfer Data Size Selection |
|---|---|
| 0 | 8 bits |
| 1 | 16 bits |

## 3.3 Allocation of DTC Control Data Area and DTC Vector Table Area

The DTC control data area and DTC vector table area are allocated differently between the R8C/36M Group and RL78/G14. In the R8C/36M Group, they are allocated at fixed addresses. In RL78/G14, set the DTCBAR register to specify the vector address to store the start address of the DTC control data area, and the DTC control data area address. The DTCBAR register value is used as a higher 8-bit address to generate a 16-bit address. Figure 3.1 shows a memory map when the DTCBAR register is set to FBH.

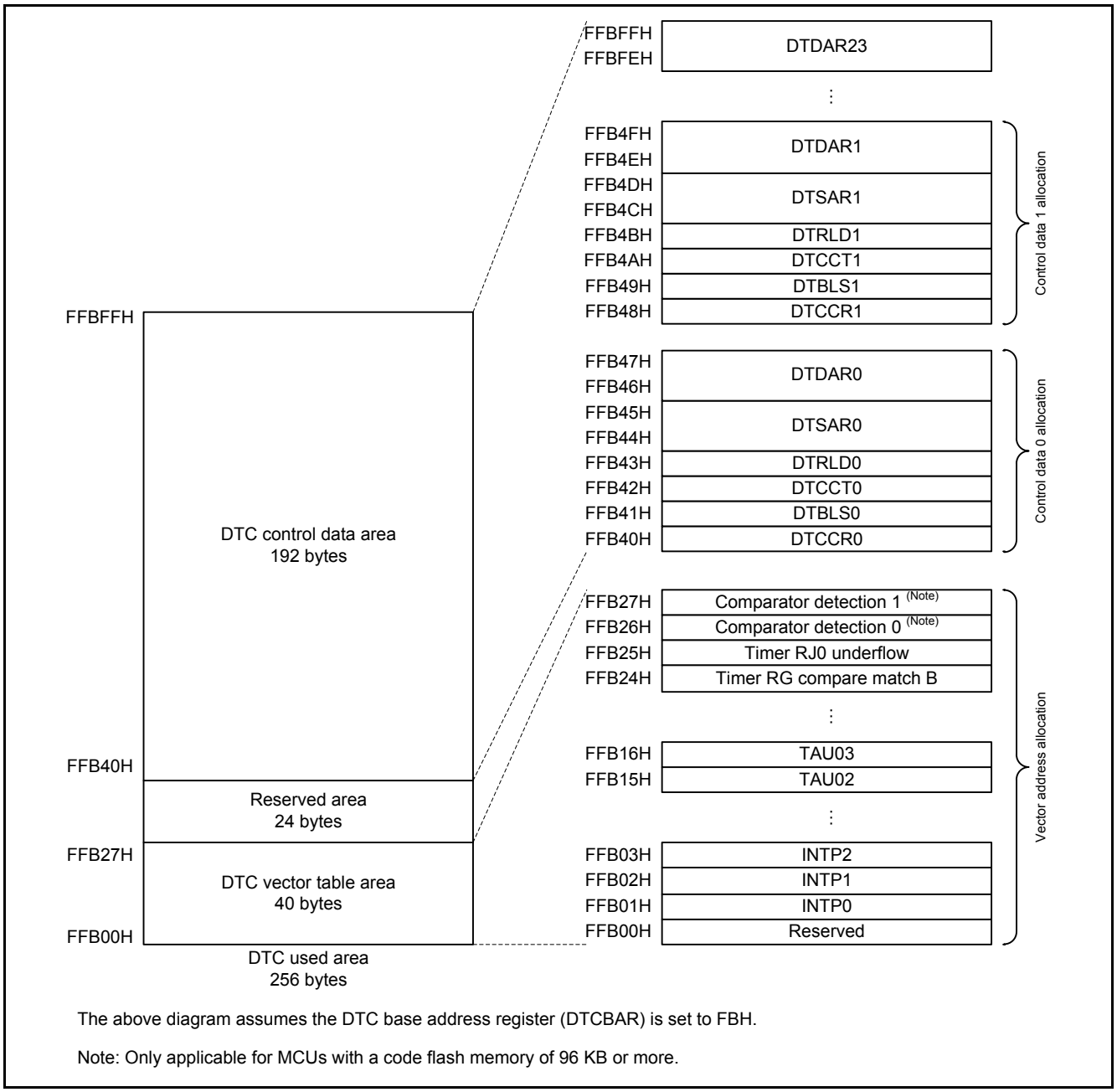


**Figure 3.1 Memory Map When the DTCBAR Register is Set to FBH**

# 4. Differences in DTC Operation

## 4.1 Activation Sources

### 4.1.1 R8C/36M Group

If multiple activation sources are simultaneously generated, the DTC activation will be performed according to the DTC activation source priority. Table 4.1 and Table 4.2 list the DTC activation sources and DTC vector addresses.

**Table 4.1 DTC Activation Sources and DTC Vector Address (1/2)**

| Interrupt Request Source | Interrupt Name | Source No. | DTC Vector Address | Priority |
|---|---|---|---|---|
| External input | $\overline{\text{INT0}}$ | 0 | 2C00h | High ↑ |
| | $\overline{\text{INT1}}$ | 1 | 2C01h | |
| | $\overline{\text{INT2}}$ | 2 | 2C02h | |
| | $\overline{\text{INT3}}$ | 3 | 2C03h | |
| | $\overline{\text{INT4}}$ | 4 | 2C04h | |
| Key input | Key input | 8 | 2C08h | |
| A/D | A/D conversion | 9 | 2C09h | |
| UART0 | UART0 reception | 10 | 2C0Ah | |
| | UART0 transmission | 11 | 2C0Bh | |
| UART1 | UART1 reception | 12 | 2C0Ch | |
| | UART1 transmission | 13 | 2C0Dh | |
| UART2 | UART2 reception | 14 | 2C0Eh | |
| | UART2 transmission | 15 | 2C0Fh | |
| SSU/$I^2C$ bus | Receive data full | 16 | 2C10h | |
| | Transmit data empty | 17 | 2C11h | |
| Voltage detection circuit | Voltage monitor 2/comparator A2 | 18 | 2C12h | |
| | Voltage monitor 1/comparator A1 | 19 | 2C13h | |
| Timer RC | Input-capture/compare-match A | 22 | 2C16h | |
| | Input-capture/compare-match B | 23 | 2C17h | |
| | Input-capture/compare-match C | 24 | 2C18h | |
| | Input-capture/compare-match D | 25 | 2C19h | |
| Timer RD0 | Input-capture/compare-match A | 26 | 2C1Ah | |
| | Input-capture/compare-match B | 27 | 2C1Bh | |
| | Input-capture/compare-match C | 28 | 2C1Ch | |
| | Input-capture/compare-match D | 29 | 2C1Dh | |
| Timer RD1 | Input-capture/compare-match A | 30 | 2C1Eh | |
| | Input-capture/compare-match B | 31 | 2C1Fh | |
| | Input-capture/compare-match C | 32 | 2C20h | |
| | Input-capture/compare-match D | 33 | 2C21h | |

**Table 4.2 DTC Activation Sources and DTC Vector Address (2/2)**

| Interrupt Request Source | Interrupt Name | Source No. | DTC Vector Address | Priority |
|---|---|---|---|---|
| Timer RE | Timer RE | 42 | 2C2Ah | ↓ |
| Timer RF | Timer RF | 43 | 2C2Bh | |
| | Compare-match 0 | 44 | 2C2Ch | |
| | Compare-match 1 | 45 | 2C2Dh | |
| | Capture | 46 | 2C2Eh | |
| Timer RG | Input-capture/compare-match A | 47 | 2C2Fh | |
| | Input-capture/compare-match B | 48 | 2C30h | |
| Timer RA | Timer RA | 49 | 2C31h | |
| Timer RB | Timer RB | 51 | 2C33h | |
| Flash memory | Flash ready status | 52 | 2C34h | Low |

### 4.1.2 RL78/G14

If DTC activation sources conflict, their priority levels are determined in order to select the source for activation when the CPU acknowledges the DTC transfer. Table 4.3 and Table 4.4 list the DTC activation sources and vector addresses.

**Table 4.3 DTC Activation Sources and Vector Address (1/2)**

| DTC Activation Sources | Source No. | Vector Address | Priority |
|---|---|---|---|
| Reserved | 0 | Address set in DTCBAR register +00H | High |
| INTP0 | 1 | Address set in DTCBAR register +01H | ↑ |
| INTP1 | 2 | Address set in DTCBAR register +02H | |
| INTP2 | 3 | Address set in DTCBAR register +03H | |
| INTP3 | 4 | Address set in DTCBAR register +04H | |
| INTP4 | 5 | Address set in DTCBAR register +05H | |
| INTP5 | 6 | Address set in DTCBAR register +06H | |
| INTP6 | 7 | Address set in DTCBAR register +07H | |
| INTP7 | 8 | Address set in DTCBAR register +08H | |
| Key input | 9 | Address set in DTCBAR register +09H | |
| A/D conversion end | 10 | Address set in DTCBAR register +0AH | |
| UART0 reception transfer end/CSI01 transfer end or buffer empty/IIC01 transfer end | 11 | Address set in DTCBAR register +0BH | |
| UART0 transmission transfer end/CSI00 transfer end or buffer empty/IIC00 transfer end | 12 | Address set in DTCBAR register +0CH | |
| UART1 reception transfer end/CSI11 transfer end or buffer empty/IIC11 transfer end | 13 | Address set in DTCBAR register +0DH | |
| UART1 transmission transfer end/CSI10 transfer end or buffer empty/IIC10 transfer end | 14 | Address set in DTCBAR register +0EH | |
| UART2 reception transfer end/CSI21 transfer end or buffer empty/IIC21 transfer end | 15 | Address set in DTCBAR register +0FH | |
| UART2 transmission transfer end/CSI20 transfer end or buffer empty/IIC20 transfer end | 16 | Address set in DTCBAR register +10H | |
| UART3 reception transfer end/CSI31 transfer end or buffer empty/IIC31 transfer end (Note) | 17 | Address set in DTCBAR register +11H | |
| UART3 transmission transfer end/CSI30 transfer end or buffer empty/IIC30 transfer end (Note) | 18 | Address set in DTCBAR register +12H | |
| End of channel 0 of timer array unit 0 count or capture | 19 | Address set in DTCBAR register +13H | |
| End of channel 1 of timer array unit 0 count or capture | 20 | Address set in DTCBAR register +14H | |
| End of channel 2 of timer array unit 0 count or capture | 21 | Address set in DTCBAR register +15H | |
| End of channel 3 of timer array unit 0 count or capture | 22 | Address set in DTCBAR register +16H | |

Note: Applicable for 80-, and 100-pin packages only.

**Table 4.4 DTC Activation Sources and Vector Address (2/2)**

| DTC Activation Sources | Source No. | Vector Address | Priority |
|---|---|---|---|
| End of channel 0 of timer array unit 1 count or capture (Note 1) | 23 | Address set in DTCBAR register +17H | |
| End of channel 1 of timer array unit 1 count or capture (Note 1) | 24 | Address set in DTCBAR register +18H | |
| End of channel 2 of timer array unit 1 count or capture (Note 1) | 25 | Address set in DTCBAR register +19H | |
| End of channel 3 of timer array unit 1 count or capture (Note 1) | 26 | Address set in DTCBAR register +1AH | |
| Timer RD compare match A0 | 27 | Address set in DTCBAR register +1BH | |
| Timer RD compare match B0 | 28 | Address set in DTCBAR register +1CH | |
| Timer RD compare match C0 | 29 | Address set in DTCBAR register +1DH | |
| Timer RD compare match D0 | 30 | Address set in DTCBAR register +1EH | |
| Timer RD compare match A1 | 31 | Address set in DTCBAR register +1FH | |
| Timer RD compare match B1 | 32 | Address set in DTCBAR register +20H | |
| Timer RD compare match C1 | 33 | Address set in DTCBAR register +21H | |
| Timer RD compare match D1 | 34 | Address set in DTCBAR register +22H | |
| Timer RG compare match A | 35 | Address set in DTCBAR register +23H | |
| Timer RG compare match B | 36 | Address set in DTCBAR register +24H | |
| Timer RJ0 underflow | 37 | Address set in DTCBAR register +25H | |
| Comparator detection 0 (Note 2) | 38 | Address set in DTCBAR register +26H | |
| Comparator detection 1 (Note 2) | 39 | Address set in DTCBAR register +27H | Low |

Notes: 1. Applicable for 80-, and 100-pin packages only.
2. Applicable for MCUs with a code flash memory greater than 96 KB only.

## 4.2 Allocation of DTC Control Data Area

### 4.2.1 R8C/36M Group

Control data is allocated from the start address in the following order: Registers DTCCRj, DTBLSj, DTCCTj, DTRLDj, DTSARj, and DTDARj (j = 0 to 23). Table 4.5 lists the control data allocation addresses.

**Table 4.5 R8C/36M Group Control Data Allocation Address**

| Register Symbol | DTCCRj | DTBLSj | DTCCTj | DTRLDj | DTSARj (Lower 8 Bits) | DTSARj (Higher 8 Bits) | DTDARj (Lower 8 Bits) | DTDARj (Higher 8 Bits) |
|---|---|---|---|---|---|---|---|---|
| DTCD0 | 2C40h | 2C41h | 2C42h | 2C43h | 2C44h | 2C45h | 2C46h | 2C47h |
| DTCD1 | 2C48h | 2C49h | 2C4Ah | 2C4Bh | 2C4Ch | 2C4Dh | 2C4Eh | 2C4Fh |
| DTCD2 | 2C50h | 2C51h | 2C52h | 2C53h | 2C54h | 2C55h | 2C56h | 2C57h |
| DTCD3 | 2C58h | 2C59h | 2C5Ah | 2C5Bh | 2C5Ch | 2C5Dh | 2C5Eh | 2C5Fh |
| … … | … … | … … | … … | … … | … … | … … | … … | … … |
| DTCD20 | 2CE0h | 2CE1h | 2CE2h | 2CE3h | 2CE4h | 2CE5h | 2CE6h | 2CE7h |
| DTCD21 | 2CE8h | 2CE9h | 2CEAh | 2CEBh | 2CECh | 2CEDh | 2CEEh | 2CEFh |
| DTCD22 | 2CF0h | 2CF1h | 2CF2h | 2CF3h | 2CF4h | 2CF5h | 2CF6h | 2CF7h |
| DTCD23 | 2CF8h | 2CF9h | 2CFAh | 2CFBh | 2CFCh | 2CFDh | 2CFEh | 2CFFh |

### 4.2.2 RL78/G14

Control data is allocated from the start address in the following order: Registers DTCCRj, DTBLSj, DTCCTj, DTRLDj, DTSARj, and DTDARj (j = 0 to 23). The higher 8 bits for start addresses 0 to 23 are set by the DTCBAR register, and the lower 8 bits are separately set according to the vector table assigned to each activation source. Table 4.6 lists the control data allocation address when the DTCBAR register is set to FBH.

The area to allocate the DTC control data and vector table depends on the MCU and use of conditions. For more information, refer to the RL78/G14 User's Manual: Hardware.

**Table 4.6 RL78/G14 Control Data Allocation Address**

| Start Address | DTCCRj | DTBLSj | DTCCTj | DTRLDj | DTSARj (Lower 8 Bits) | DTSARj (Higher 8 Bits) | DTDARj (Lower 8 Bits) | DTDARj (Higher 8 Bits) |
|---|---|---|---|---|---|---|---|---|
| 0 | FFB40H | FFB41H | FFB42H | FFB43H | FFB44H | FFB45H | FFB46H | FFB47H |
| 1 | FFB48H | FFB49H | FFB4AH | FFB4BH | FFB4CH | FFB4DH | FFB4EH | FFB4FH |
| 2 | FFB50H | FFB51H | FFB52H | FFB53H | FFB54H | FFB55H | FFB56H | FFB57H |
| 3 | FFB58H | FFB59H | FFB5AH | FFB5BH | FFB5CH | FFB5DH | FFB5EH | FFB5EH |
| … … | … … | … … | … … | … … | … … | … … | … … | … … |
| 20 | FFBE0H | FFBE1H | FFBE2H | FFBE3H | FFBE4H | FFBE5H | FFBE6H | FFBE7H |
| 21 | FFBE8H | FFBE9H | FFBEAH | FFBEBH | FFBECH | FFBEDH | FFBEEH | FFBEFH |
| 22 | FFBF0H | FFBF1H | FFBF2H | FFBF3H | FFBF4H | FFBF5H | FFBF6H | FFBF7H |
| 23 | FFBF8H | FFBF9H | FFBFAH | FFBFBH | FFBFCH | FFBFDH | FFBFEH | FFBFFH |

## 4.3 Differences in Normal Mode

### 4.3.1 R8C/36M Group

1 to 256 bytes of data are transferred by one activation.

### 4.3.2 RL78/G14

1 to 256 bytes of data are transferred by one activation during 8-bit transfer, and 2 to 512 bytes during 16-bit transfer.

## 4.4 Number of DTC Execution Cycles (Clocks)

The number of cycles (clocks) to read the control data when the DTC is activated differs between the R8C/36M Group and RL78/G14. Table 4.7 lists the differences in the number of control data read cycles (clocks).

**Table 4.7 Differences in the Number of Control Data Read Cycles**

| | R8C/36M Group | RL78/G14 |
|---|---|---|
| Control data read | 5 cycles | 4 clocks |

The number of cycles to read or write data differs between the R8C/36M Group and RL78/G14. Table 4.8 lists the number of clock cycles required for data read and write in the R8C/36M Group. Table 4.9 lists the number of clock cycles required for data read and write in RL78/G14.

**Table 4.8 R8C/36M Group Number of Clock Cycles Required for Data Read and Data Write**

| Operation | Unit of Transfers | Internal RAM (During DTC Transfers) | | Internal ROM (Program ROM) | Internal ROM (Data Flash) | SFR (Word Access) | | SFR (Byte Access) | SFR (DTC Control Data Area) | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Even address | Odd address | | | Even address | Odd address | | Even address | Odd address |
| Data read | 1-byte SK1 | 1 | | 1 | 2 | 2 | | 2 | 1 | |
| | 2-byte SK2 | 1 | 2 | 2 | 4 | 2 | 4 | 4 | 1 | 2 |
| Data write | 1-byte SL1 | 1 | | N/A | N/A | 2 | | 2 | 1 | |
| | 2-byte SL2 | 1 | 2 | N/A | N/A | 2 | 4 | 4 | 1 | 2 |

**Table 4.9 RL78/G14 Number of Clock Cycles Required for Data Read and Data Write**

| Operation | RAM | Code Flash Memory | Data Flash Memory | Special Function Register (SFR) | Extended Special Function Register (2nd SFR) | |
|---|---|---|---|---|---|---|
| | | | | | No Wait State | Wait States |
| Data read | 1 | 2 | 4 | 1 | 1 | 1 + number of wait states (Note) |
| Data write | 1 | N/A | N/A | 1 | 1 | 1 + number of wait states (Note) |

Note: The number of wait states differs depending on the specifications of the register allocated to the extended special function register (2nd SFR) to be accessed.

## 4.5 DTC Pending Instruction

Even if a DTC transfer request is generated, DTC transfer is held immediately after the instructions below. Also, the DTC is not activated between PREFIX instruction code and the instruction immediately after that code.

- Call/return instruction
- Unconditional branch instruction
- Conditional branch instruction
- Read access instruction for code flash memory
- Bit manipulation instructions for IFxx, MKxx, PRxx, and PSW, and 8-bit manipulation instruction that has the ES register as operand
- Instruction for accessing the data flash memory

Notes: 1. When a DTC transfer request is acknowledged, all interrupt requests are held until DTC transfer is completed.
2. While the DTC is held pending by the DTC pending instruction, all interrupt requests are held.

## 4.6 DTC Response Time

The DTC response time is the time from when the DTC activation source is detected until DTC transfer starts. The DTC response time does not include the number of DTC execution clocks.

Note that the response from the DTC may be further delayed under the conditions below. The number of delayed clock cycles differs depending on the conditions.

- When executing an instruction from the internal RAM
  Maximum response time: 20 clocks
- When executing a DTC pending instruction (refer to 4.5 DTC Pending Instruction)
  Maximum response time: Maximum response time for each condition + execution clock cycles for the instruction to be held under the condition.
- When accessing the TRJ0 register that wait occurs
  Maximum response time: Maximum response time for each condition + 1 clock

## 5. Reference Documents

User's Manual: Hardware

RL78/G14 User's Manual: Hardware Rev.2.00

R8C/36M Group User's Manual: Hardware Rev.1.01

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

## Website and Support

Renesas Electronics website

http://www.renesas.com

Inquiries

http://www.renesas.com/contact/

| REVISION HISTORY | RL78/G14, R8C/36M Group<br>Migration Guide from R8C to RL78: Data Transfer Controller |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | Dec. 2, 2013 | — | First edition issued |
| | | | |

## General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to a product with a different type number, confirm that the change will not lead to problems.
   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

# Notice

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