RL78/G14, H8/36109

Migration Guide from H8 to RL78: SCI3

Introduction

This application note describes how to migrate the serial communication interface 3 (SCI3) of the H8/36109 to the serial array unit (SAU) of the RL78/G14 (100-pin package).

Target Device

RL78/G14, H8/36109

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Functions of SCI3 of H8/36109 and SAU of RL78/G14

Table 1.1 shows the functions of the serial communication interface 3 (SCI3) of H8/36109, and Table 1.2 shows the functions of the serial array unit (SAU) of RL78/G14.

Table 1.1 Functions serial communication interface 3 (SCI3)

Function	Explanation
Asynchronous mode	In asynchronous mode, serial data communication can be carried out using standard asynchronous communication chips such as a UART or ACIA.
Clock synchronous mode	In clock synchronous mode, data is transmitted or received synchronous with clock pulses.
Multiprocessor Communication Function	Use of the multiprocessor communication function enables data transfer between a number of processors sharing communication lines by asynchronous serial communication using the multiprocessor format, in which a multiprocessor bit is added to the transfer data.

Table 1.2 Functions of Serial Array Unit (SAU)

Function	Explanation
3-wire serial I/O	This is a clocked communication function that uses three lines: serial clock (SCK) and serial data (SI and SO) lines.
UART	This is a start-stop synchronization function using two lines: serial data transmission (TXD) and serial data reception (RXD) lines.
Simplified I2C (only master function with a single master)	This is a clocked communication function to communicate with two or more devices by using two lines: serial clock (SCL) and serial data (SDA).
LIN Communication (Note)	LIN stands for Local Interconnect Network and is a low-speed (1 to 20 kbps) serial communication protocol designed to reduce the cost of an automobile network.

Note. The LIN-bus is accepted in UART0

Remarks1. For H8/36109, the distinction by channel (SCI3, SCI3_2, SCI3_3) is omitted.

Remarks2. For RL78/G14, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

Remarks3. The functions incorporated and port functions to use are different depending on the product. For details, refer to the appropriate user's manuals (hardware).

H8/36109 includes a serial communication interface 3 (SCI3), which has independent three channels. The SCI3 can handle both asynchronous and clock synchronous serial communication. A function for serial communication between multiple processors (multiprocessor communication function) is also provided. The basic function is the same for all three channels (SCI3, SCI3_2, SCI3_3).

Figure 1.1 shows a block diagram of SCI3. Separate explanations are not given in this section.

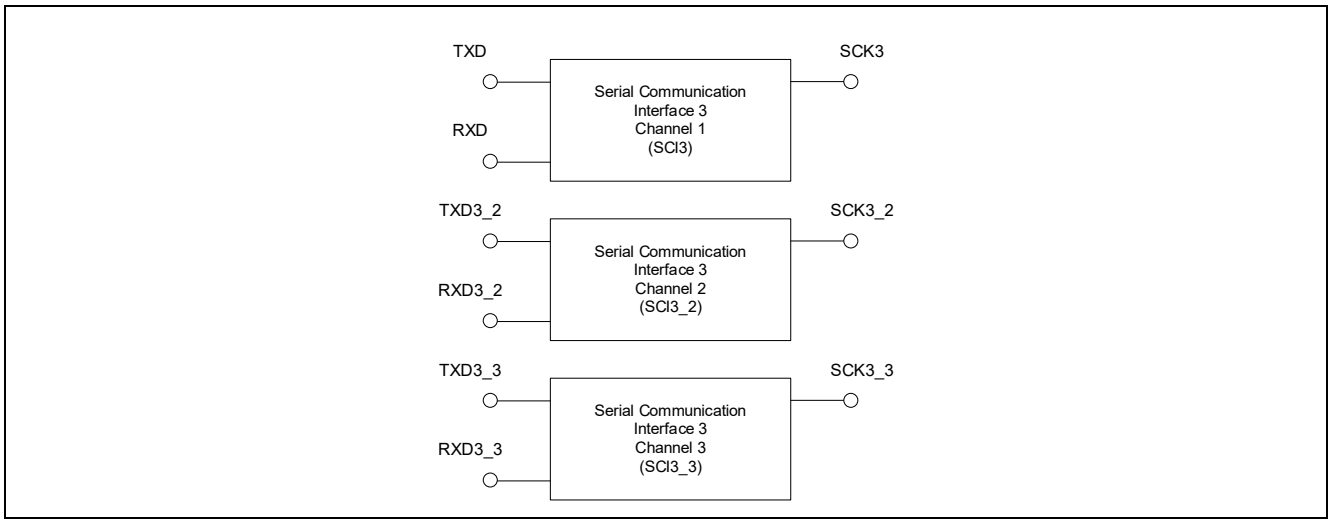

Figure 1.1 Block diagram of the serial communication interface 3 (SCI3)

A single serial array unit (SAU) in the RL78/G14 has up to four serial channels. Each channel can achieve 3-wire serial (CSI), UART, and simplified I2C communication. CSI and simplified I2C communication are implemented by one serial channels of SAU. UART communication is implemented by two serial channels of SAU.

Table 1.3 shows assignment of the functions supported by the RL78/G14 (100-pin product) for each channel.

Table 1.3 Function assignment of serial array unit (SAU)

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I^2C
0	0	CSI00	UART0 (Supporting LIN-bus)	IIC00
	1	CSI01		IIC01
	2	CSI10	UART1	IIC10
	3	CSI11		IIC11
1	0	CSI20	UART2	IIC20
	1	CSI21		IIC21
	2	CSI30	UART3	IIC30
	3	CSI31		IIC31

Table 1.4 shows the SAU functions corresponding to the SCI3.

Table 1.4 Correspondence between Functions

H8/36109 SCI3	RL78/G14 SAU
Asynchronous mode	UART
Clock synchronous mode	3-wire serial I/O (CSI)
Multiprocessor Communication Function	None (Substituted by UART and software processing)

The asynchronous mode of the SCI3 correspond to the UART of the SAU.

The clock synchronous mode of the SCI3 correspond to the 3-wire serial I/O (CSI)of the SAU.

The multiprocessor communication function of the SCI3 has no counterpart; it can be substituted by UART and software processing of the SAU.

2. Summary of Differences between Functions

Table 2.1 summarizes the differences between the functions SCI3 and SAU.

Table 2.1 Summary of Differences between Functions

Item	H8/36109 Serial communication interface 3 (SCI3)	RL78/G14 Serial array unit (SAU)
Data length	7 bit (Note1), 8 bit	7 bit, 8 bit, 9 bit (Note2)
Transfer clock source.	- On-chip baud rate generator - External clock	- Transfer clock (f_{TCLK}) - f_{SCK} (Slave transfer in CSI mode)
Count clock	φ, φ/4, φ/16, φ/64, SCK3	f_{TCLK} (f_{CLK} to $f_{CLK}/2^{15}$)
First bit of communication data	LSB	- LSB - MSB
Double-buffering	Yes	Yes
Output a clock of the same frequency as the bit rate	Yes	None
SNOOZE mode	None	Yes
Interrupt source	- Transmit-end - Transmit-data-empty - Receive-data-full - Overrun error - Framing error - Parity error	- Transfer end interrupt (Transmission, Reception) - Buffer empty interrupt - Error interrupt (Framing error, Parity error, Overrun error)
Noise canceller	Yes (Only for RXD_3)	Yes (RXDm pin)

Note1. For H8/36109, asynchronous mode only

Note2. For RL78/G14, UART0, UART2 only

Remark. For RL78/G14, m = 0, 1, 2, 3

2.1 Differences between asynchronous mode

The asynchronous mode of the SCI3 of the H8/36109 correspond to the UART of the SAU of the RL78/G14. Table 2.2 and Table 2.3 shows the differences between asynchronous mode.

Table 2.2 Differences between asynchronous mode (1/2)

Item	H8/36109 SCI3 Asynchronous mode	RL78/G14 Serial array unit (SAU) UART
Data length	7 bit, 8 bit	7 bit, 8 bit, 9 bit (Note1)
Stop bit length	Transfer 1 bit, 2 bit Receive 1 bit	Transfer 1 bit, 2 bit Receive 1 bit
Parity bit	- None - Even - Odd	- No parity bit - Appending 0 parity - Appending even parity - Appending odd parity
Maximum bit rate	625k bps (Note2)	5.3M bps (Note3)
Transfer clock source	- On-chip baud rate generator - External clock	Transfer clock (f_{TCLK})
Count clock	φ, φ/4, φ/16, φ/64, SCK3	$f_{TCLK} = f_{CLK}$ to $f_{CLK}/2^{15}$
First bit of communication data	LSB first	- LSB first - MSB first
Break detection	Yes	None
Output a clock of the same frequency as the bit rate	Yes	None
SNOOZE mode	None	Yes
Noise canceller	Yes (Only for RXD_3)	Yes (RXDm pin)
Operation disabled	Write 0 to the TE bit, RE bit in the SCR3 register	Write 1 to the STmn bit in the STm register
Operation Enable	Write 1 to the TE bit, RE bit in the SCR3 register	Write 1 to the SSmn bit in the SSm register
Operating mode setting	Write 0 to the COM bit in the SMR register	Write 0 and 1 to the MDmn2 and MDmn1 bits in the SMRmn register, respectively.
Transmission operation start	Write transmit data to TDR register	Write transmit data to SDRmn register
Reception operation start	When the start bit has been detected	When the start bit has been detected
Reception error	- Overrun error - Parity error - Framing error	- Overrun error - Parity error - Framing error

Note1. UART0, UART2

Note2. ϕ = 20MHz

Note3. HS (high-speed main) mode, and f_{CLK} = 32MHz

Remark. For RL78/G14, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
q: UART number (q = 0 to 3)

Table 2.3 Differences between asynchronous mode (2/2)

Item	H8/36109 SCI3 Asynchronous mode	RL78/G14 Serial array unit (SAU) UART
Interrupt sources	- Transmit-end - Transmit-data-empty - Receive-data-full - Receive-error Overrun error, Framing error, Parity error	- Transfer end interrupt (Transmission) - Transfer end interrupt (Reception]) - Buffer empty interrupt - Error interrupt (Framing error, Parity error, Overrun error)
Interrupt occur timing	Transmission - SCR3 register When the TIE bit is 1 and data is transferred from TDR to TSR - SCR3 register When the TEIE bit is 1 and the stop bit is transmitted Reception - When the stop bit is detected - When the overrun error is detected - When the framing error is detected - When the parity error is detected	Single-transmission mode - After the last stop bit is transmitted. Continuous transmission mode - When the transmit data is transferred from the SDRmn register to the shift register Reception - When the stop bit is received (Including the case where a parity error or framing error occurs) - When an overrun error occurs
Receive data input pin	RXD pin	RxDq pin
Transmit data output pin	TXD pin	TxDq pin

Remark. For RL78/G14, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
q: UART number (q = 0 to 3)

2.2 Differences between clock synchronous mode

The clock synchronous mode of the SCI3 of the H8/36109 correspond to the 3-wire serial I/O (CSI) of the SAU of the RL78/G14. Table 2.4 and Table 2.5 shows the differences between clock synchronous mode.

Table 2.4 Differences between clock synchronous mode (1/2)

Item	H8/36109 SCI3 Clock synchronous mode	RL78/G14 Serial array unit (SAU) 3-wire serial I/O (CSI)
Data length	8bit	7bit, 8bit
Maximum bit rate	4MHz (Note)	- Master transmission/reception 16MHz (CSI00, CSI20 only) 8MHz (CSImn) - Slave transmission/reception 4MHz
Transfer clock source	- On-chip baud rate generator - External clock	Transfer clock (f_{TCLK})
Count clock	φ, φ/4, φ/16, φ/64, SCK3	$f_{TCLK} = f_{CLK}$ to $f_{CLK}/2^{15}$
First bit of communication data	LSB first	- LSB first - MSB first
SNOOZE mode	None	Yes
Operation disabled	Write 0 to the TE bit, RE bit in the SCR3 register	Write 1 to the STmn bit in the STm register
Operation Enable	Write 1 to the TE bit, RE bit in the SCR3 register	Write 1 to the SSmn bit in the SSm register
Operating mode setting	Write 1 to the COM bit in the SMR register	Write 0 and 0 to the MDmn2 and MDmn1 bits in the SMRmn register, respectively.
Transmission operation start	Write transmit data to TDR register	Write transmit data to SIOp register (When TXEmn = 1)
Reception operation start	- Supply synchronous clock - Write H'FF as dummy data to TDR register	- Write transmit data to SIOp register - Write FFH as dummy data to SDRmn register
Reception error	Overrun error	Overrun error
Interrupt sources	- Transmit-end - Transmit-data-empty - Receive-data-full - Receive-error (Overrun error)	- Transfer end interrupt (Transmission) - Transfer end interrupt (Reception]) - Buffer empty interrupt - Error interrupt (Overrun error)

Note. Continuous transfer is not possible

Remark. For RL78/G14, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31) mn = 00 to 03, 10 to 13

Table 2.5 Differences between clock synchronous mode (2/2)

Item	H8/36109 SCI3 Clock synchronous mode	RL78/G14 Serial array unit (SAU) 3-wire serial I/O (CSI)
Interrupt occur timing	Transmission - SCR3 register When the TIE bit is 1 and data is transferred from TDR to TSR Reception - When the stop bit is detected - When the overrun error is detected	Single-transmission mode - When data is transferred from the SDRmn register to the shift register. Reception - When the stop bit is received - When an overrun error occurs
Clock input/output	SCK3 pin	SCKmn pin
Receive data input pin	RXD pin	SImn pin
Transmit data output pin	TXD pin	SOmn pin

Remark. For RL78/G14, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31) mn = 00 to 03, 10 to 13

3. Comparison between Registers

Table 3.1 to Table 3.3 compares the registers for the H8/36109 SCI3 and the registers for the RL78/G14 SAU.

Table 3.1 Comparison between Registers (1/3)

Item	H8/36109 SCI3	RL78/G14 Serial array unit (SAU)
Control of SCI3 input clock supply	MSTCR1 register MSTS3 bit MSTCR2 register MSTS3_2 bit	None
Control of serial array unit input clock	None	PER0 register SAU1EN bit, SAU0EN bit
Serial mode control register	SMCR register	None
Noise Cancel Function Select	SMCR register NFEN_3 bit	NFEN0 register SNFEN30 bit, SNFEN20 bit SNFEN10 bit, SNFEN00 bit
TXD_3 Pin Select	SMCR register TXD_3 bit	None
SCI3_3 Module Standby	SMCR register MSTS3_3 bit	None
Receive Data Register	RDR register	Lower 8/9 bits (Note1) of SDRmn register (Note2)
Transmit Data Register	TDR register	Lower 8/9 bits (Note1) of SDRmn register (Note3)
Serial Mode Register	SMR register	SMRmn register
Communication Mode	SMR register COM bit	SMRmn register MDmn2, MDmn1 bit
Character Length (enabled only in asynchronous mode)	SMR register CHR bit	SCRmn register DLSmn1 (Note4), DLSmn0 bit
Parity Enable (enabled only in asynchronous mode)	SMR register PE bit	SCRmn register PTCmn1, PTCmn0 bit
Parity Mode (enabled only when the PE bit is 1 in asynchronous mode)	SMR register PM bit	
Stop Bit Length (enabled only in asynchronous mode)	SMR register STOP bit	SCRmn register SLCmn1 (Note5), SLCmn0 bit
Multiprocessor Mode	SMR register MP bit	None

Note1. Only following UARTs can be specified for the 9-bit data length.
80, 100-pin products: UART0 and UART2

Note2. mn = 00, 02, 10, 12 (Even channel is UART transmission function)

Note3. mn = 01, 03, 11, 13 (Odd channel is UART reception function)

Note4. The SCR00 and SCR01 registers and SCR10 and SCR11 registers for 80, 100-pin products only.
Others are fixed to 1.

Note5. The SCR00, SCR02, SCR10, and SCR12 registers only.

Remark. For RL78/G14, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

Table 3.2 Comparison between Registers (2/3)

Item	H8/36109 SCI3	RL78/G14 Serial array unit (SAU)
Clock Select	SMR register CKS1, CKS0 bit	SPSm register PRSmk3 - PRSmk0 bit SMRmn register CKSmn bit, CCSmn bit
Serial Control Register	SCR3 register	None
Transmit Interrupt Enable	SCR3 register TIE bit	SMRmn register MDmn0
Receive Interrupt Enable	SCR3 register RIE bit	
Transmit Enable	SCR3 register TE bit	SCRmn register TXEmn, RXEmn bit SSm register SSmn bit STm register STmn bit
Receive Enable	SCR3 register RE bit	
Multiprocessor Interrupt Enable	SCR3 register MPIE bit	None
Transmit End Interrupt Enable	SCR3 register TEIE bit	SMRmn register MDmn0
Clock Enable	SCR3 register CKE1, CKE0 bit	SPSm register PRSmk3 - PRSmk0 bit SMRmn register CKSmn bit, CCSmn bit
Serial Status Register	SSR register	SSRmn register
Transmit Data Register Empty	SSR register TDRE bit	SSRmn register BFFmn bit
Receive Data Register Full	SSR register RDRF bit	
Overrun Error	SSR register OER bit	SSRmn register OVFmn bit
Framing Error	SSR register FER bit	SSRmn register FEFmn (Note1) bit
Parity Error	SSR register PER bit	SSRmn register PEFmn bit
Transmit End	SSR register TEND bit	SSRmn register TSFmn bit
Multiprocessor Bit Receive	SSR register MPBR bit	None
Multiprocessor Bit Transfer	SSR register MPBT bit	None
Bit Rate Register	BRR register	Higher 7 bits of SDRmn register

Note1. The SIR01, SIR03, SIR11, and SIR13 registers only.

Remark. For RL78/G14, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), k = 0, 1

Table 3.3 Comparison between Registers (3/3)

Item	H8/36109 SCI3	RL78/G14 Serial array unit (SAU)
Selection of data and clock phase in CSI mode	None	SCRmn register DAPmn, CKPmn bit
Mask control of error interrupt signal	None	SCRmn register EOCmn bit
Selection of data transfer sequence	None	SCRmn register DIRmn bit
Serial flag clear trigger register	None	SIRmn register
Clear trigger of framing error	None	SIRmn register FECTmn bit (注)
Clear trigger of parity error flag	None	SIRmn register PECTmn bit
Clear trigger of overrun error flag	None	SIRmn register OVCTmn bit
Serial channel enable status register	None	SEm register
Indication of operation enable/stop status of channel n	None	SEm register SEmn bit
Serial output enable register	None	SOEm register
Serial output register	None	SOm register
Serial clock output of channel n	None	SOm register CKOmn bit
Serial data output of channel n	None	SOm register SOmn bit
Serial output level register	None	SOLm register
Selects inversion of the level of the transmit data of channel n in UART mode	None	SOLm register SOLmn bit
Selection of whether to enable or disable the generation of communication error interrupts in the SNOOZE mode	None	SSCm register SSECm bit
Setting of the SNOOZE mode	None	SSCm register SWCm bit
Input switch control register	None	ISC register

Note. The SIR01, SIR03, SIR11, and SIR13 registers only.

Remark. For RL78/G14, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

4. Sample Code for Serial Array Unit

The sample code for the serial array unit is explained in the following application notes.

- RL78/G13 Serial Array Unit for 3-Wire Serial I/O (Master Transmission/Reception) CC-RL (R01AN2547)
- RL78/G13 Serial Array Unit for 3-Wire Serial I/O (Slave Transmission/Reception) CC-RL (R01AN2711)
- RL78/G13 Low-power Consumption Operation (CSI in SNOOZE Mode) CC-RL (R01AN2762)
- RL78/G13 Serial Array Unit (UART Communication) CC-RL (R01AN2517)
- RL78/G13 DMA Controller (UART Sequential Reception) CC-RL (R01AN2835)
- RL78/G13 Self-Programming (Received Data via UART) CC-RL (R01AN2761)
- RL78/G13 Low-power Consumption Operation (UART in SNOOZE Mode) CC-RL (R01AN2713)

5. Documents for Reference

User's Manual:

- RL78/G14 User's Manual: Hardware (R01UH0186)
- H8/36109 Group User's Manual: Hardware (R01UH0294)

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News:

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Apr. 06, 2020	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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