RL78/G14, H8/36109

Migration Guide from H8 to RL78: Exception Handling

Introduction

This application note describes how to migrate the Exception handling of H8/36109 to the Reset function and the Interrupt function of RL78/G14 (100-pin package).

Target Device

RL78/G14, H8/36109

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Exception handling of H8/36109 and Interrupt function and Reset function of RL78/G14

Table 1.1 shows the functions of the Exception handling of H8/36109, Table 1.2 shows the functions of Reset function of RL78/G14, Table 1.3 shows the functions of Interrupt function of RL78/G14.

Table 1.1 Functions of Exception handling of H8/36109

Function	Explanation
Reset	A reset has the highest exception priority. Exception handling starts after the reset state is cleared by a negation of the $\overline{\text{RES}}$ signal. Exception handling is also started when the watchdog timer overflows. The exception handling executed at this time is the same as that for a reset by the $\overline{\text{RES}}$ pin.
Trap Instruction	Exception handling starts when a trap instruction (TRAPA) is executed. A vector address corresponding to a vector number from 0 to 3 which are specified in the instruction code is generated. Exception handling can be executed at all times in the program execution state, regardless of the setting of the I bit in CCR.
Interrupts	External interrupts other than the NMI and internal interrupts other than the address break are masked by the I bit in CCR, and kept pending while the I bit is set to 1. Exception handling starts when the current instruction or exception handling ends, if an interrupt is requested. The priority levels of interrupt sources other than the NMI and address break can be set for each module by the interrupt control register (ICR).

Table 1.2 Functions of Reset function of RL78/G14

Function	Explanation
External reset	External reset input via $\overline{\text{RESET}}$ pin
Internal reset	- Internal reset by watchdog timer program loop detection - Internal reset by comparison of supply voltage and detection voltage of power-on-reset (POR) circuit - Internal reset by comparison of supply voltage of the voltage detector (LVD) and detection voltage - Internal reset by execution of illegal instruction (Note) - Internal reset by RAM parity error - Internal reset by illegal-memory access

Note. The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

Table 1.3 Functions of Interrupt function of RL78/G14

Function	Explanation
Maskable interrupts	These interrupts undergo mask control. Maskable interrupts can be divided into four priority groups by setting the priority specification flag registers. Multiple interrupt servicing can be applied to low-priority interrupts when high-priority interrupts are generated. If two or more interrupt requests, each having the same priority, are simultaneously generated, then they are processed according to the default priority of vectored interrupt servicing. A standby release signal is generated and STOP, HALT, and SNOOZE modes are released. External interrupt requests and internal interrupt requests are provided as maskable interrupts.
Software interrupt	This is a vectored interrupt generated by executing the BRK instruction. It is acknowledged even when interrupts are disabled. The software interrupt does not undergo interrupt priority control.

Table 1.4 shows the Exception handling corresponding to the Reset function and the Interrupt function.

Table 1.4 Correspondence between Functions

H8/36109	RL78/G14
Reset	External reset, Internal reset
Trap Instruction	None
Interrupts (Include NMI interrupt request)	Maskable interrupts

2. Differences between Reset

Table 2.1 summarizes the differences between the reset functions of H8/36109 and RL78/G14.

Table 2.1 Summary of Differences between Functions

Item	H8/36109	RL78/G14
Reset sources	Reset by the $\overline{\text{RES}}$ pin	External reset input via $\overline{\text{RESET}}$ pin
	Reset by the Watchdog timer	- Internal reset by watchdog timer program loop detection - Internal reset by comparison of supply voltage and detection voltage of power-on-reset (POR) circuit - Internal reset by comparison of supply voltage of the voltage detector (LVD) and detection voltage - Internal reset by execution of illegal instruction (Note) - Internal reset by RAM parity error - Internal reset by illegal-memory access

Note. The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

3. Differences between Interrupt

3.1 Differences in Function Overview

Table 3.1 shows the differences between the Interrupt.

Table 3.1 Difference between Interrupt

Item	H8/36109 Interrupt	RL78/G14 Interrupt
Interrupt request	- External interrupt - Internal interrupt	- External interrupt - Internal interrupt
External interrupt request	- IRQ3 to IRQ0 interrupt - WKP interrupt	- Pin input edge detection - Key return signal detection
	Non-maskable interrupt	None
Priority level	2 level	4 level
Interrupt Response Time	19 to 41 States	9 clocks to 16 clocks (1 clock = 1/f_{CLK})
Interrupt request flag	IRRXX bit IWPXX bit	XXIFX bit
Interrupt Enable	IENXX bit	XXMKX bit
Interrupt Priority Level	ICRXX bit	XXPR1X, XXPR0X bit

3.2 Register Compatibilities

Table 3.2 compares the registers for the Interrupt functions of the H8/36109 and the RL78/G14.

Table 3.2 Comparison between Registers

Item	H8/36109	RL78/G14
Interrupt edge select register	IEGR1 register, IEGR2 register	EGP0 register, EGP1 register EGN0 register, EGN1 register
Interrupt enable register	IENR1 register, IENR2 register	MK0L register, MK0H register MK1L register, MK1H register MK2L register, MK2H register
Interrupt flag register	IRR1 register, IRR2 register	IF0L register, IF0H register IF1L register, IF1H register IF2L register, IF2H register
Wakeup interrupt flag register	IWPR register	None
Interrupt control registers	ICRA register ICRB register ICRC register ICRD register	PR00L register, PR00H register PR01L register, PR01H register PR02L register, PR02H register PR10L register, PR10H register PR11L register, PR11H register PR12L register, PR12H register

3.3 Comparison between Interrupt Priorities

Table 3.3 to Table 3.7 compare the interrupt priorities of H8/36109 and RL78/G14 (100-pin products).

Table 3.3 Comparison between Interrupt Priorities (1/5)

H8/36109				RL78/G14			
Vector Number	Related Module	Exception Sources	Vector Address (Note)	Default Priority	Name	Trigger	Vector Table Address
-	-	-	-	-	Reset	Reset Source	00000H
0	$\overline{\text{RES}}$ pin Watchdog timer	Reset	H'000000	0	INTWDTI	Watchdog timer interval	00004H
1	-	Reserved for system use	H'000004	1	INTLVI	Voltage detection	00006H
2				2	INTP0	Pin input edge detection	00008H
3				3	INTP1		0000AH
4				4	INTP2		0000CH
5				5	INTP3		0000EH
6				6	INTP4		00010H
7	External interrupt pin	NMI	H'00001C	7	INTP5		00012H
8	CPU	Trap instruction #0	H'000020	8	INTST2/ INTCSI20/ INTIIC20	UART2 transmission transfer end or buffer empty interrupt/CSI20 transfer end or buffer empty interrupt/IIC20 transfer end	00014H
9	CPU	Trap instruction #1	H'000024	9	INTSR2 INTCSI21/ INTIIC21	UART2 reception transfer end/CSI21 transfer end or buffer empty interrupt/IIC21 transfer end	00016H
10	CPU	Trap instruction #2	H'000028	10	INTSRE2	UART2 reception communication error occurrence	00018H
					INTTM11H	End of timer channel 11 count or capture (at higher 8-bit timer operation)	
11	CPU	Trap instruction #3	H'00002C	11	INTST0/ INTCSI00/ INTIIC00	UART0 transmission transfer end or buffer empty interrupt/CSI00 transfer end or buffer empty interrupt/IIC00 transfer end	0001EH

Note. Only the first address is listed.

Table 3.4 Comparison between Interrupt Priorities (2/5)

H8/36109				RL78/G14			
Vector Number	Related Module	Exception Sources	Vector Address (Note)	Default Priority	Name	Trigger	Vector Table Address
12	Address break	Break conditions satisfied	H'000030	12	INTSR0/ INTCSI01/ INTIIC01	UART0 reception transfer end/CSI01 transfer end or buffer empty interrupt/IIC01 transfer end	00020H
13	CPU	Direct transition by executing the SLEEP instruction	H'000034	13	INTSRE0	UART0 reception communication error occurrence	00022H
					INTTM01H	End of timer channel 01 count or capture (at higher 8-bit timer operation)	
14	External interrupt pin	IRQ0 Low-voltage detection interrupt	H'000038	14	INTST1/ INTCSI10/ INTIIC10	UART1 transmission transfer end or buffer empty interrupt/CSI10 transfer end or buffer empty interrupt/IIC10 transfer end	00024H
15		IRQ1	H'00003C	15	INTSR1/ INTCSI11/ INTIIC11	UART1 reception transfer end/CSI11 transfer end or buffer empty interrupt/IIC11 transfer end	00026H
16		IRQ2	H'000040	16	INTSRE1	UART1 reception communication error occurrence	00028H
					INTTM03H	End of timer channel 03 count or capture (at higher 8-bit timer operation)	
17		IRQ3	H'000044	17	INTIICA0	End of IICA0 communication	0002AH
18		WKP	H'000048	18	INTTM00	End of timer channel 00 count or capture	0002CH
19	RTC	Overflow	H'00004C	19	INTTM01	End of timer channel 01 count or capture	0002EH
20	-	Reserved for system use	H'000050	20	INTTM02	End of timer channel 02 count or capture	00030H
21				21	INTTM03	End of timer channel 03 count or capture	00032H

Note. Only the first address is listed.

Table 3.5 Comparison between Interrupt Priorities (3/5)

H8/36109				RL78/G14			
Vector Number	Related Module	Exception Sources	Vector Address (Note)	Default Priority	Name	Trigger	Vector Table Address
22	Timer V	Compare match A Compare match B Overflow	H'000058	22	INTAD	End of A/D conversion	00034H
23	SCI3	Receive data full Transmit data empty Transmit end Receive error	H'00005C	23	INTRTC	Fixed-cycle signal of real-time clock/alarm match detection	00036H
24	IIC2	Transmit data empty Transmit end Receive data full Arbitration lost/overrun error NACK detection Stop condition detected	H'000060	24	INTIT	Interval signal detection	00038H
25	-	Reserved for system use	H'000064	25	INTKR	Key return signal detection	0003AH
26				26	INTST3/ INTCSI30/ INTIIC30	UART3 transmission transfer end or buffer empty interrupt/CSI30 transfer end or buffer empty interrupt/IIC30 transfer end	0003CH
27				27	INTSR3/ INTCSI31/ INTIIC31	UART3 reception transfer end/CSI31 transfer end or buffer empty interrupt/IIC31 transfer end	0003EH
28				28	INTTRJ0	Timer RJ interrupt	00040H
29	Timer B1	Overflow	H'000074	29	INTTM10	End of timer channel 10 count or capture	00042H
30	-	Reserved for system use	H'000078	30	INTTM11	End of timer channel 11 count or capture	00044H
31				31	INTTM12	End of timer channel 12 count or capture	00046H
32	SCI3_2	Receive data full Transmit data empty Transmit end Receive error	H'000080	32	INTTM13	End of timer channel 13 count or capture	00048H

Note. Only the first address is listed.

Table 3.6 Comparison between Interrupt Priorities (4/5)

H8/36109				RL78/G14			
Vector Number	Related Module	Exception Sources	Vector Address (Note)	Default Priority	Name	Trigger	Vector Table Address
33	-	Reserved for system use	H'000084	33	INTP6	Pin input edge detection	0004AH
34	SCI3_3	Receive data full Transmit data empty Transmit end Receive error	H'000088	34	INTP7		0004CH
35	Timer RC	Input capture A / compare match A Input capture B / compare match B Input capture C / compare match C Input capture D / compare match D Overflow	H'00008C	35	INTP8		0004EH
36	A/D converter	A/D conversion end	H'000090	36	INTP9		00050H
37	Timer RD_0	Compare match / input capture A0 to D0 Overflow	H'000094	37	INTP10	Pin input edge detection	00052H
					INTCMP0	Comparator detection 0	
38	Timer RD_1	Compare match / input capture A1 to D1 Overflow	H'000098	38	INTP11	Pin input edge detection	00054H
					INTCMP1	Comparator detection 1	
39	Timer RD_2	Compare match / input capture A2 to D2 Overflow	H'00009C	39	INTTRD0	Timer RD0 input capture, compare match, overflow, underflow interrupt	00056H
40	Timer RD_3	Compare match / input capture A3 to D3 Overflow	H'0000A0	40	INTTRD1	Timer RD1 input capture, compare match, overflow, underflow interrupt	00058H
41	Clock switching	When the system clock sources are switched from the external-input signal to the internal-generated signal	H'0000A4	41	INTTRG	Timer RG input capture, compare match, overflow, underflow interrupt	0005AH

Note. Only the first address is listed.

Table 3.7 Comparison between Interrupt Priorities (5/5)

H8/36109				RL78/G14			
Vector Number	Related Module	Exception Sources	Vector Address (Note)	Default Priority	Name	Trigger	Vector Table Address
-	-	-	-	42	INTSRE3	UART3 reception communication error occurrence	0005CH
					INTTM13H	End of timer channel 13 count or capture (at 8-bit timer operation)	
-	-	-	-	43	INTIICA1	End of IICA1 communication	00060H
-	-	-	-	44	INTFL	Reserved (Note2)	00062H

Note1. Only the first address is listed.
Note2. Be used at the flash self-programming library or the data flash library.

4. Sample Code for Interrupt Function

The sample code for the interrupt functions is explained in the following application notes.

- RL78/G13 Key Interrupt Function CC-RL (R01AN2700)

5. Documents for Reference

User's Manual:

- RL78/G14 User's Manual: Hardware (R01UH0186)
- RL78 family User's Manual: Software (R01US0015)
- H8/36109 Group User's Manual: Hardware (R01UH0294)
- H8/300H Series Software Manual (REJ09B0213)

The latest versions can be downloaded from the Renesas Electronics website.

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Revision History

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		Page	Summary
1.00	Jul.10, 2020.	-	First edition issued

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2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
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