RL78/G13, 78K0/Kx2

Migration Guide from 78K0 to RL78: Watchdog Timer

Introduction

This application note describes how to migrate the Watchdog Timer of the 78K0/Kx2 to that of the RL78/G13.

Target Device

RL78/G13, 78K0/Kx2

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Differences in Function Overview

Table 1.1 summarizes the differences between the watchdog timer of the 78K0/Kx2 and the watchdog timer of the RL78/G13.

Table 1.1 Differences

Item	78K0/Kx2	RL78/G13
Configuration	17-bit counter	17-bit counter
Count clock (Note)	$f_{RL}/2$	f_{IL}
Count Mode	Count up	Count up
Counter operation enabled	Setting bit 4 (WDTON) of the option byte (0080H) to 1	Setting bit 4 (WDTON) of the option byte (000C0H) to 1
Watchdog timer counter overflow time	$2^{10}/f_{RL}$, $2^{11}/f_{RL}$, $2^{12}/f_{R}$, $2^{13}/f_{RL}$, $2^{14}/f_{RL}$, $2^{15}/f_{RL}$, $2^{16}/f_{RL}$, $2^{17}/f_{RL}$	$2^{6}/f_{IL}$, $2^{7}/f_{IL}$, $2^{8}/f_{IL}$, $2^{9}/f_{IL}$, $2^{11}/f_{IL}$, $2^{13}/f_{IL}$, $2^{14}/f_{IL}$, $2^{16}/f_{IL}$
Interval time interrupt	None	Yes (When 75% + 1/2 f_{IL} of the overflow time is reached, an interval interrupt can be generated.)
Window Open Period of Watchdog Timer	Select from 25%, 50%, 75%, 100%	Select from 50%, 75%, 100%

Note. 78K0/Kx2: f_{RL} = TYP. 240kHz
(2.7 V≦VDD≦5.5 V: 216kHz to 264 kHz, 1.8 V≦VDD＜2.7 V:192kHz to 264kHz)

RL78/G13: f_{IL} = TYP. 15kHz (15kHz±15%)

The watchdog timer of the 78K0/Kx2 operates with the internal low-speed oscillation clock ($f_{RL}/2$) to detect an inadvertent program loop. It generates an internal reset signal upon detecting an inadvertent program loop. A window open period can be specified in the watchdog timer. During the window open period, writing "ACH" to the WDTE register causes the watchdog timer to clear the counter and restart counting. During the window close period, writing "ACH" to the WDTE register is detected as an abnormality and an internal reset is generated.

The watchdog timer in the RL78/G13 operates with the low-speed on-chip oscillator clock (f_{IL}) to detect an inadvertent program loop. It generates an internal reset signal upon detecting an inadvertent program loop. A window open period can be specified in the watchdog timer. During the window open period, writing "ACH" to the WDTE register causes the watchdog timer to clear the counter and restart counting. During the window close period, writing "ACH" to the WDTE register is detected as an abnormality. In addition, an interval interrupt can be generated when 75% of the overflow time + 1/2 f_{IL} is reached.

Figure 1.1 shows the case where the window open period for the watchdog timer is set to 75% of the overflow time.

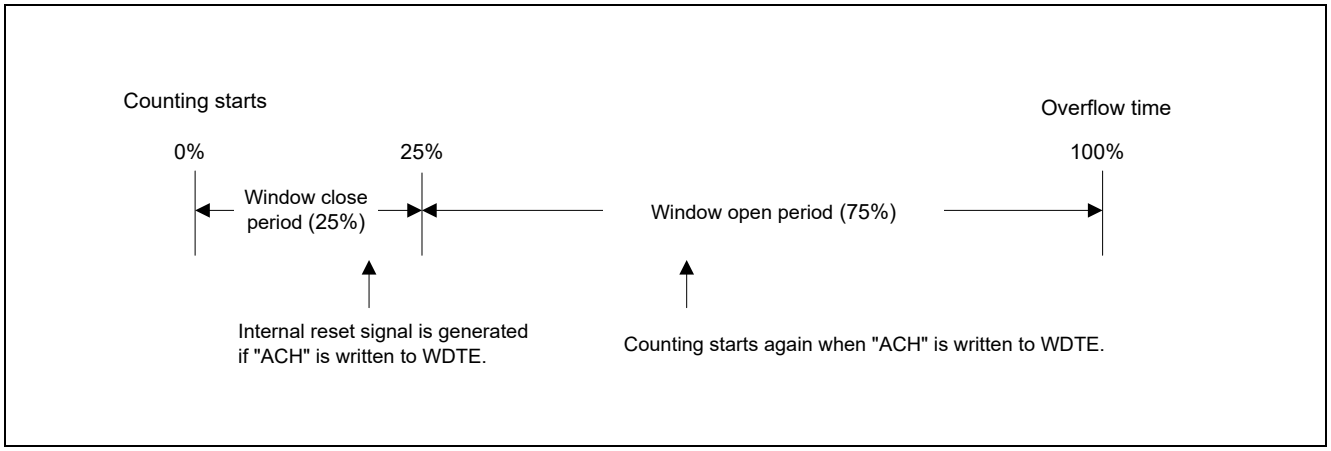

Figure 1.1 If the window open period of watchdog timer is 75%

2. Differences between Watchdog Timer

The watchdog timer of the 78K0/Kx2 corresponds to the watchdog timer of the RL78/G13.

Table 2.1 and Table 2.2 show the differences between the watchdog timer.

Table 2.1 Differences between Watchdog Timer (1/2)

Item	78K0/Kx2	RL78/G13
Count clock	$f_{RL}/2$	f_{IL}
Overflow Time setting	Setting the WDCS2, WDCS1, WDCS0 in option byte (Address:0080H) Overflow Time (Min.) $2^{10}/f_{RL}$ (3.878 ms) $2^{11}/f_{RL}$ (7.757 ms) $2^{12}/f_{RL}$ (15.51 ms) $2^{13}/f_{RL}$ (31.03 ms) $2^{14}/f_{RL}$ (62.06 ms) $2^{15}/f_{RL}$ (124.1 ms) $2^{16}/f_{RL}$ (248.2 ms) $2^{17}/f_{RL}$ (496.4 ms)	Setting the WDCS2, WDCS1, WDCS0 in option byte (Address: 000C0H) Overflow Time (Min.) $2^{6}/f_{IL}$ (3.710 ms) $2^{7}/f_{IL}$ (7.420 ms) $2^{8}/f_{IL}$ (14.84 ms) $2^{9}/f_{IL}$ (29.68 ms) $2^{11}/f_{IL}$ (118.7 ms) $2^{13}/f_{IL}$ (474.8 ms) $2^{14}/f_{IL}$ (949.7 ms) $2^{16}/f_{IL}$ (3799 ms)
Window open period of watchdog timer	Selecting 25%, 50%, 75%, or 100% by bits 6 and 5 (WINDOW1 and WINDOW0) of the option byte (address: 0080H).	Selecting 50%, 75%, or 100% by bits 6 and 5 (WINDOW1 and WINDOW0) of the option byte (address: 00C00H). (Note)
Counter operation enabled	Setting bit 4 (WDTON) of the option byte (0080H) to 1	Setting bit 4 (WDTON) of the option byte (000C0H) to 1
Counter operation disabled	Setting bit 4 (WDTON) of the option byte (0080H) to 0	Setting bit 4 (WDTON) of the option byte (000C0H) to 0
Counter operation stopped	Setting bit 0 (LSROSC) of the option byte (address: 0080H) to "0" and the LSRSTOP bit of the RCM register to "1". In the HALT or STOP mode, operation can be stopped by setting LSROSC = 0.	Setting bit 0 (WDSTBYON) of the option byte (address: 000C0H) to "0". (This is only effective in the HALT, STOP, or SNOOZE mode.)

Note. The window open period is 100% when WDSTBYON = 0, regardless the value of the WINDOW1 and WINDOW0 bits.

Remark. Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

Table 2.2 Differences between Watchdog Timer (2/2)

Item	78K0/Kx2	RL78/G13
Counter clearing source	- Writing "ACH" to the WDTE register during the window open period - Reset release	- Writing "ACH" to the WDTE register during the window open period - Reset release
Internal reset generation source	- If the watchdog timer counter overflows - If a 1-bit manipulation instruction is executed on the watchdog timer enable register (WDTE) - If data other than “ACH” is written to WDTE - If data is written to WDTE during a window close period - If the instruction is fetched from an area not set by the IMS and IXS registers (detection of an invalid check while the CPU hangs up) - If the CPU accesses an area that is not set by the IMS and IXS registers (excluding FB00H to FFCFH and FFE0H to FFFFH) by executing a read/write instruction (detection of an abnormal access during a CPU program loop)	- If the watchdog timer counter overflows - If a 1-bit manipulation instruction is executed on the watchdog timer enable register (WDTE) - If data other than “ACH” is written to the WDTE register - If data is written to the WDTE register during a window close period

Remark. Different products are provided with different functions. For details, refer to the appropriate user’s manuals (hardware).

3. Documents for Reference

User's Manual:

- RL78/G13 User's Manual: Hardware (R01UH0146)
- 78K0/Kx2 User's Manual: Hardware (R01UH0008)

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News:

The latest information can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Data	Description	
		Page	Summary
1.00	Jun.04, 2019	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

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1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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