RL78/G11

LED Control by Using 16-Bit Timer KB0 CC-RL

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Abstract

This application note describes how to control LED lights by using the timer KB0 of the RL78/G11.

The application covered in this application note provides ON/OFF control through sensor detection, light control through volume input, and constant current control.

Target Device

RL78/G11

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

Figure 1.1 shows a block diagram of the LED control system. With this system, the human sensor output is detected by the internal comparator. Once detected, the volume input is measured periodically. The volume input voltage is measured by the A/D converter. According to the volume input voltage, the current to be passed to the LED module (target current) is determined. The LED current is controlled through the PWM output of the 16-bit timer KB0 (hereinafter referred to as timer KB0). The LED current is measured by the programmable gain amplifier (hereinafter referred to as PGA) and A/D converter. By comparing the target current to the LED current, the PWM output of the timer KB0 is controlled (feedback processing).

The application covered in this application note controls the PWM output in the simplified manner. In the actual application, PI control or other appropriate control is necessary according to the circuit and the specifications. For PI control, refer to LED Control Using RL78/I1A (R01AN1087EJ).

If an over-current is detected when LED current is measured, the PWM output is stopped by using the forced output stop function of the timer KB0, and the high-level signal is output (alarm processing) from the P51 pin by using the comparator detection interrupt.

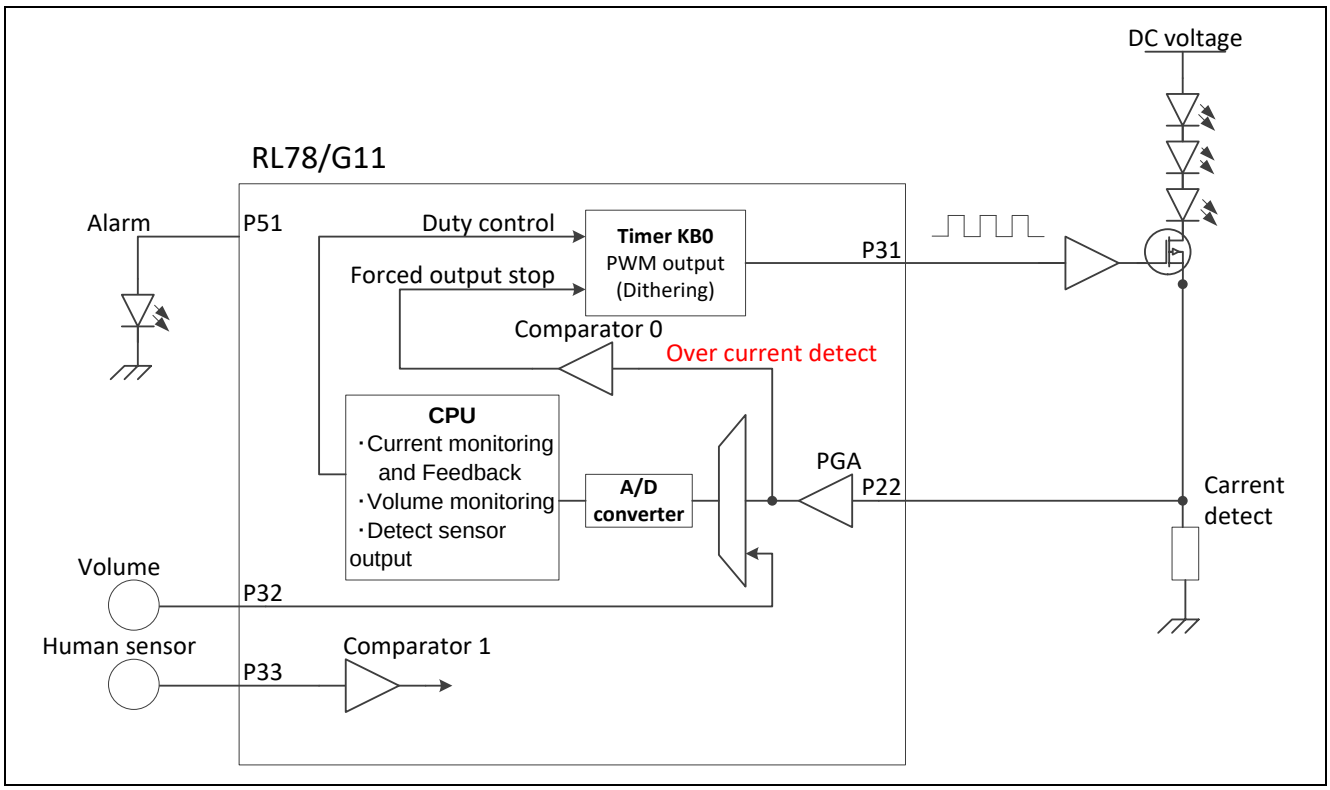

Figure 1.1 System Block Diagram

Table 1.1 shows the peripheral functions used and their applications

Table 1.1 Peripheral Functions and Their Applications

Peripheral Functions	Applications
P51	Alarm output (High level output at overcurrent detection)
16-bit Timer KB0	Current control of LED module due to PWM output, forced stop
D/A Converter	Reference voltage output for overcurrent detection
Programmable Gain Amplifier(PGA)	LED current measurement
Comparator 0	Over current detection
Comparator 1	Human sensor detection
Timer Array Unit	Generation of LED current measurement interval
A/D Converter	Measure output voltage of current detection circuit Volume output voltage measurement

1.1 Detection of Human Sensor Output by Comparator 1

This application assumes the human sensor with digital output. The human sensor output is assumed to be such that its high level can be recognized by the RL78/G11 when the RL78/G11 detects the detection target.

The internal reference voltage (1.45 V) is selected as the reference voltage of the comparator. After power on, when the comparator detection 1 interrupt (INTCMP1) occurs, the 12-bit interval timer starts counting and the timer KB0 starts PWM output.

According to the count clock of the 12-bit interval timer (f_{IL} = TYP. 15 kHz) and the compare value of the 12-bit interval timer (ITCMP11-ITCMP0 = FFFH), the INTIT period is approximately 273 ms (1/15 [kHz] x (4095 + 1)), and thus LED is lit for approximately five minutes by counting INTIT 1099 times. However, if INTCMP1 occurs within the five minutes, the INTIT count is once initialized and counting is continued to extend lighting for approximately five minutes.

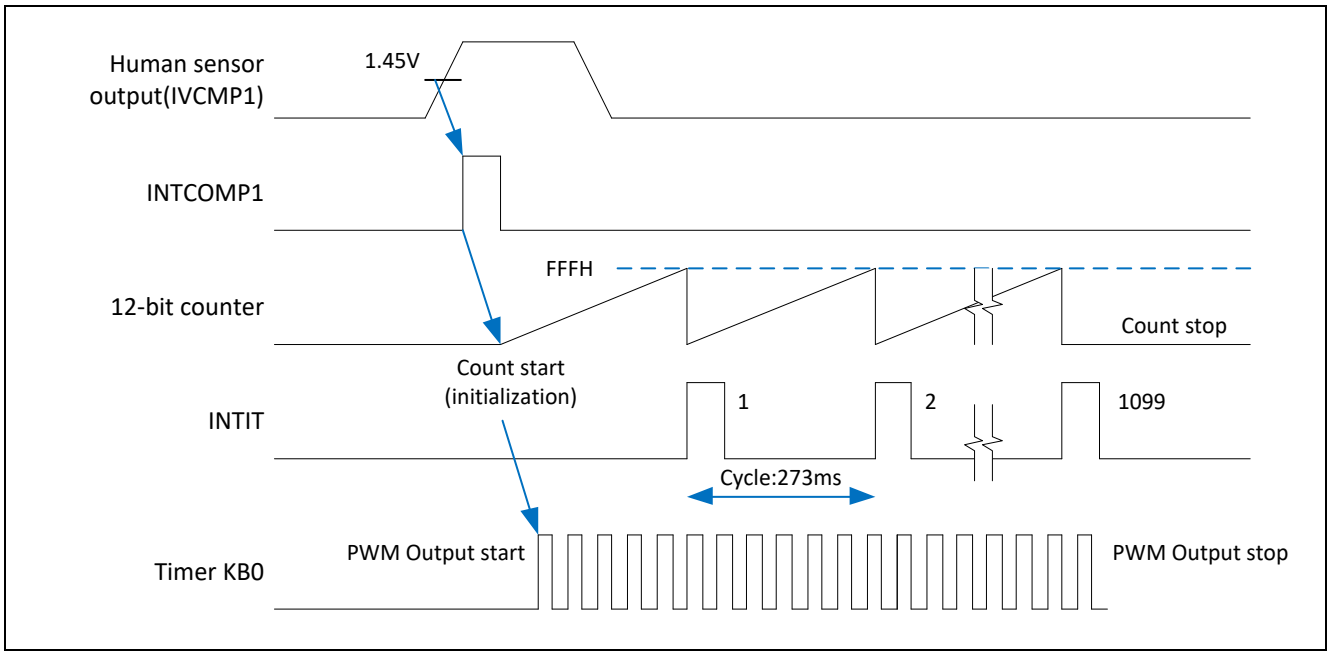

Figure 1.2 Detection of Human Sensor Output

1.2 Basic Settings of Timer KB0

The PWM output from the timer KB0 is used to control the LED current. The count clock of the timer KB is set to 48 MHz; the default and active levels of the PWM output are set to the low and high levels, respectively; and the PWM frequency is set to 250 kHz. In the initial setting, the duty ratio is set to 0% and then the PWM duty ratio is adjusted according to the current to be passed to the LED module.

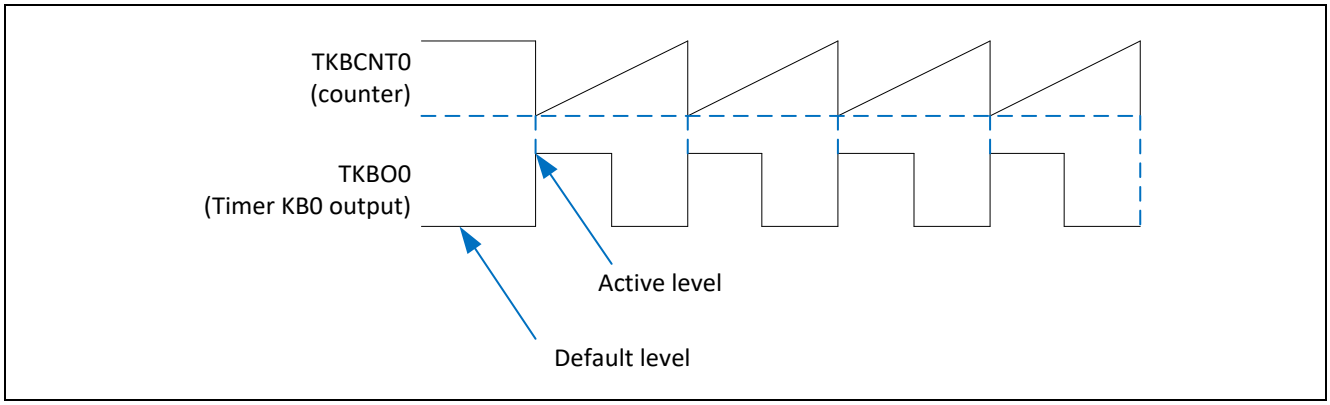

Figure 1.3 Basic operation of timer KB0

1.3 Feedback to Timer KB0

The application covered in this application note performs the feedback processing in the simplified manner.

The voltage applied to the volume input pin determines the target current. When the voltage applied to the volume input pin is 5 V, the target current is approximately 350 mA.

The LED current is measured by the PGA. The current is A/D-converted with the PGA amplification factor set to 8.

The interval timer period is set to 300 us, and the LED current is measured every 300 us. According to the measured LED current, the active level width of the PWM output of the timer KB0 is changed.

- When target current > LED current, and previous LED current ≥ LED current:
  Active level width = previous active level width + 1 (compare register value)

- When target current < LED current, and previous LED current ≤ LED current:
  Active level width = previous active level width – 1 (compare register value)

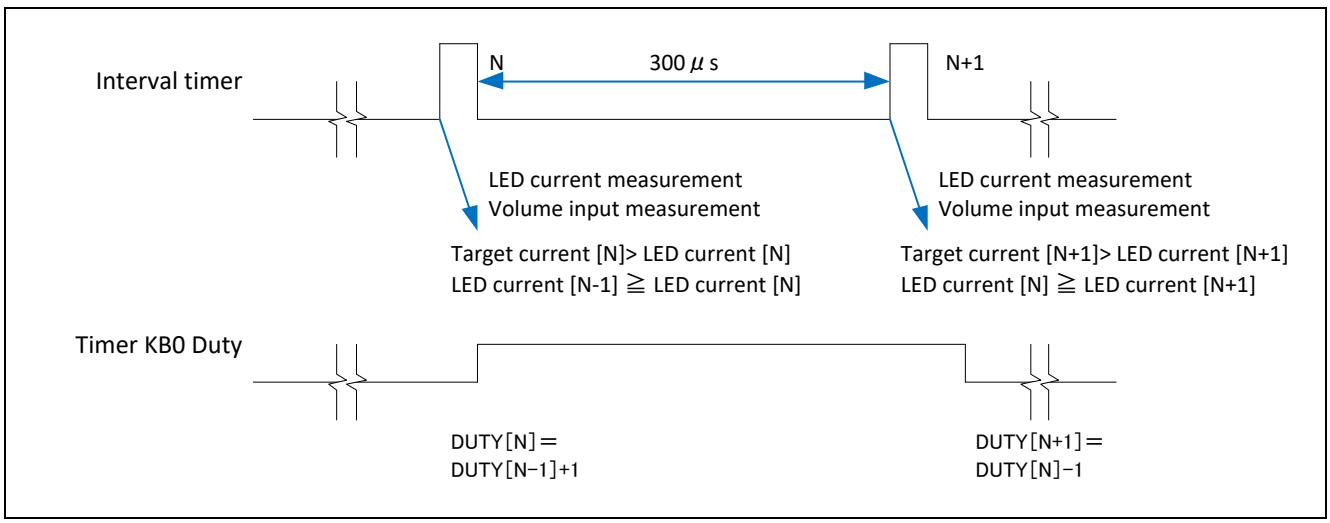

Figure 1.4 Feedback to timer KB0

1.4 Forced Output Stop of Timer KB0 by Using Comparator 0

Forced output stop function 1 of the timer KB0 is used. The IVCMP0 pin is used to measure the over-current of the system. IVCMP0 is compared to the channel 0 output of the internal D/A converter. At the rising edge of the CMP0 output, the timer KB0 is fixed to the low level. The LED current above 400 mA is determined as over-current.

Note that the forced output stop function can be cancelled by so setting the software bit TKBPAHTSnp. However, in this application, the forced output stop function is not cancelled.

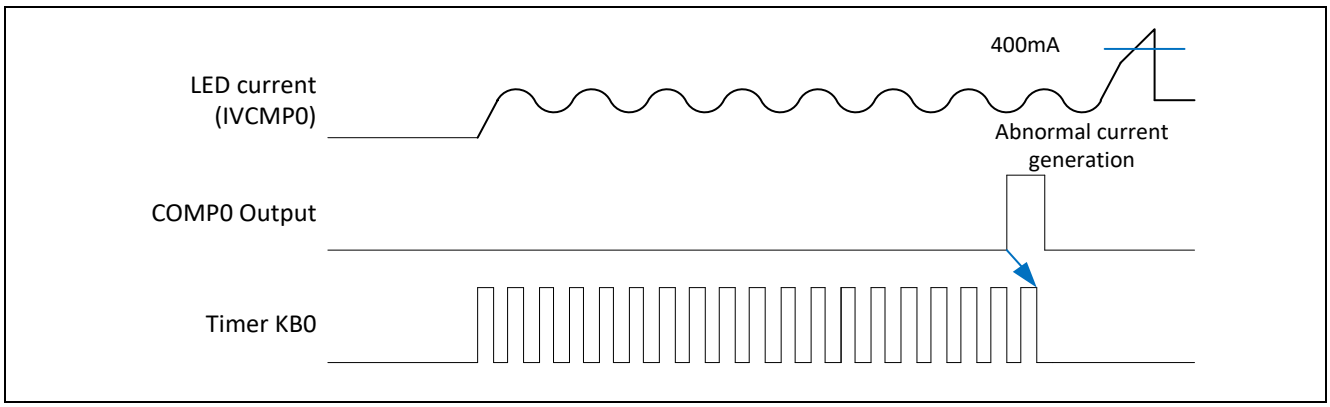

Figure 1.5 Forced Output Stop of Timer KB0

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	RL78/G11（R5F1058A）
Operating frequencies	● High-speed on-chip oscillator clock (f_{HOCO}): 24MHz (typ.) ● CPU/peripheral hardware clock (f_{CLK}): 24MHz/48MHz
Operating voltage	5.0V (operation possible from 2.7V to 5.5V) LVD operation (V_{LVD}) in reset mode is 2.81V at the rising edge or 2.75V at the falling edge.
Integrated development environment(CS+)	CS+ for CC V6.01.00 from Renesas Electronics Corp.
C compiler(CS+)	CC-RL V1.06.00 from Renesas Electronics Corp.
Integrated development environment(e2studio)	e2studio V5.4.0.018 from Renesas Electronics Corp.
C compiler(e2studio)	CC-RL V1.06.00 from Renesas Electronics Corp.
RL78/G11 code library	RL78/L13 code library V1.02.01.01 from Renesas Electronics Corp.

3. Related Application Notes

The application note related to this application note is listed below for reference.

LED Control Using RL78/I1A (R01AN1087EJ)

4. Hardware Descriptions

4.1 Hardware Configuration Example

Figure 4.1 shows an example of the hardware configuration described in this application note.

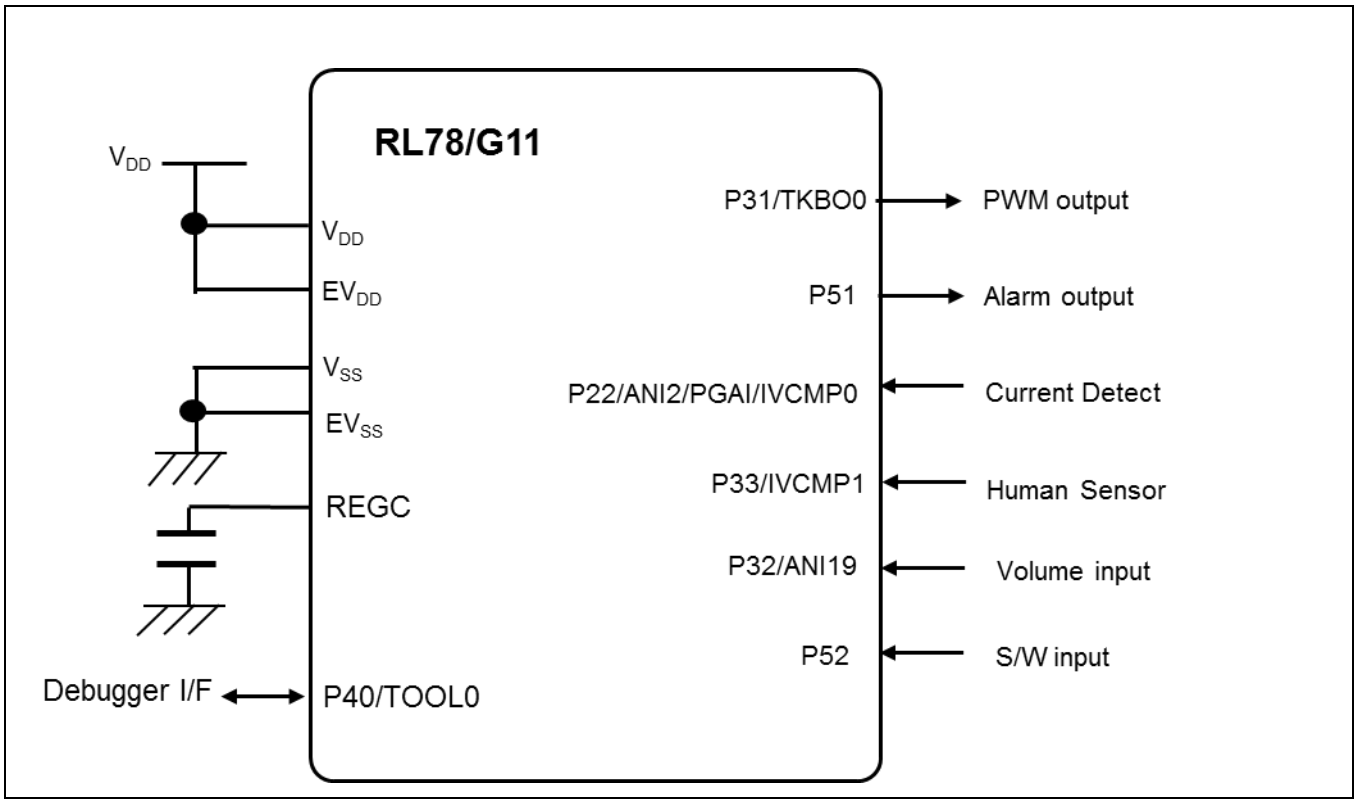

Figure 4.1 Hardware Configuration

Caution: The above figure is simplified to show an overview of the hardware connection. When designing application circuits, make sure to handle unused pins appropriately to satisfy the electrical characteristics (connect input-only ports independently to either V_{DD} or V_{SS} via resistors).

4.2 List of Pins Used

Table 4.1 lists the pins used and their functions.

Table 4.1 Pins Used and Their Functions

Pin Name	I/O	Function
P31/TKBO0	Output	LED control PWM output
P51	Output	Alarm Output
P22/ANI2/PGAI	Analog Input	Current detection
P33/ANI18/IVCMP1	Analog Input	Human sensor detection
P32/ANI19	Analog Input	Volume input level measurement

5. Software Description

5.1 Operation Overview

This section describes the sample code attached to this application note.

This sample code makes the following initial settings.

- Ports
- Clocks
- Timer KB0
- D/A converter
- PGA
- Comparators 0 and 1
- Timer array unit
- 12-bit interval timer
- A/D converter

After completion of the initial settings, the system is shifted to HALT mode. LED lighting control and over-current detection are performed.

The sample code is described in detail below.

1. Makes the initial settings for the port.
   - Sets P51 for output.

2. Makes the initial settings for the clocks.
   - Sets the operation mode to high speed main mode with 2.7 V ≤ VDD ≤ 5.5 V.
   - Sets the high-speed on-chip oscillator clock (fIH) to the main system clock (fMAIN).
   - Selects 48 MHz for the high-speed on-chip oscillator clock (fHOCO).
   - Sets the low-speed on-chip oscillator clock (fIL) to the subsystem clock (fSUB).
   - Selects fIL = 15 kHz for the interval timer operation clock.
   - Selects fIH = 24 MHz for the CPU and peripheral clock (fCLK).

3. Makes the initial settings for the timer KB0.
   - Sets TMKB0 to standalone mode.
   - Selects the high level and the low level as the active level and the default level of timer output TKBO0, respectively.
   - Sets the period and duty ratio of PWM to 4 us and 0%, respectively. Adjusts the PWM duty ratio according to the LED current.
   - Sets trigger output TKBTGCR0 to 3 us.
   - Sets forced output stop function 1 for TKBO0, and selects fixed low-level output. Selects comparator 0 as the trigger for function 1. Selects type 1 as the operation mode.

4. Makes the initial settings for the D/A converter.
   - Sets 163 as the conversion value for the D/A converter 0.

   Assuming that the LED over-current is 400 mA; PGA amplification factor is 8; and current detection resistance is 1 Ω, the reference voltage of the over-current detection is expressed as below.

   400 mA × 8 × 1 Ω = 3.2 V

   Since the reference voltage of the over-current detection is generated using the analog output from the D/A converter,

   Analog output voltage VANOi = VDD × (DACSi)/256

   Since VANOi = 3.2 V and VDD = 5 V, DACSi = 163.

5. Makes the initial settings for the PGA.
   - Selects PGAGND as the GND for the PGA.
   - Sets the PGA amplification factor to 8.

6. Makes the initial settings for the comparators.
   - Selects comparator high-speed mode as the comparator speed.

   <Comparator 0 (over-current detection)>
   - Selects standard mode.
   - Selects the reference voltage specified with COMPISEL.C0REFSEL as the reference voltage of comparator 0.
   - Selects the PGA output as the input signal to the comparator 0 + pin.
   - Selects the output from the internal D/A converter channel 0 as the input signal to the comparator 0 – pin.
   - Selects the interrupt request generated by comparator 0 one-edge detection.
   - Selects the interrupt request generated at comparator 0 rising edge.
   - Selects the mode in which comparator 0 filter is enabled with sampling at f_{CLK}. ($f_{CLK} = f_{IH}$ = 24 MHz)
   - Enables the comparator 0 interrupt and sets priority level to 3.

   <Comparator 1 (human sensor detection)>
   - Selects standard mode.
   - Selects BGRVREF as the reference voltage of comparator 1.
   - Selects the interrupt request generated by comparator 1 one-edge detection.
   - Selects the interrupt request generated at comparator 1 rising edge.
   - Selects the mode in which comparator 1 filter is enabled with sampling at f_{CLK}. ($f_{CLK} = f_{IH}$ = 24 MHz)
   - Enables the comparator 1 interrupt and sets priority level to 3.

7. Makes the initial settings for the timer array unit.
   - Sets channel 0 as the interval timer.
   - Sets the interval time to 300 us.
   - Enables the count end interrupt of timer channel 0 and sets priority level to 3.

8. Makes the initial settings for the 12-bit interval timer.
   - Selects f_{IL} as the operation clock for the interval timer.
   - Sets the interval time to TYP. 273 ms.
   - Enables the interval signal of 12-bit interval timer detection and sets priority level to 3.

9. Makes the initial settings for the A/D converter.
   - Stops the comparators.
   - Selects 10-bit resolution.
   - Selects VDD for VREF(+) and VSS for VREF(–).
   - Sets software trigger mode and one-shot select mode.
   - Sets the ANI2 and ANI19 pins for analog input and sets ANI19 as the conversion-start channel.
   - Sets the conversion time to $95/f_{CLK}$ (3.9583 us) in normal 1 mode.
   - Sets ADLL ≤ ADCR ≤ ADUL as the interrupt signal (INTAD) generation condition. Sets the upper limit ADUL to 255 and lower limit ADLL to 0.

10. After completing the initial settings, shifts the system to HALT mode.

11. Detects the human sensor by comparator 1. Measures the voltage applied to the volume pin by the A/D converter and determines the target current. Controls the LED current through the PWM output of the timer KB0. Measures the LED current by the PGA and A/D converter. Compares the target current to the LED current to control the PWM output of the timer KB0. Also detects the LED over-current.

5.2 List of Option Byte Settings

Table 5.1 shows the settings of the option bytes.

Table 5.1 Option Byte Settings

Address	Setting Value	Contents
000C0H	11101111B	Stops the watchdog timer (counting is stopped when a reset is released)
000C1H	01111111B	Sets the LVD in reset mode Detection voltage: 2.81V at the rising edge, 2.75V at the falling edge
000C2H	11100000B	Sets the high-speed on-chip oscillator clock to 24MHz in HS (high-speed main) mode
000C3H	10000100B	Enables on-chip debugging

5.3 List of Constants

Table 5.2 lists the constants that are used in the sample program.

Table 5.1 Constants for the Sample Program

Constant Name	Setting Value	Contents
—	—	—

5.4 List of Variables

Table 5.3 lists the global variables.

Table 5.2 Global Variables

Type	Variable Name	Contents	Function Used
unsigned int	INT12Count	Interrupt count value of 12-bit interval timer	main、 r_it_interrupt、 r_comp1_interrupt
unsigned int	ReqLEDValue	Target current value according to the A/D conversion result of the Volume input terminal	main、 r_tau0_channel0_ interrupt
unsigned int	FbLEDValue	LED current value by A/D conversion result of current detection terminal	main、 r_tau0_channel0_ interrupt
unsigned int	FbLEDValue_old	LED current value due to the A/D conversion result of the previous current detection terminal	main、 r_tau0_channel0_ interrupt
unsigned int	LEDDuty	Set on feedback TMKB compare register value	main、 r_tau0_channel0_ interrupt
unsigned int	LEDDuty_old	Timer KB compare register value set at previous feedback	main、 r_tau0_channel0_ interrupt

5.5 List of Functions

Table 5.4 lists the functions.

Table 5.3 Functions

Function Name	Outline
R_DAC0_Start	DAC0 operation start
R_PGA_Start	PGA operation start
R_COMP0_Start	Comparator 0 operation start
R_COMP1_Start	Comparator 1 operation start
R_IT_Start	12-bit interval timer operation start
R_TMR_KB_Start	16-bit timer KB0 operation start
R_IT_Stop	12-bit interval timer operation stop
R_TMR_KB_Stop	16-bit timer KB0 operation stop
r_comp0_interrupt	Comparator 0 interrupt processing
r_comp1_interrupt	Comparator 1 interrupt processing
r_it_interrupt	12-bit interval timer interrupt processing
r_tau0_channel0_interrupt	TAU0 interrupt processing

5.6 Function Specifications

This section gives the specifications of the functions used in the sample program.

R_ DAC0_Start

Outline	DAC0 operation start
Header	r_cg_dac.h
Declaration	void R_ DAC0_Start(void)
Description	Starts the D/A converter operation.
Arguments	None
Return Value	None
Remarks	None

R_ PGA_Start

Outline	PGA operation start
Header	r_cg_pga.h
Declaration	void R_ PGA_Start(void)
Description	Starts the PGA operation.
Arguments	None
Return Value	None
Remarks	None

R_ COMP0_Start

Outline	Comparator 0 operation start
Header	r_cg_comp.h
Declaration	void R_ COMP0_Start(void)
Description	Starts the Comparator 0 operation.
Arguments	None
Return Value	None
Remarks	None

R_COMP1_Start

Outline	Comparator 1 operation start
Header	r_cg_comp.h
Declaration	void R_ COMP1_Start(void)
Description	Starts the Comparator 1 operation.
Arguments	None
Return Value	None
Remarks	None

R_IT_Start

Outline	12-bit interval timer operation start
Header	r_cg_it.h
Declaration	void R_ IT_Start (void)
Description	Starts the 12-bit interval timer operation.
Arguments	None
Return Value	None
Remarks	None

R_TMR_KB0_Start

Outline	16-bit timer KB0 operation start
Header	r_cg_tmkb.h
Declaration	void R_TMR_KB0_Start (void)
Description	Starts the 16-bit timer KB0 operation.
Arguments	None
Return Value	None
Remarks	None

R_IT_Stop

Outline	12-bit interval timer operation stop
Header	r_cg_it.h
Declaration	void R_ IT_Stop (void)
Description	Stops the 12-bit interval timer operation.
Arguments	None
Return Value	None
Remarks	None

R_TMR_KB0_Stop

Outline	16-bit timer KB0 operation stop
Header	r_cg_tmkb.h
Declaration	void R_TMR_KB0_Start (void)
Description	Stops the 16-bit timer KB0 operation.
Arguments	None
Return Value	None
Remarks	None

r_comp0_interrupt

Outline	Comparator 0 interrupt processing
Header	r_cg_comp.h
Declaration	r_comp0_interrupt (void)
Description	Comparator 0 interrupt processing
Arguments	None
Return Value	None
Remarks	Alarm output. The forced output stop using the comparator 0 is processed by hardware.

r_comp1_interrupt

Outline	Comparator 1 interrupt processing
Header	r_cg_comp.h
Declaration	r_comp0_interrupt (void)
Description	Comparator 1 interrupt processing
Arguments	None
Return Value	None
Remarks	The operation of the timer array unit, the interval timer and the timer KB is started by sensing the human sensor.

r_it_interrupt

Outline	12-bit interval timer interrupt processing
Header	r_cg_it.h
Declaration	r_it_interrupt(void)
Description	12-bit interval timer interrupt processing
Arguments	None
Return Value	None
Remarks	None

r_tau0_channel0_interrupt

Outline	TAU0 interrupt processing
Header	r_cg_tau.h
Declaration	r_tau0_channel0_interrupt (void)
Description	TAU0 interrupt processing
Arguments	None
Return Value	None
Remarks	Change the duty ratio of Volume input and LED current measurement, PWM output.

5.7 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

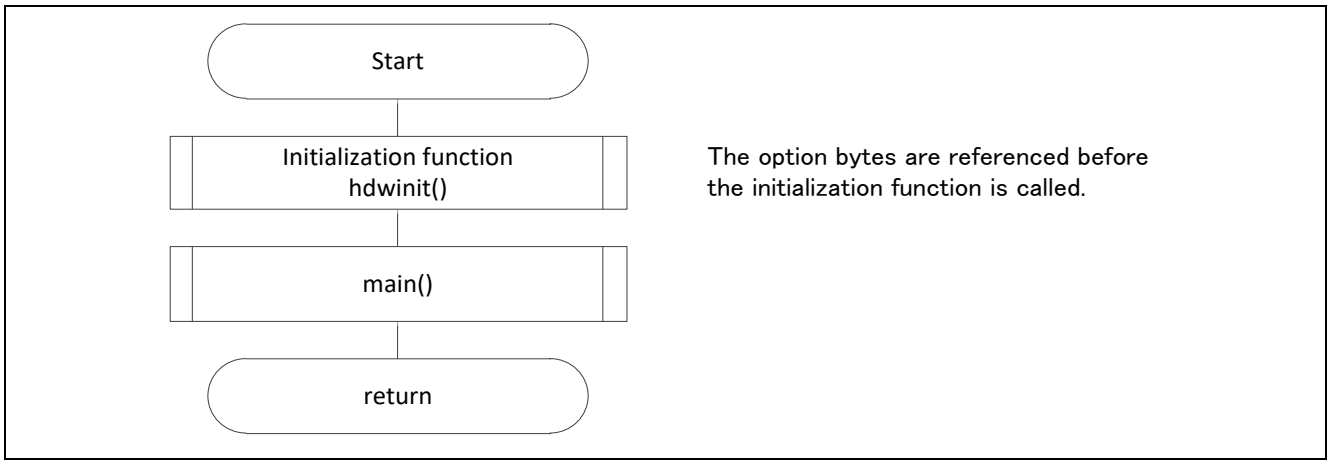

Figure 5.1 Overall Flow

Note: The start-up routine is executed before and after the initial setting function.

5.7.1 Initial Setting Function

Figure 5.2 shows the flowchart for the initial setting function.

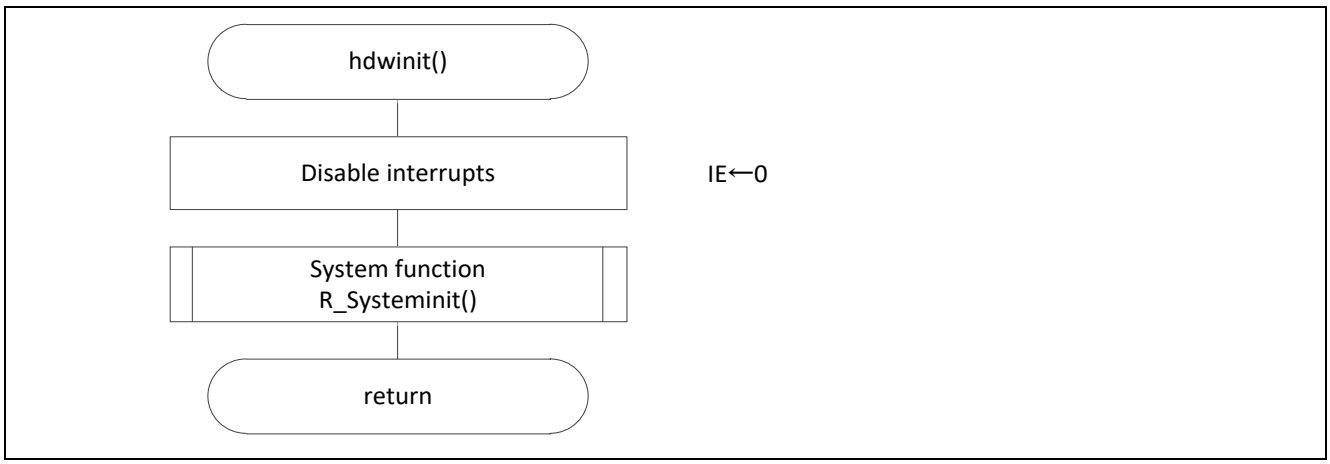

Figure 5.2 Initial Setting Function

5.7.2 System Function

Figure 5.3 shows the flowchart for the system function.

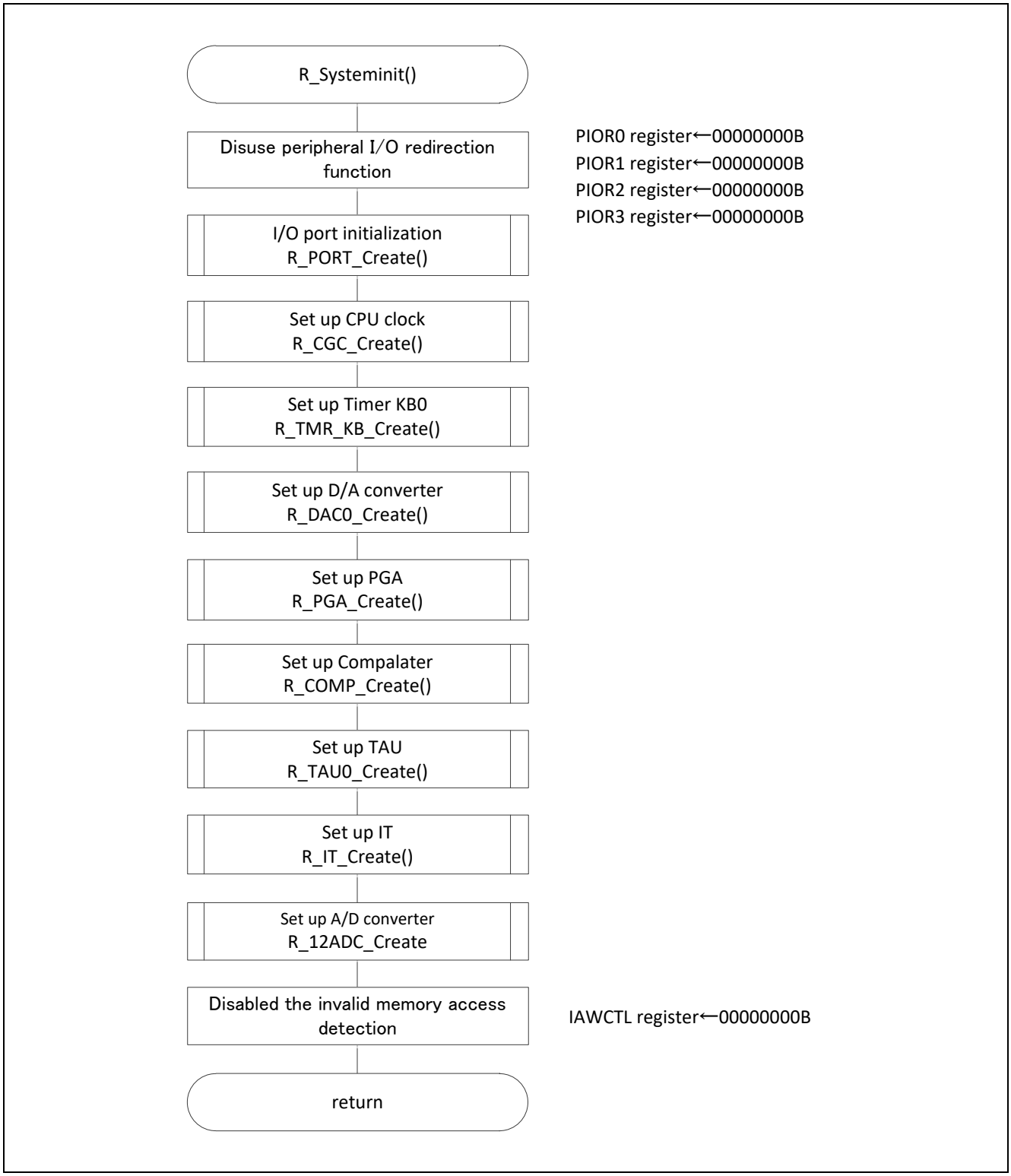

図 5.3 システム関数

5.7.3 Setting I/O Ports

Figure 5.4 shows the flowchart for setting the I/O ports.

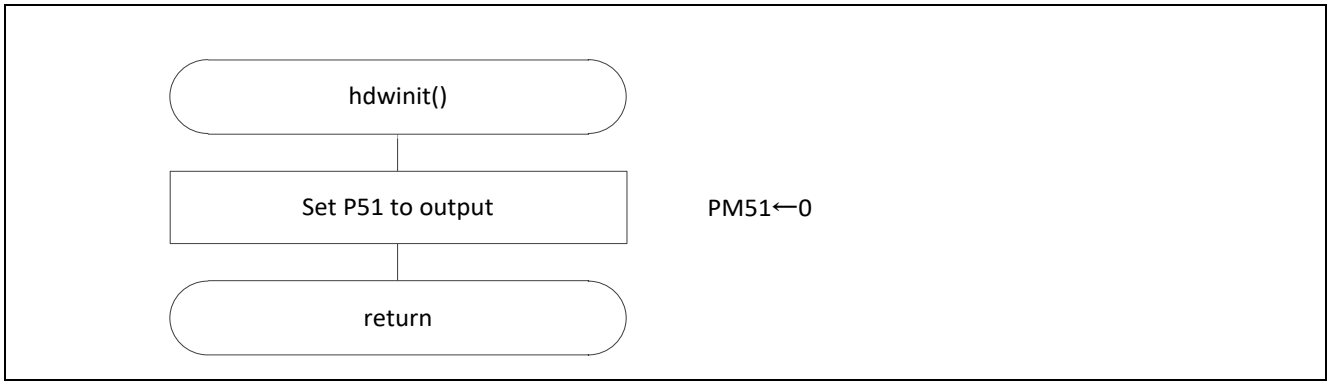

Figure 5.4 Setting I/O Ports

Note: Refer to RL78/G11 User's Manual: Hardware for the configuration of the unused ports.

Caution: Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

5.7.4 Setting CPU Clocks

Figure 5.5 shows the flowchart for setting the CPU clocks.

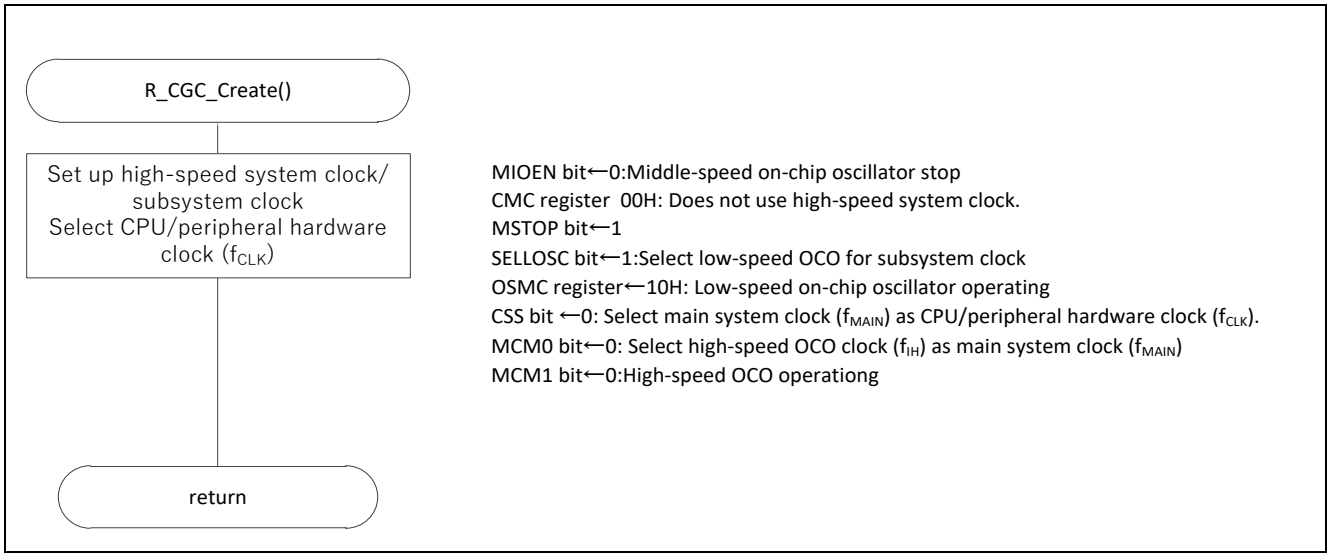

Figure 5.5 Setting CPU Clock

5.7.5 Setting Timer KB0

Figure 5.6 shows the flowchart for setting the timer KB0.

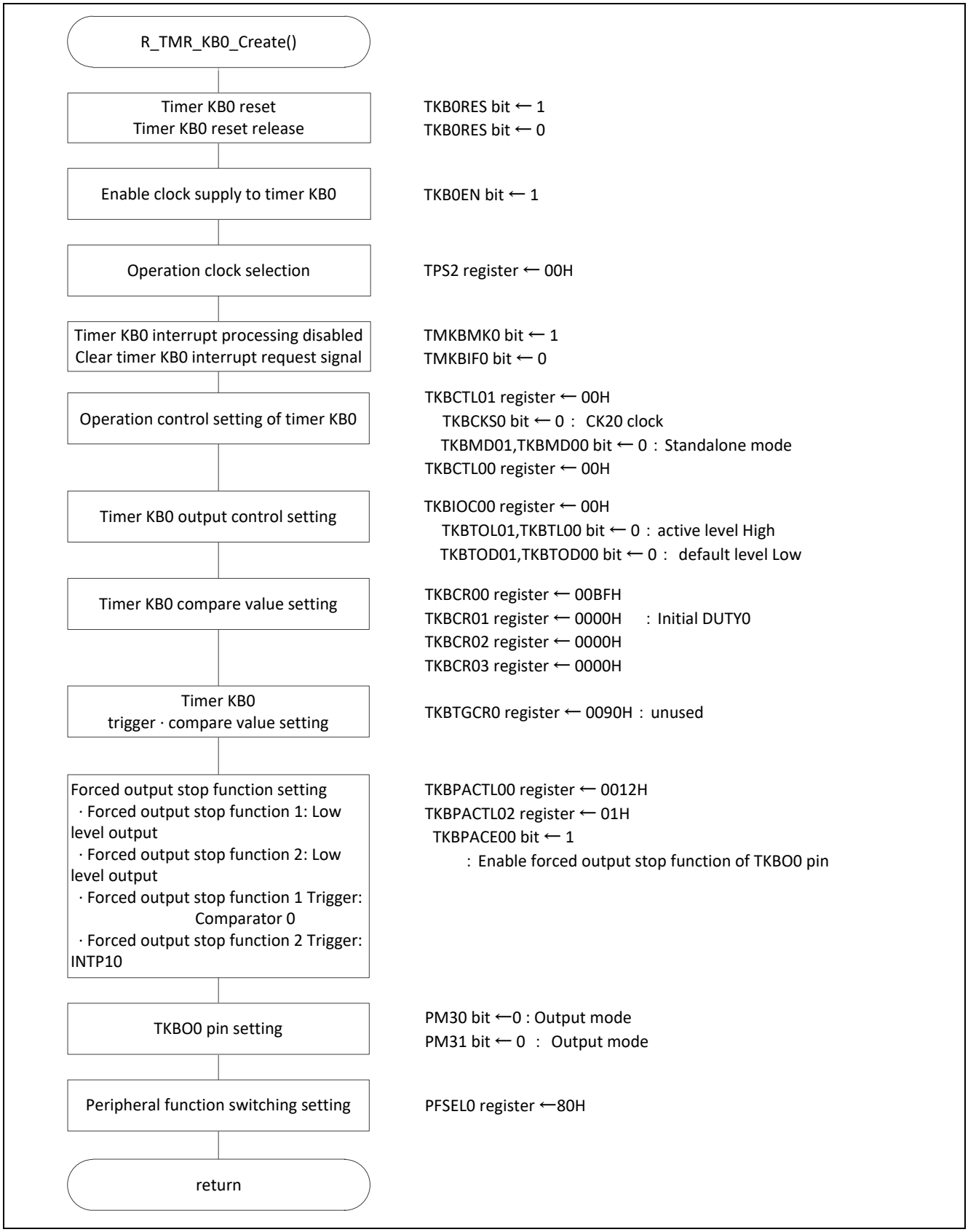

Figure 5.6 Setting Timer KB0

Controlling timer KB0 reset

- Peripheral reset control register 2 (PRR2)
  Control reset of the timer KB0.

Symbol：PRR2

7	6	5	4	3	2	1	0
TMKARES	0	DOCRES	0	0	0	0	TKB0RES
x	0	x	0	0	0	0	**1/0**

Bit 0

TKB0RES	Reset control of 16-bit timer KB0
0	**16-bit timer KB0 is released from the reset state**.
1	**16-bit timer KB0 is in the reset state**

Starting clock supply to timer KB0

- Peripheral enable register 2 (PER2)
  Start supplying clock to the timer KB0.

Symbol: PER2

7	6	5	4	3	2	1	0
TMKAEN	0	DOCEN	0	0	0	0	TKB0EN
x	0	x	0	0	0	0	**1**

Bit 0

TKB0EN	Control of timer KB0 input clock
0	Stops supply of input clock.
1	**Supplies input clock.**

Caution: For details on the register setup procedures, refer to RL78/G11 User's Manual: Hardware.

Setting timer KB0 operation clock

- Timer clock select register 2 (TPS2)
  Select the timer KB0 operation clock.

Symbol: TPS2

7	6	5	4	3	2	1	0
0	TPS212	TPS211	TPS210	0	TPS202	TPS201	TPS200
0	**0**	**0**	**0**	0	**0**	**0**	**0**

User option byte (000C2H/010C2H) FRQSEL4 = 1

TPS202	TPS201	TPS200	Selection of operation clock (CK20)				
				f_{HOCO} = 6 MHz	f_{HOCO} = 12 MHz	F_{HOCO} = 24 MHz	F_{HOCO} = 48 MHz
0	**0**	**0**	**f_{HOCO}**	6 MHz	12 MHz	24 MHz	**48MHz**
0	0	1	$f_{HOCO}/2$	3 MHz	6 MHz	12 MHz	12 MHz
0	1	0	$f_{HOCO}/2^2$	1.5 MHz	3 MHz	6 MHz	6 MHz
0	1	1	$f_{HOCO}/2^3$	750 kHz	1.5 MHz	3 MHz	3 MHz
1	0	0	$f_{HOCO}/2^4$	375kHz	750 kHz	1.5 MHz	1.5 MHz
1	0	1	$f_{HOCO}/2^5$	187.5kHz	375kHz	750 kHz	750 kHz
Other than the above			Setting prohibited				

Caution: For details on the register setup procedures, refer to RL78/G11 User's Manual: Hardware.

Setting timer KB0 interrupts

- Interrupt request flag register (IF2L)
  Clear the relevant interrupt request flag.
- Interrupt mask flag register (MK2L)
  Disable the relevant interrupt processing.

Symbol：IF2L

7	6	5	4	3	2	1	0
FLIF	IICAIF1	TMKBIF0	ITIF01	ITIF00	DOCIF	CMPIF1	CMPIF0
x	x	**0**	x	x	x	x	x

Bit 5

TMKBIF0	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol：MK2L

7	6	5	4	3	2	1	0
FLMK	IICAMK1	TMKBMK0	ITMK01	ITMK00	DOCMK	CMPMK1	CMPMK0
X	x	**1**	x	x	x	x	x

Bit 5

TMKBMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Caution: For details on the register setup procedures, refer to RL78/G11 User's Manual: Hardware.

Controlling timer KB operation

- 16-bit timer KB2 operation control register 01 (TKBCTL01)
  Control the timer KB0 operation.
  Select the timer KB0 clock.
  Select the timer KB0 operation mode.

Symbol：TKBCTL01

7	6	5	4	3	2	1	0
TKBCE0	0	0	TKBCKS0	0	0	TKBMD01	TKBMD00
0	0	0	**0**	0	0	**0**	**0**

Bit 7

TKBCE0	Timer KB0 operation control
0	**Stops timer operation (counter is set to FFFF).**
1	Enables timer count operation.

Bit 4

TKBCKS0	Timer KB0 clock selection
0	**CK20 clock selected by TPS202 to TPS200 bits**
1	CK21 clock selected by TPS212 to TPS210 bits

Bit 1 to 0

TKBMD01	TKBMD00	Timer KB0 operation mode selection
0	**0**	**Standalone mode (uses master)**
1	1	Interleave PFC output mode
Other than the above		Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G11 User's Manual: Hardware.

Controlling timer KB0 output levels

- 16-bit timer KB2 output control register 00 (TKBIOC00)
  Set the active level of the timer output TKBO0.
  Set the default level of the timer output TKBO2.

Symbol：TKBIOC00

7	6	5	4	3	2	1	0
0	0	0	0	TKBTOL01	TKBTOL00	TKBTOD01	TKBTOD00
0	0	0	0	**0**	**0**	**0**	**0**

Bit 3 and 2

TKBTOL0n	Active level setting of timer output TKBOp
0	**High level**
1	Low level

Bit 1 and 0

TKBTOD0n	Default level setting of timer output TKBOp
0	**Low level**
1	High level

Caution: For details on the register setup procedures, refer to RL78/G11 User's Manual: Hardware.

Controlling timer KB0 forced output stop function

- Forced output stop function control register 00 (TKBPACTL00)
  Select the external interrupt trigger, comparator trigger, and operation mode for forced output stop function 2.
  Select the comparator trigger, output status, and cancellation condition for forced output stop function 1.

- Forced output stop function control register 02 (TKBPACTL02)
  Control trigger signal input.

Symbol：TKBPACTL00

15	14	13	12	11	10	9	8
TKBPAFXS013	TKBPAFXS012	TKBPAFXS011	TKBPAFXS010	0	0	0	TKBPAFCM01
0	**0**	**0**	**0**	0	0	0	**0**

7	6	5	4	3	2	1	0
0	0	TKBPAHZS011	TKBPAHZS010	KBPAHCM011	KBPAHCM010	TKBPAMD011	TKBPAMD010
0	0	**0**	**1**	**0**	**0**	**1**	**0**

Bit 15

TKBPAFXS013	External interruption trigger selection for forced output stop function 2
0	**INTP11 cannot be used as a trigger**
1	INTP11 can be used as a trigger

Bit 14

TKBPAFXS012	External interruption trigger selection for forced output stop function 2
0	**INTP10 cannot be used as a trigger**.
1	INTP10 can be used as a trigger

Bit 13

TKBPAFXS011	Comparator trigger selection for forced output stop function 2
0	**Comparator 1 cannot be used as a trigger.**
1	Comparator 1 can be used as a trigger

Bit 12

TKBPAFXS010	Comparator trigger selection for forced output stop function 2
0	**Comparator 0 cannot be used as a trigger.**
1	Comparator 0 can be used as a trigger

Bit 8

TKBPAFCM01	Operation mode selection for forced output stop function 2
0	**Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period**
1	Forced output stop function 2 starts with trigger input, and forced output stop function 2 is cleared at the next counter period following detection of the reverse edge of the trigger

Caution: For details on the register setup procedures, refer to RL78/G11 User's Manual: Hardware.

Symbol：TKBPACTL00

15	14	13	12	11	10	9	8
TKBPAFXS013	TKBPAFXS012	TKBPAFXS011	TKBPAFXS010	0	0	0	TKBPAFCM01
0	**0**	**0**	**0**	0	0	0	**0**

7	6	5	4	3	2	1	0
0	0	TKBPAHZS011	TKBPAHZS010	KBPAHCM011	KBPAHCM010	TKBPAMD011	TKBPAMD010
0	0	**0**	**1**	**0**	**0**	**1**	**0**

Bit 5

TKBPAHZS011	Comparator trigger selection for forced output stop function 1
0	**Comparator 1 cannot be used as a trigger.**
1	Comparator 1 can be used as a trigger.

Bit 4

TKBPAHZS010	Comparator trigger selection for forced output stop function 1
0	Comparator 0 cannot be used as a trigger.
1	**Comparator 0 can be used as a trigger.**

Bit 3 and 2

TKBPAHCM011	TKBPAHCM010	Clear condition selection for forced output stop function 1
0	**0**	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared when forced output stop function release trigger (TKBPAHTT0p) = 1 is written, regardless of the trigger signal level.
0	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing “forced output stop function release trigger (TKBPAHTT0p) = 1” is invalid. Forced output stop function 1 is cleared when forced output stop function release trigger (TKBPAHTT0p) = 1 is written while the trigger signal is in its inactive period.
1	0	Forced output stop function 1 starts with trigger input, and forced output stop function 1 is cleared at the next counter period after forced output stop function release trigger (TKBPAHTT0p) = 1 is written, regardless of the trigger signal level.
1	1	Forced output stop function 1 starts with trigger input, and when the trigger signal is in its active period, writing “forced output stop function release trigger (TKBPAHTT0p) = 1” is invalid. Forced output stop function 1 is cleared at the next counter period after forced output stop function release trigger (TKBPAHTT0p) = 1 is written when the trigger signal is in its inactive period.

Caution: For details on the register setup procedures, refer to RL78/G11 User's Manual: Hardware.

Symbol：TKBPACTL00

15	14	13	12	11	10	9	8
TKBPAFXS013	TKBPAFXS012	TKBPAFXS011	TKBPAFXS010	0	0	0	TKBPAFCM01
0	**0**	**0**	**0**	0	0	0	**0**

7	6	5	4	3	2	1	0
0	0	TKBPAHZS011	TKBPAHZS010	KBPAHCM011	KBPAHCM010	TKBPAMD011	TKBPAMD010
0	0	**0**	**1**	**0**	**0**	**1**	**0**

Bit 1 and 0

TKBPAMD011	TKBPAMD010	Output status selection when executing forced output stop function	
		Forced output stop function 1	Forced output stop function 2
0	0	Hi-Z output	Output fixed at low level
0	1	Hi-Z output	Output fixed at high level
1	**0**	**Output fixed at low level**	**Output fixed at low level**
1	1	Output fixed at high level	Output fixed at high level

Caution: For details on the register setup procedures, refer to RL78/G11 User's Manual: Hardwar

Symbol：TKBPACTL02

7	6	5	4	3	2	1	0
0	0	0	0	0	0	TKBPACE01	TTKBPACE00
0	0	0	0	0	0	**0**	**1**

Bit 1 and 0

TKBPACE0n	Input control of trigger signal used for forced output stop function of the TKBOp pin.
0	**Disable operation of forced output stop function**
1	**Enable operation of forced output stop function**

Caution: For details on the register setup procedures, refer to RL78/G11 User's Manual: Hardware.

5.7.6 Setting D/A Converter

Figure 5.7 shows the flowchart for setting the D/A converter.

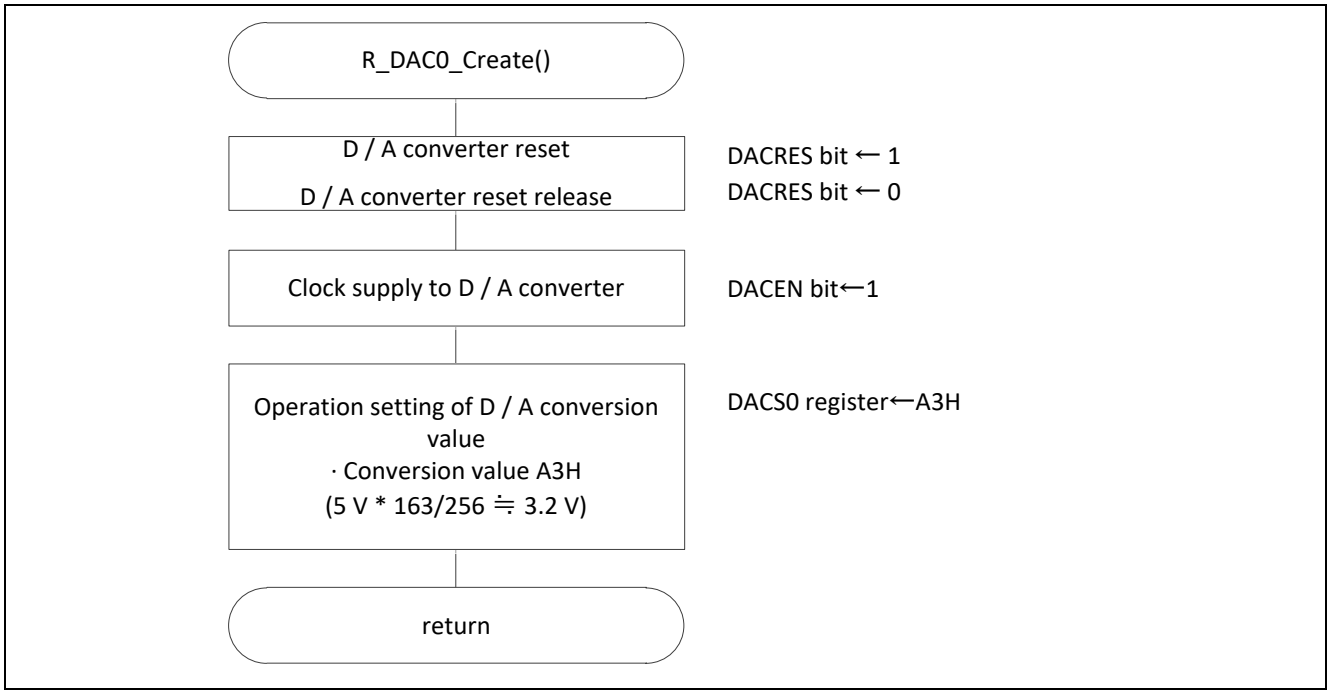

Figure 5.7 Setting D/A Converter

Setting peripheral reset for D/A converter

- Peripheral reset control register 1 (PRR1)
  Control peripheral reset for the D/A converter.

Symbol：PRR1

7	6	5	4	3	2	1	0
DACRES	0	CMPRES	0	0	PGA0RES	0	0
0/1	0	x	0	0	x	0	0

Bit 7

DACRES	Reset control of DAC
0	**D/A converter is released from the reset state.**
1	**D/A converter is in the reset state.**

Starting clock supply to D/A converter

- Peripheral enable register 1 (PER1)
  Start supplying clock to the D/A converter.

Symbol：PER1

7	6	5	4	3	2	1	0
DACEN	0	CMPEN	0	DTCEN	PGA0EN	0	0
1	0	x	0	x	x	0	0

Bit 0

DACEN	Control of D/A converter input clock
0	Stops input clock supply.
1	**Supplies input clock.**

Caution: For details on the register setup procedures, refer to RL78/G11 User's Manual: Hardware.

Setting D/A conversion value

- D/A conversion value setting register 0 (DACS0)
  Set the analog voltage value to be output to the D/A converter pins.

Symbol：DACS0

7	6	5	4	3	2	1	0
DACS07	DACS06	DACS05	DACS04	DACA03	DACS02	DACS01	DACS00
1	**0**	**1**	**0**	**0**	**0**	**1**	**1**

Caution: For details on the register setup procedures, refer to RL78/G11 User's Manual: Hardware.

5.7.7 Setting Programmable Gain Amplifier (PGA)

Figure 5.8 shows the flowchart for setting the PGA.

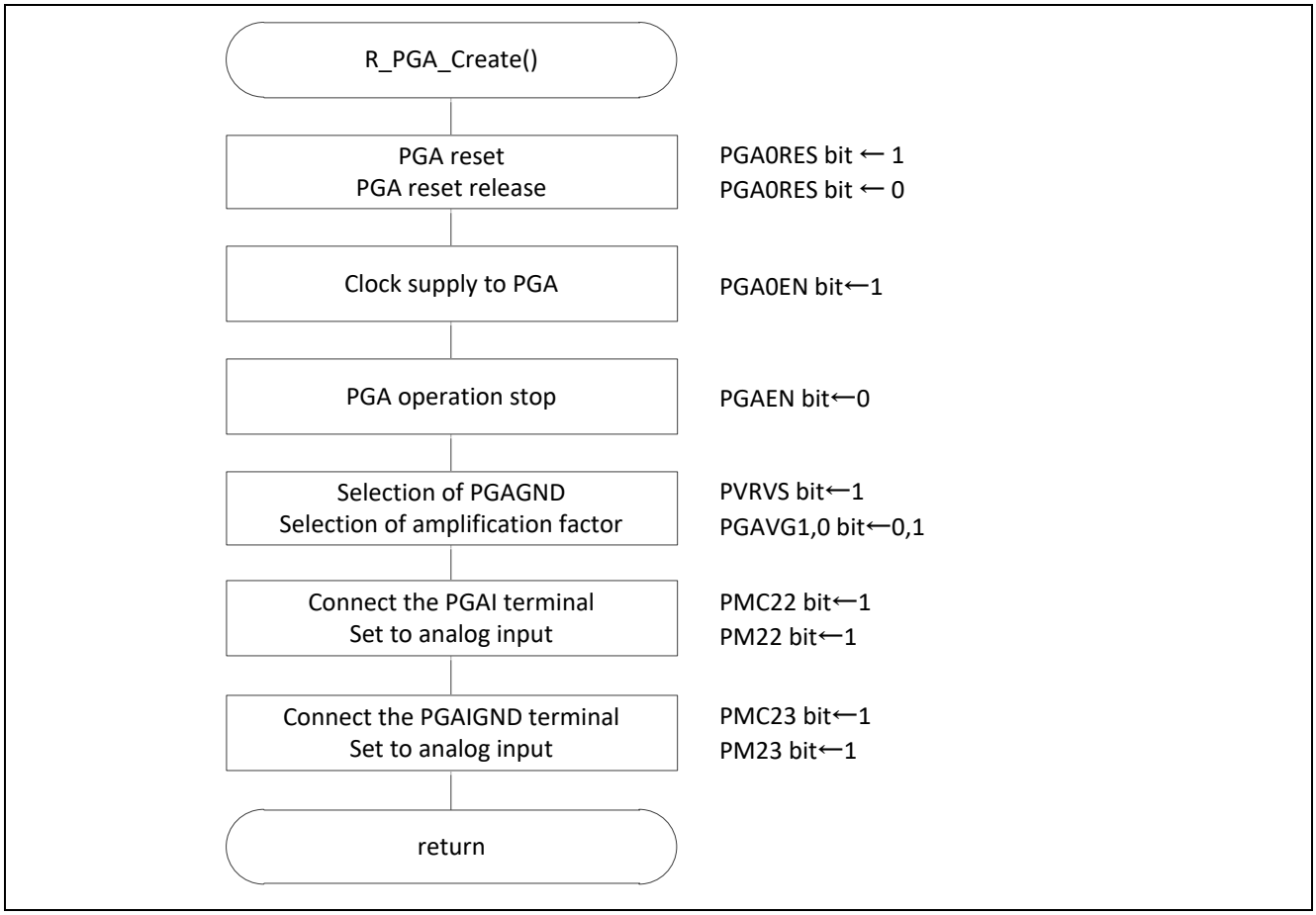

Figure 5.8 Setting PGA

Starting clock supply to PGA

- Peripheral enable register 1 (PER1)
  Start supplying clock to the PGA.

Symbol：PER1

7	6	5	4	3	2	1	0
DACEN	0	CMPEN	0	DTCEN	PGA0EN	0	0
x	0	x	0	x	1	0	0

Bit 2

PGA0EN	Programmable gain amplifier input clock control
0	• SFR used by the programmable gain amplifier cannot be written. • Programmable gain amplifier is not initialized.
1	**• SFR used by the programmable gain amplifier can be read/written.**

Selecting GND and amplification factor for PGA

- PGA control register (PGACTL)
  Set PGA operation.

Symbol：PGACTL

7	6	5	4	3	2	1	0
PGAEN	0	0	0	PVRVS	0	PGAVG1	PGAVG0
x	0	0	0	**1**	0	**0**	**1**

Bit 3

PVRVS	GND selection of feedback resistance of the programmable gain amplifier
0	Selects V_{SS}.
1	**Selects PGAGND.**

Bit 1 and 0

PGAVG1	PGAVG0	Programmable gain amplifier amplification factor selection
0	0	×4
0	**1**	**×8**
1	0	×16
1	1	×32

5.7.8 Setting Comparator

Figure 5.9 shows the flowchart for setting the comparator.

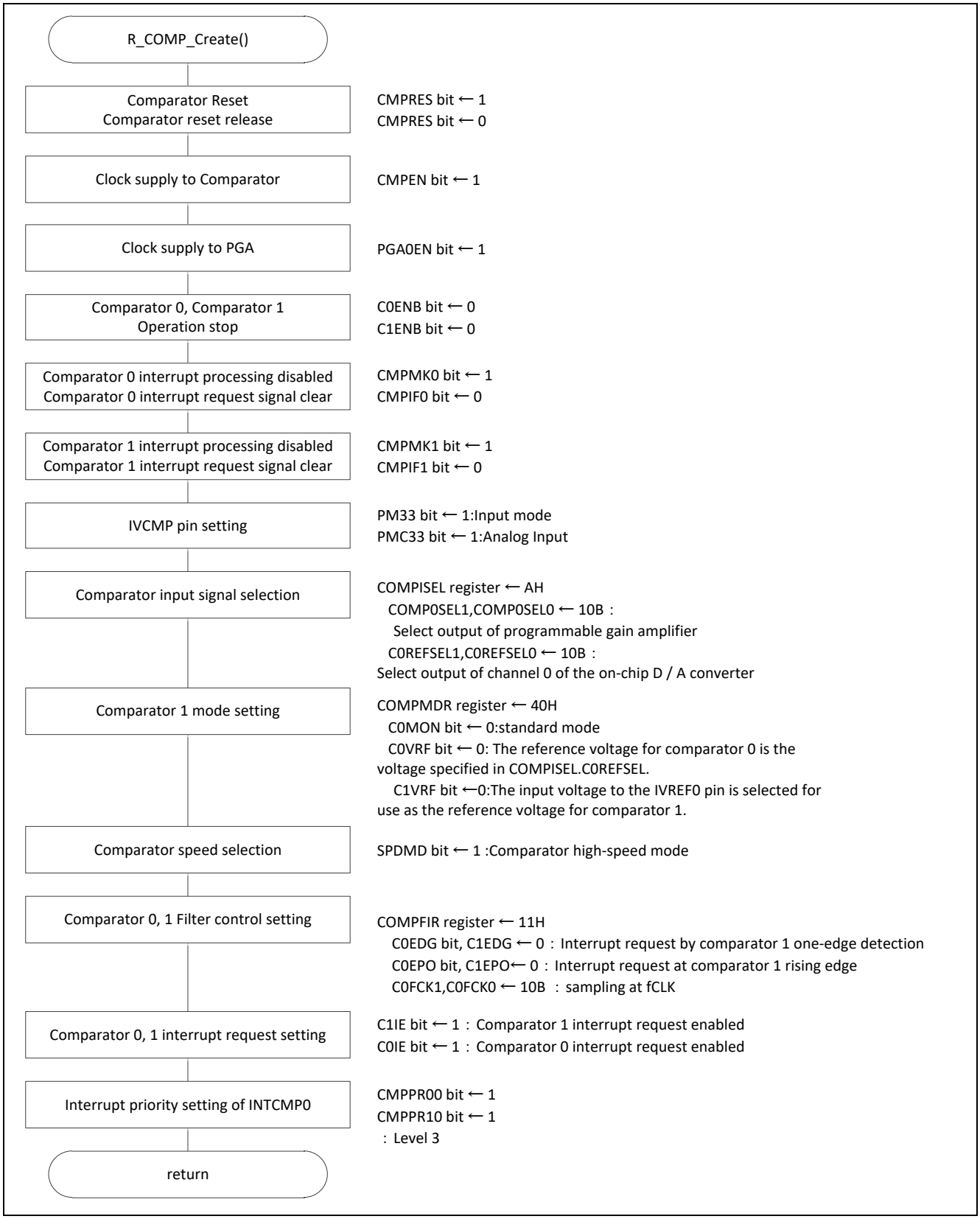

Figure 5.9 Setting Comparator

Starting clock supply to comparator

- Peripheral enable register 1 (PER1)
  Start supplying clock to the comparator.

Symbol：PER1

7	6	5	4	3	2	1	0
DACEN	0	CMPEN	0	DTCEN	PGA0EN	0	0
x	0	**1**	0	x	1	0	0

Bit 5

CMPEN	Control of comparator input clock
0	Stops input clock supply.
1	**Supplies input clock**

Bit 2

PGA0EN	Programmable gain amplifier input clock control
0	• SFR used by the programmable gain amplifier cannot be written. • Programmable gain amplifier is not initialized.
1	**• SFR used by the programmable gain amplifier can be read/written.**

Setting comparator operation

- Comparator mode setting register (COMPMDR)
Enable comparator operation.

Symbol：COMPMDR

7	6	5	4	3	2	1	0
C1MON	C1VRF	C1WDE	C1ENB	C0MON	C0VRF	C0WDE	C0ENB
x	x	x	**0**	x	x	x	**0**

Bit 4

C1ENB	Comparator 1 operation enable
0	**Comparator 1 operation disabled**
1	Comparator 1 operation enabled

Bit 0

C0ENB	Comparator 0 operation enable
0	**Comparator 0 operation disabled**
1	Comparator 0 operation enabled

Caution: For details on the register setup procedures, refer to RL78/G11 User's Manual: Hardware.

Setting comparator interrupts

- Interrupt request flag register (IF2L)
  Clear the relevant interrupt request flag.
- Interrupt mask flag register (MK2L)
  Disable the relevant interrupt.

Symbol：IF2L

7	6	5	4	3	2	1	0
FLIF	IICAIF1	TMKBIF0	ITIF01	ITIF00	DOCIF	CMPIF1	CMPIF0
x	x	x	x	x	x	**0**	**0**

Bits 1 and 0

CMPIF0,1	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol：MK2L

7	6	5	4	3	2	1	0
FLMK	IICAMK1	TMKBMK0	ITMK01	ITMK00	DOCMK	CMPMK1	CMPMK0
x	x	x	x	x	x	**1**	**1**

Bits 5 and 4

CMPMK0,1	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Setting peripheral reset for comparator

- Peripheral reset control register 1 (PRR1)
  Control peripheral reset for the comparator.

Symbol：PRR1

7	6	5	4	3	2	1	0
DACRES	0	CMPRES	0	0	PGA0RES	0	0
x	0	**0/1**	0	0	x	0	0

Bit 5

CMPRES	Peripheral reset control on each peripheral hardware
0	**Peripheral module is released from the reset state.**
1	**Peripheral module is in the reset state.**

Caution: For details on the register setup procedures, refer to RL78/G11 User's Manual: Hardware.

5.7.9 Setting Timer Array Unit

Figure 5.10 shows the flowchart for setting the timer array unit.

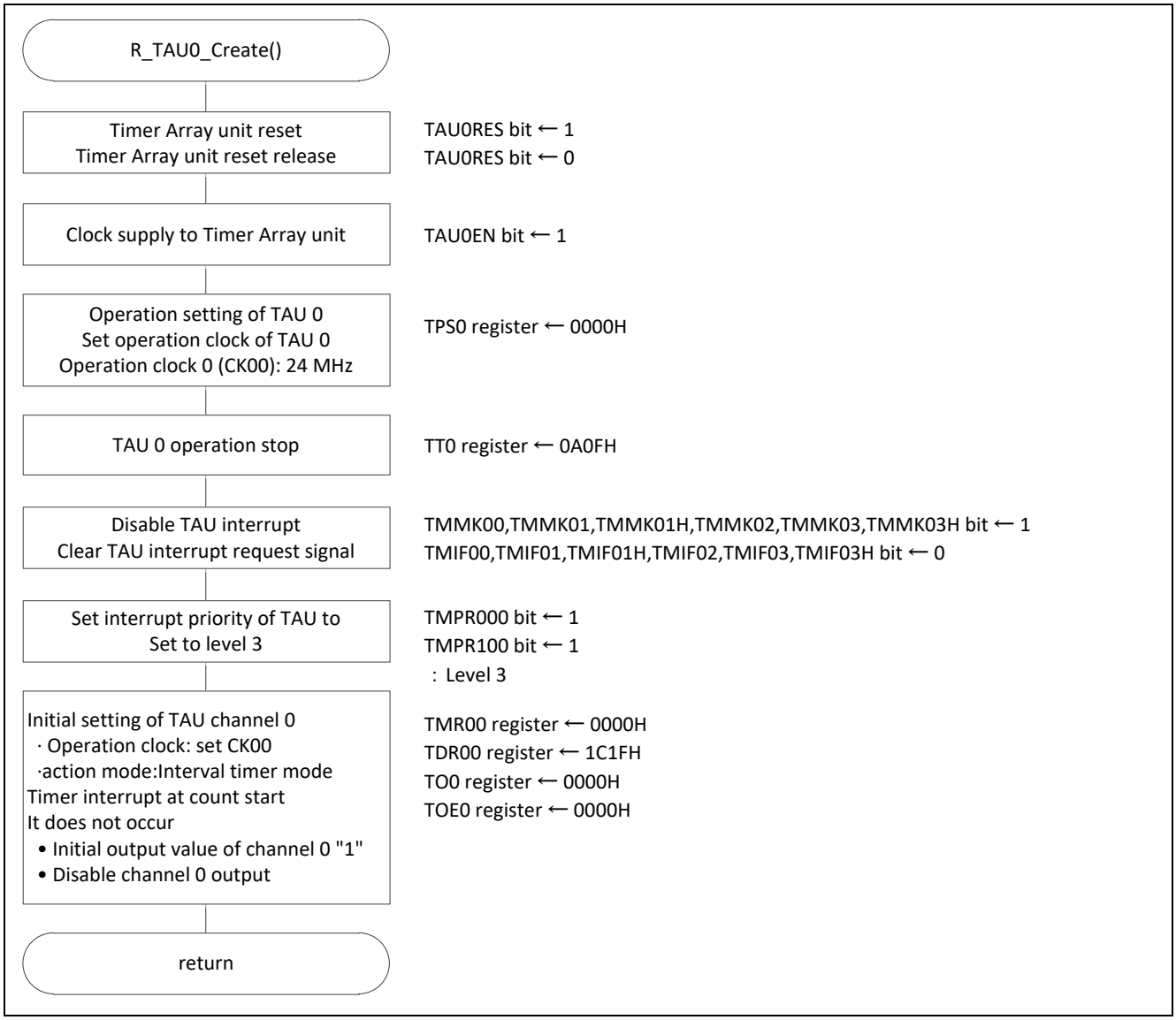

Figure 5.10 Setting Timer Array Unit

Starting clock supply to timer array unit 0

- Peripheral enable register 0 (PER0)
  Start supplying clock to the timer array unit 0.

Symbol：PER0

7	6	5	4	3	2	1	0
0	IICA1EN	ADCEN	IICA0EN	0	SAU0EN	0	TAU0EN
0	x	x	x	0	x	0	**1**

Bit 0

TAU0EN	Control of timer array 0 unit input clock
0	Stops supply of input clock.
1	**Supplies input clock.**

Setting timer clock frequency

- Timer clock select register 0 (TPS0)
  Select the operating clock for timer array unit 0.

Symbol：TPS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	PRS031	PRS030	0	0	PRS021	PRS020	PRS013	PRS012	PRS011	PRS010	PRS003	PRS002	PRS001	PRS000
x	x	x	x	x	x	x	x	x	x	x	x	**0**	**0**	**0**	**0**

Bit 3 to 0

PRS003	PRS002	PRS001	PRS000		Selection of operation clock (CK00)				
					f_{CLK}= 2MHz	f_{CLK}= 5MHz	f_{CLK}= 10MHz	f_{CLK}= 20MHz	f_{CLK}= 24MHz
0	**0**	**0**	**0**	**f_{CLK}**	2 MHz	5 MHz	10 MHz	20 MHz	**24 MHz**
0	0	0	1	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz	12 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz	6 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz	3 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	312.5 kHz	625 kHz	1.25 MHz	1.5 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	156.2 kHz	313kHz	625 kHz	750 kHz
0	1	1	0	$f_{CLK}/2^6$	31.25 kHz	78.1 kHz	156 kHz	313 kHz	375 kHz
0	1	1	1	$f_{CLK}/2^7$	15.62 kHz	39.1 kHz	78.1 kHz	156 kHz	187.5 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	19.5 kHz	39.1 kHz	78.1 kHz	93.8 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	9.76 kHz	19.5 kHz	39.1 kHz	46.9 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	4.88 kHz	9.77 kHz	19.5 kHz	23.4 kHz
1	0	1	1	$f_{CLK}/2^{11}$	976 Hz	2.44 kHz	4.88 kHz	9.77 kHz	11.7 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	1.22 kHz	2.44 kHz	4.88 kHz	5.86 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	610 Hz	1.22 kHz	2.44 kHz	2.93 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	305 Hz	610 Hz	1.22 kHz	1.46 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61 Hz	153 Hz	305 Hz	610 Hz	732 Hz

Caution: For details on the register setup procedures, refer to RL78/G11 User's Manual: Hardware.

Setting channel 0 operation mode

- Timer mode register 00 (TMR00)
  Select operating clock (f_{MCK}).
  Select the counting clock.
  Set software trigger start.
  Set the operation mode.

Symbol：TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	CKS 000	0	CCS 00	0	STS 002	STS 001	STS 000	CIS 001	CIS 000	0	0	MD 003	MD 002	MD 001	MD 000
0	**0**	0	**0**	0	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**0**

Bit 15and 14

CKS001	CKS000	Selection of operation clock (f_{MCK}) of channel 0
0	**0**	**Operation clock CKm0 set by timer clock select register m (TPSm)**
0	1	Operation clock CKm2 set by timer clock select register m (TPSm)
1	0	Operation clock CKm1 set by timer clock select register m (TPSm)
1	1	Operation clock CKm3 set by timer clock select register m (TPSm

Bit 12

CCS00	Selection of count clock (f_{TCLK}) of channel 0
0	**Operation clock (f_{MCK}) specified by the CKSmn0 and CKSmn1 bits**
1	Valid edge of input signal input from the TImn pin In channels 0 and 1, valid edge of input signal selected by TIS0

Bits 10 to 8

STS002	STS001	STS000	Setting of start trigger or capture trigger of channel 1
0	**0**	**0**	**Only software trigger start is valid (other trigger sources are unselected).**
0	0	1	Valid edge of the TImn pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TImn pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
1	1	0	INTTMmn of the master channel is used as a start trigger, and the valid edge of the TImp pin input of the slave channel is used as a end trigger (capture trigger).
Other than the above			Setting prohibited

Bits 7 and 6

CIS001	CIS000	Selection of TImn pin input valid edge
0	**0**	**Falling edge**
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: Falling edge, Capture trigger: Rising edge
1	1	Both edges (when high-level width is measured) Start trigger: Rising edge, Capture trigger: Falling edge

Caution: For details on the register setup procedures, refer to RL78/G11 User's Manual: Hardware.

Symbol：TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	CKS 000	0	CCS 00	0	STS 002	STS 001	STS 000	CIS 001	CIS 000	0	0	MD 003	MD 002	MD 001	MD 000
0	**0**	0	**0**	0	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**0**

Bits 3 to 0

MD 003	MD 002	MD 001	Operation mode of channel 1	Corresponding function	Count operation of TCR
0	**0**	**0**	**Interval timer mode**	**Interval timer / Square wave output / Divider function / PWM output (master)**	**Counting down**
0	1	0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	Event counter mode	External event counter	Counting down
1	0	0	One-count mode	Delay counter / One-shot pulse output / PWM output (slave)	Counting down
1	1	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than the above			Setting prohibited		
The operation of each mode varies depending on MDmn0 bit (see table below).					

Operation mode (Value set by the MDmn3 to MDmn1 bits (see table above))	MD000	Setting of starting counting and interrupt
• Interval timer mode (0, 0, 0) **• Capture mode (0, 1, 0)**	**0**	**Timer interrupt is not generated when counting is started (timer output does not change, either).**
	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated.
	1	Start trigger is valid during counting operation At that time, interrupt is not generated
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time, interrupt is not generated.

Caution: For details on the register setup procedures, refer to RL78/G11 User's Manual: Hardware.

Setting interval for interval timer

- Timer data register 01 (TDR01)
  Set the compare value for the interval timer.

Symbol：TDR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Generation of timer interrupt (INTTM01) = (TDR01 set value + 1) × count clock period

Enabling timer output

- Timer output enable register 0 (TOE0)
  Enable or disable timer output of each channel.

Symbol：TOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	TOE07	TOE06	TOE05	TOE04	TOE03	TOE02	TOE01	TOE00
0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	**0**

Bit 1

TOE01	Timer output enable/disable of channel 0
0	**Timer output is disabled.** **Timer operation is not applied to the TOmn bit and the output is fixed.** **Writing to the TOmn bit is enabled and the level set in the TOmn bit is output from the TOmn pin.**
1	Timer output is enabled. Timer operation is applied to the TOmn bit and an output waveform is generated. Writing to the TOmn bit is ignored.

Caution: For details on the register setup procedures, refer to RL78/G11 User's Manual: Hardware.

5.7.10 Setting 12-Bit Interval Timer

Figure 5.11 shows the flowchart for setting the 12-bit interval timer

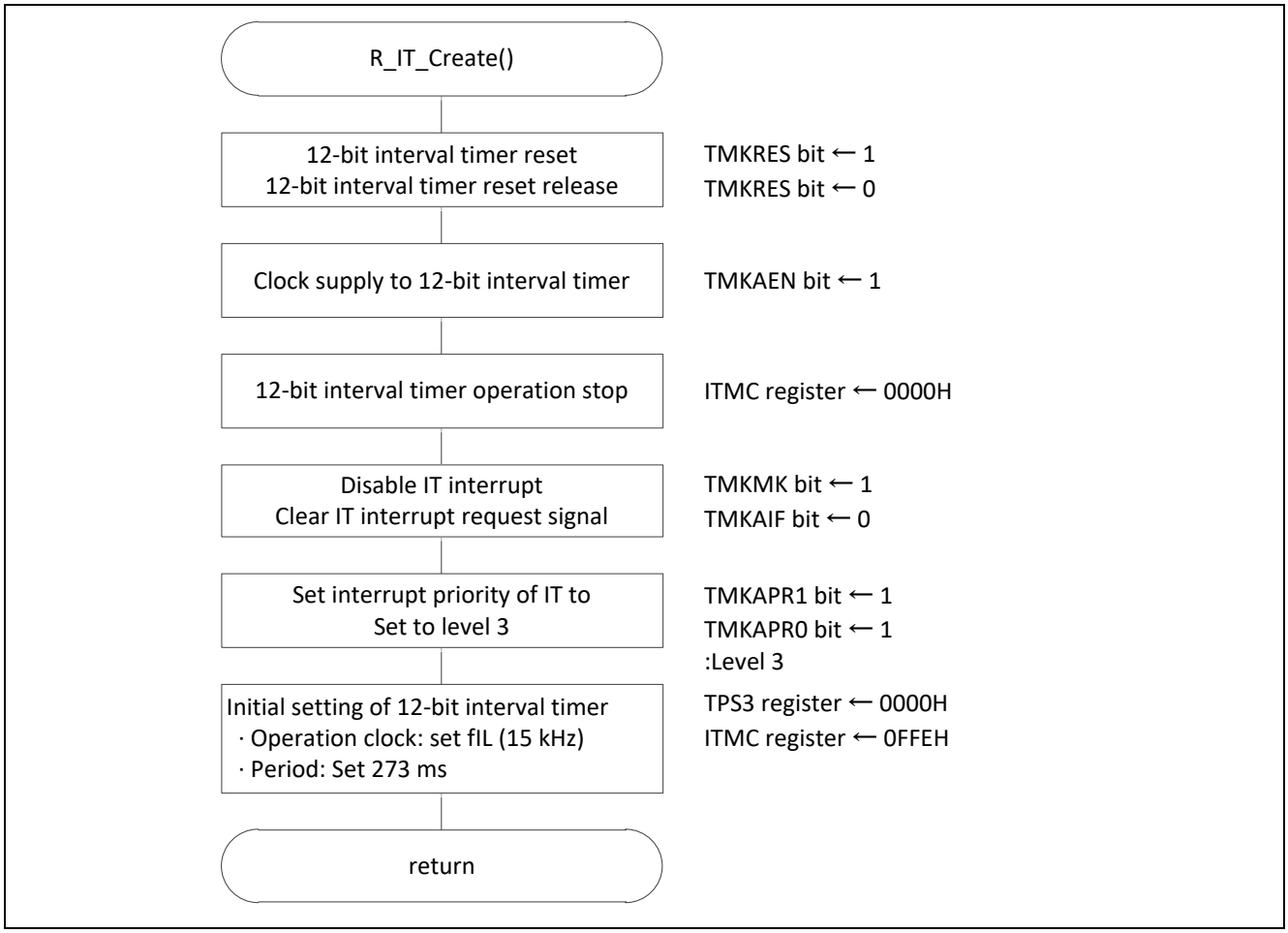

Figure 5.11 Setting 12-Bit Interval Timer

Starting clock supply to 12-bit interval timer

- Peripheral enable register 2 (PER2)
  Start supplying clock to the 12-bit interval timer.

Symbol：PER2

7	6	5	4	3	2	1	0
TMKAEN	0	DOCEN	0	0	0	0	TKB0EN
1	0	x	0	0	0	0	x

Bit 7

TMKAEN	Control of 12-bit interval timer input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

Caution: For details on the register setup procedures, refer to RL78/G11 User's Manual: Hardware.

Setting count clock for 12-bit interval timer

- Timer clock select register 3 (TPS3)
  Select the count clock for the 12-bit interval timer.

Symbol：TPS3

7	6	5	4	3	2	1	0
0	0	0	0	0	TPS302	TPS301	TPS300
0	0	x	0	0	**0**	**0**	**0**

TPS302	TPS301	TPS300		Selection of count clock				
				f_{CLK}=2MHz	f_{CLK}=5MHz	f_{CLK}=10MHz	f_{CLK}=20MHz	f_{CLK}=24MHz
0	**0**	**0**	**fIL**	**15kHz**				
0	0	1	fCLK	2MHz	5MHz	10MHz	20MHz	24MHz
0	1	0	fCLK/2	1MHz	2.5MHz	5MHz	10MHz	12MHz
0	1	1	$fCLK/2^2$	500kHz	1.25NHz	2.5MHz	5MHz	6MHz
1	0	0	$fCLK/2^3$	250kHz	625kHz	1.25NHz	2.5MHz	3MHz
1	0	1	$fCLK/2^4$	125kHz	313kHz	625kHz	1.25NHz	1.5MHz
1	1	0	$fCLK/2^5$	62.5kHz	156kHz	313kHz	625kHz	750kHz
Other than the above			Setting prohibited					

Caution: For details on the register setup procedures, refer to RL78/G11 User's Manual: Hardware.

5.7.11 A/D Converter Setup

Figure 5.12 shows the flowchart for setting up the A/D converter.

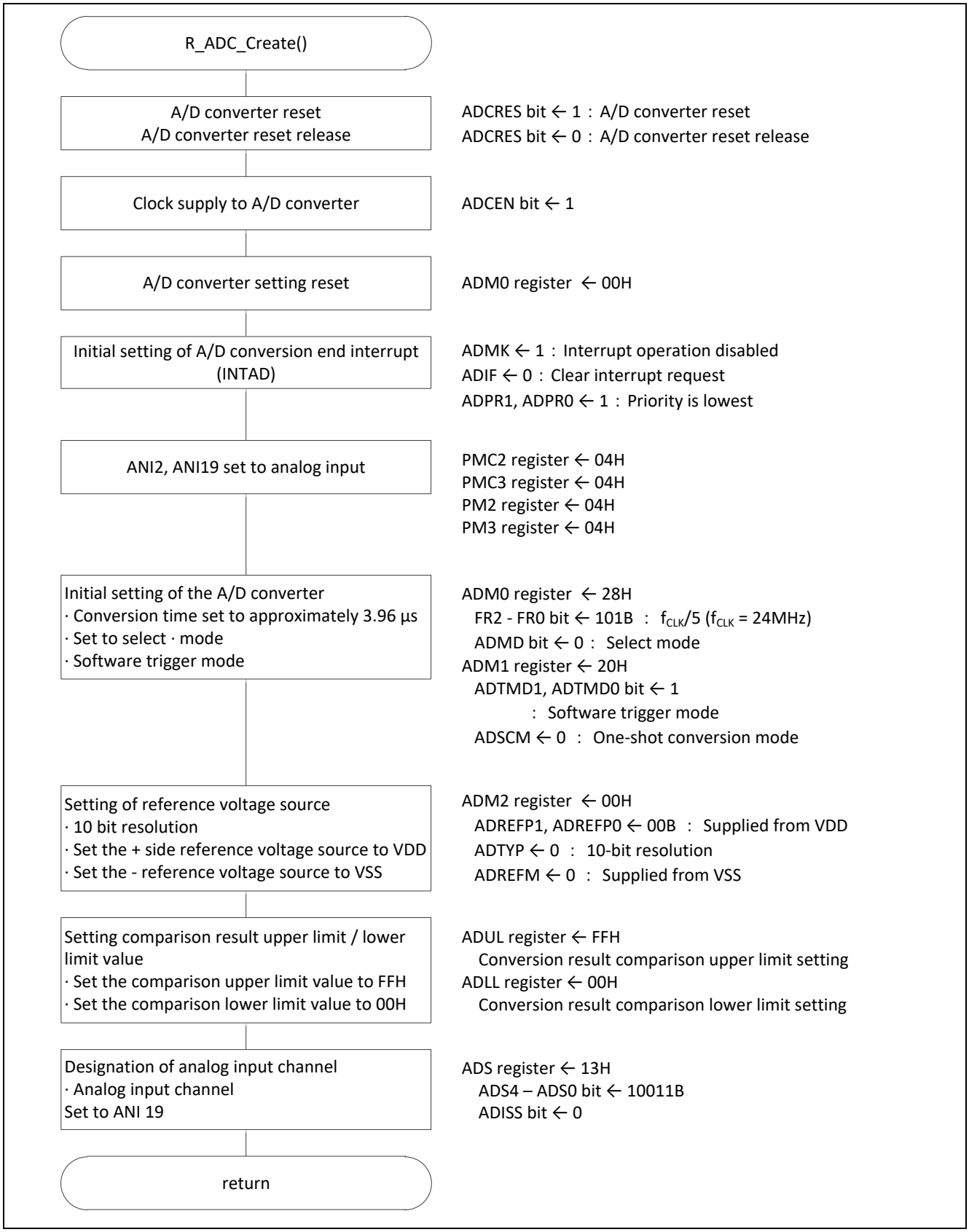

Figure 5.12 A/D Converter Setup

Starting clock supply to A/D converter

- Peripheral enable register 0 (PER0)
  Start supplying clock to the A/D converter.

Symbol：PER0

7	6	5	4	3	2	1	0
0	ICA1EN	ADCEN	IICA0EN	0	SAU0EN	0	TAU0EN
0	x	**1**	x	0	x	0	x

Bit 5

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

Setting A/D conversion time and operation mode

- A/D converter mode register 0 (ADM0)
  Control A/D conversion operation.
  Specify the A/D conversion channel selection mode.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
x	**0**	**0**	**0**	**1**	**0**	**0**	x

Bit 6

ADMD	Specification of the A/D conversion channel selection mode
0	**Select mode**
1	Scan mode

Caution: For details on the register setup procedures, refer to RL78/G11 User's Manual: Hardware.

Symbol：ADM0

7	6	5	4	3	2	1	0
ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
x	**0**	**0**	**0**	**1**	**0**	**0**	x

Bits 5 to 1

A/D Converter Mode Register 0 (ADM0)					Mode	Conversion Clock (f_{AD})	Number of Conversion Clock	Conversion Time	Conversion Time at 10-Bit Resolution				
FR2	FR1	FR0	LV1	LV2					f_{CLK}= 1MHz	f_{CLK}= 4MHz	f_{CLK}= 8MHz	f_{CLK}= 16MHz	f_{CLK}= 24MHz
0	0	0	**0**	**0**	**Normal 1**	**f_{CLK}/64**	**19 f_{AD} (number of sampling clock: 7 f_{AD})**	1216/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	84µs	50.667µs
0	**0**	**1**				**f_{CLK}/32**		608/f_{CLK}			76µs	42µs	25.333µs
0	1	0				f_{CLK}/16		304/f_{CLK}		76µs	38µs	19µs	12.667µs
0	**1**	**1**				**f_{CLK}/8**		**152/f_{CLK}**		38µs	19µs	9.5µs	**6.333µs**
1	0	0				f_{CLK}/6		114/f_{CLK}		28.5	14.25µs	7.125µs	4.75µs
1	0	1				f_{CLK}/5		95/f_{CLK}	95µs	23.75µs	11.875µs	5.938µs	3.958µs
1	1	0				f_{CLK}/4		76/f_{CLK}	76µs	19µs	9.5µs	4.75µs	3.167µs
1	1	1				f_{CLK}/2		38/f_{CLK}	38µs	9.5µs	4.75µs	2.375µs	Setting prohibited
0	0	0	1	1	Normal 2	f_{CLK}/64	17 f_{AD} (number of sampling clock: 5 f_{AD})	1088/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	68µs	45.333µs
0	0	1				f_{CLK}/32		544/f_{CLK}			68µs	34µs	22.667µs
0	1	0				f_{CLK}/16		272/f_{CLK}		68µs	34µs	17µs	11.333µs
0	1	1				f_{CLK}/8		136/f_{CLK}		34µs	17µs	8.5µs	5.667µs
1	0	0				f_{CLK}/6		102/f_{CLK}		25.5µs	12.75µs	6.375µs	4.25µs
1	0	1				f_{CLK}/5		85/f_{CLK}	85µs	21,25µs	10.625µs	5.3125µs	3.542µs
1	1	0				f_{CLK}/4		68/f_{CLK}	68µs	17µs	8.5µs	4.25µs	2.833µs
1	1	1				f_{CLK}/2		34/f_{CLK}	34µs	8.5µs	4.25µs	2.125µs	Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G11 User's Manual: Hardware.

Setting A/D conversion trigger mode

- A/D converter mode register 1 (ADM1)
  Select A/D conversion trigger mode.
  Set the A/D conversion mode.
  Select the hardware trigger signal.

Symbol: ADM1

7	6	5	4	3	2	1	0
ADTMD1	ADTMD0	ADSCM	0	0	0	ADTRS1	ADTRS0
0	**0**	**1**	0	0	0	**0**	**0**

Bits 7 and 6

ADTMD1	ADTMD0	Selection of the A/D conversion trigger mode
0	**0**	**Software trigger mode**
1	0	Hardware trigger no-wait mode
1	1	Hardware trigger wait mode

Bit 5

ADSCM	Specification of the A/D conversion mode
0	Sequential conversion mode
1	**One-shot conversion mode**

Bits 1 and 0

ADTRS1	ADTRS0	Selection of the hardware trigger signal
0	**0**	**End of timer channel 1 count or capture interrupt signal (INTTM01)**
0	1	Event signal selected by ELC
1	0	Setting prohibited
1	1	12-bit interval timer interrupt signal (INTIT)

Caution: For details on the register setup procedures, refer to RL78/G11 User's Manual: Hardware.

Setting reference voltage source

- A/D converter mode register 2 (ADM2)
  Select the + side reference voltage source of the A/D converter.
  Select the – side reference voltage source of the A/D converter.
  Check the upper limit and lower limit conversion result values.
  Specify the SNOOZE mode.
  Select the A/D conversion resolution.

Symbol: ADM2

7	6	5	4	3	2	1	0
ADREFP1	ADREFP0	ADREFM	0	ADRCK	AWC	0	ADTYP
0	**0**	**0**	0	**0**	**0**	0	**0**

Bits 7 and 6

ADREFP1	ADREFP0	Selection of the + side reference voltage source of the A/D converter
0	**0**	**Supplied from V_{DD}**
0	1	Supplied from P20/AV_{REFP}/ANI0
1	0	Supplied from the internal reference voltage (1.45 V)
1	1	Setting prohibited

Bit 5

ADREFM	Selection of the - side reference voltage of the A/D converter
0	**Supplied from V_{SS}**
1	Supplied from P21/AV_{REFM}/ANI1

Bit 3

ADRCK	Checking the upper limit and lower limit conversion result values
0	**The interrupt signal (INTAD) is output when the ADLL register ≤ the ADCR register ≤ the ADUL register(AREA1).**
1	The interrupt signal (INTAD) is output when the ADCR register < the ADLL register (AREA2) or the ADUL register < the ADCR register (AREA3).

Bit 2

AWC	Specification of the SNOOZE mode
0	**Do not use the SNOOZE mode function.**
1	Use the SNOOZE mode function.

Bit 0

ADTYP	Selection of the A/D conversion resolution
0	**10-bit resolution**
1	8-bit resolution

Caution: For details on the register setup procedures, refer to RL78/G11 User's Manual: Hardware.

Setting upper-limit and lower-limit values for checking A/D conversion results

- Conversion result comparison upper limit setting register (ADUL)
- Conversion result comparison lower limit setting register (ADLL)

Set upper-limit and lower-limit values for conversion result comparison.

Symbol: ADUL

7	6	5	4	3	2	1	0
ADUL7	ADUL6	ADUL5	ADUL4	ADUL3	ADUL2	ADUL1	ADUL0
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Symbol: ADLL

7	6	5	4	3	2	1	0
ADLL7	ADLL6	ADLL5	ADLL4	ADLL3	ADLL2	ADLL1	ADLL0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Setting input channels

- Analog input channel specification register (ADS)
  Specify the input channel of the analog voltage to be A/D converted.

Symbol: ADS

7	6	5	4	3	2	1	0
ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0
0	0	0	**1**	**0**	**0**	**1**	**1**

Bits 7, 4 to 0

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog input channel	Input source
0	0	0	0	0	0	ANI0	P20/ANI0 pinAV$_{REFP}$ pin
0	0	0	0	0	1	ANI1	P21/ANI1 pin/AV$_{REFM}$ pin
0	0	0	0	1	0	ANI2	P22/ANI2 pin
0	0	0	0	1	1	ANI3	P23/ANI3 pin
0	1	0	0	0	0	ANI16	P01/ANI16 pin
0	1	0	0	0	1	ANI17	P00/ANI17 pin
0	1	0	0	1	0	ANI18	P33/ANI18 pin
0	**1**	**0**	**0**	**1**	**1**	**ANI19**	**P32/ANI19 pin**
0	1	0	1	0	0	ANI20	P31/ANI20 pin
0	1	0	1	0	1	ANI21	P30/ANI21 pin
0	1	0	1	1	0	ANI22	P56/ANI22 pin
0	1	0	1	1	1	—	PGAOUT (PGA output)
1	0	0	0	0	0	—	Temperature sensor output voltage
1	0	0	0	0	1	—	Internal reference voltage (1.45 V)
Other than the above						Setting prohibited	

Caution: For details on the register setup procedures, refer to RL78/G11 User's Manual: Hardware.

Setting A/D conversion end interrupt

- Interrupt request flag register (IF1H)
  Clear the relevant interrupt request flag.
- Interrupt mask flag registers (MK1H)
  Disable the relevant interrupt.

Symbol: IF1H

7	6	5	4	3	2	1	0
PIF11	PIF10	PIF9	PIF8	PIF7	KRIF	TMKAIF	ADIF
x	x	x	x	x	x	x	**0**

Bit 0

ADIF	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK1H

7	6	5	4	3	2	1	0
PMK11	PMK10	PMK9	PMK8	PMK7	KRMK	TMKAMK	ADMK
x	x	x	x	x	x	x	**1**

Bit 0

ADMK	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Caution: For details on the register setup procedures, refer to RL78/G11 User's Manual: Hardware.

5.7.12 Main Function

Figure 5.13 shows the flowchart for the main function.

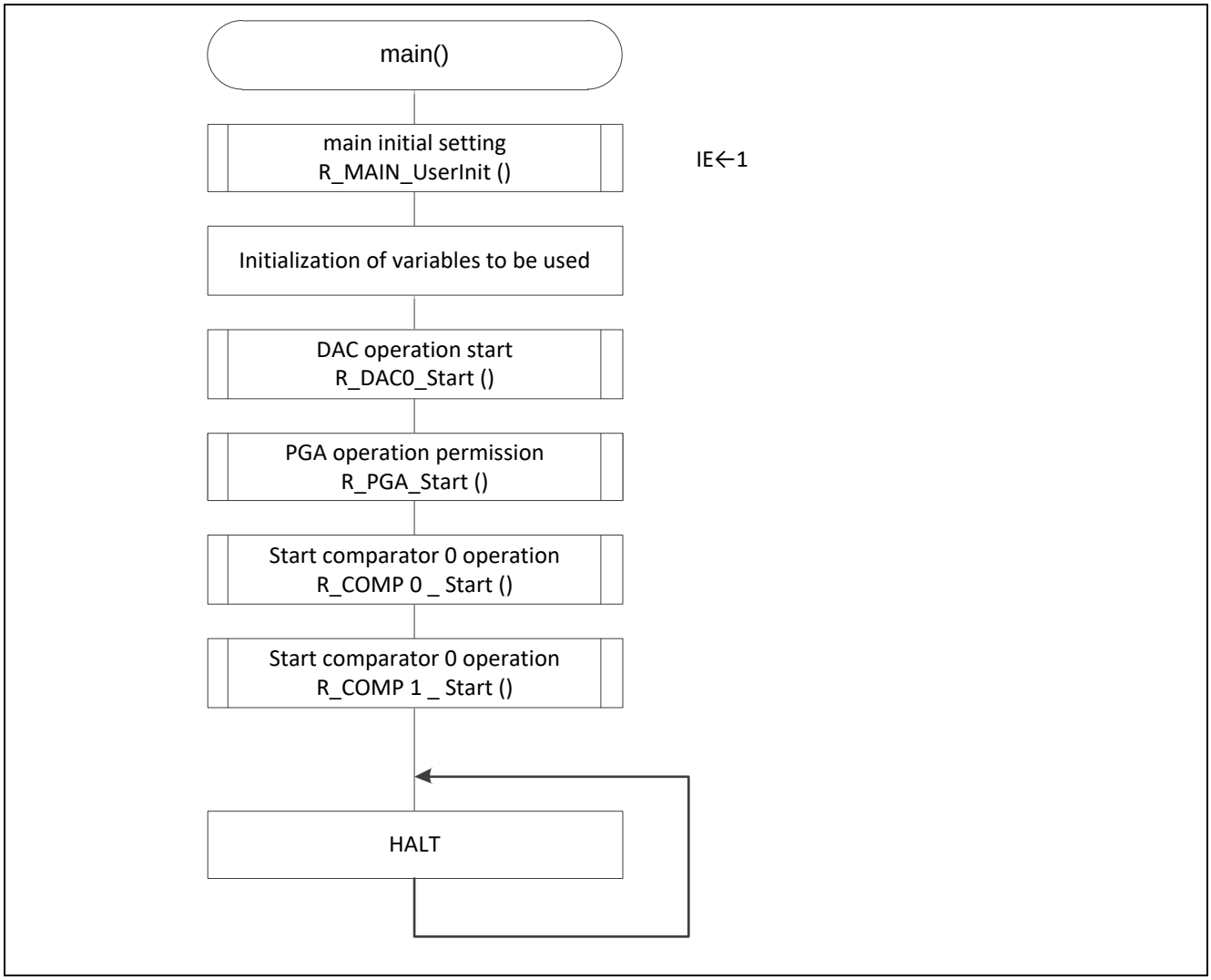

Figure 5.13 Main Function

5.7.13 Initial Setting for “main”

Figure 5.14 shows the flowchart of the initial setting for “main”.

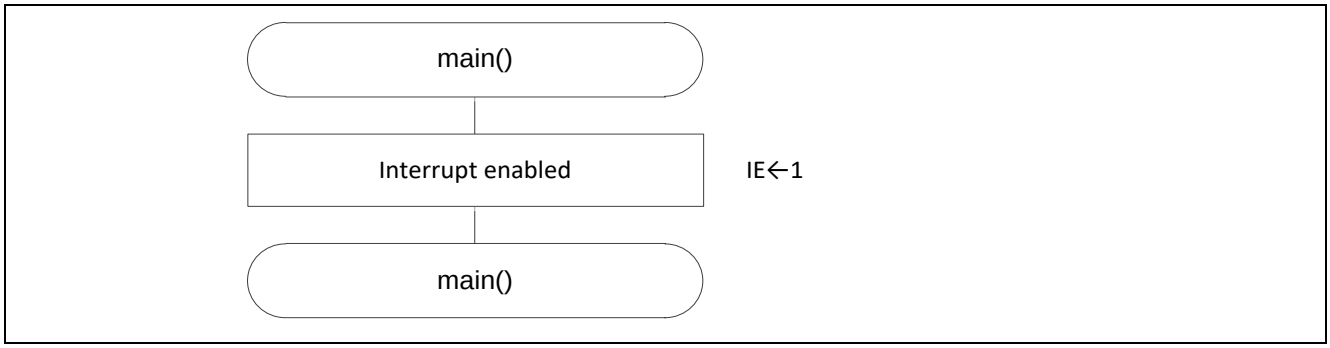

Figure 5.14 Initial Setting for “main”

5.7.14 Starting D/A Converter Operation

Figure 5.15 shows the flowchart for starting D/A converter operation.

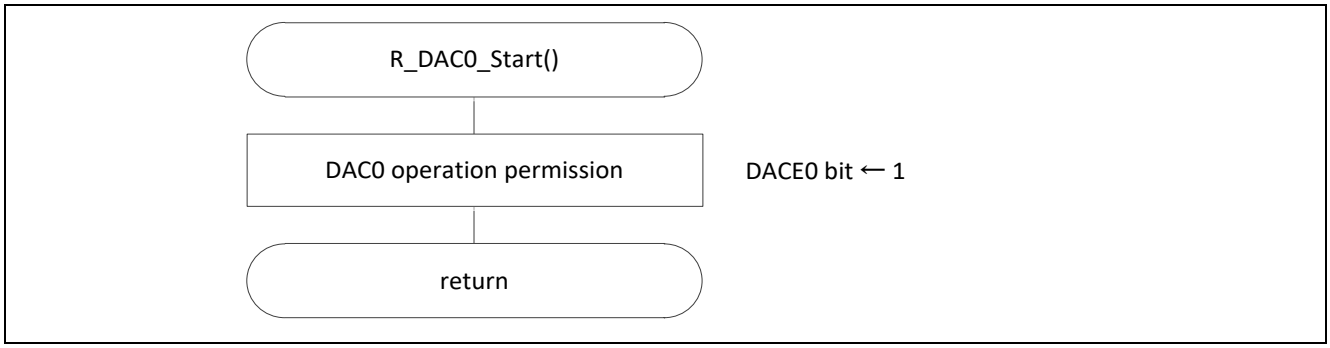

Figure 5.15 Starting D/A Converter Operation

5.7.15 Starting PGA Operation

Figure 5.16 shows the flowchart for starting PGA operation.

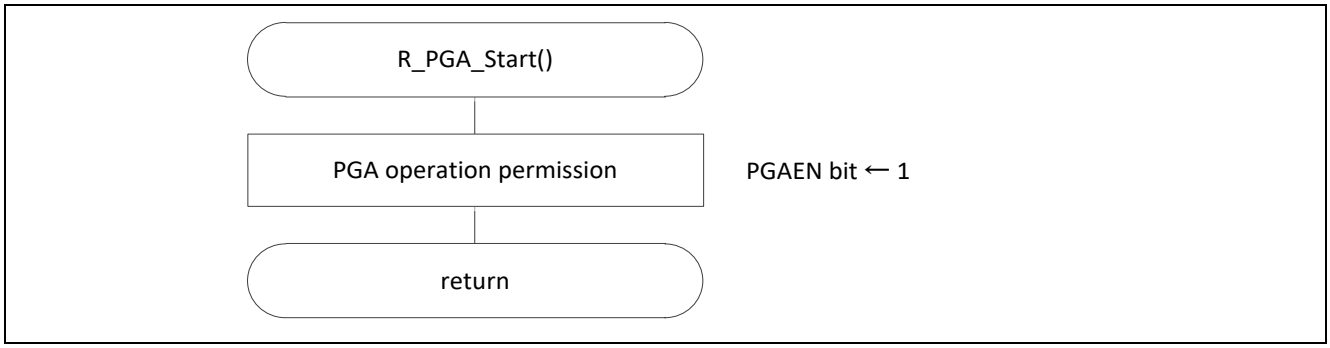

Figure 5.16 Starting PGA Operation

5.7.16 Starting Comparator 0 Operation

Figure 5.17 shows the flowchart for starting comparator 0 operation.

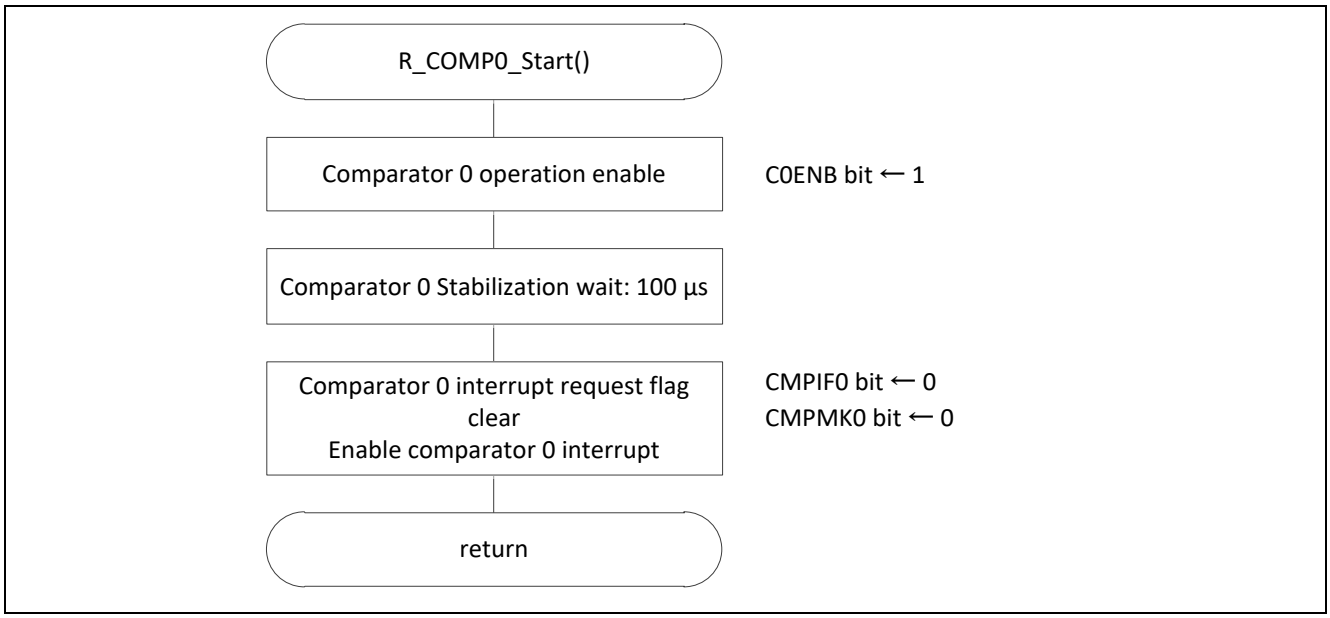

Figure 5.17 Starting Comparator 0 Operation

5.7.17 Starting Comparator 1 Operation

Figure 5.18 shows the flowchart for starting comparator 1 operation.

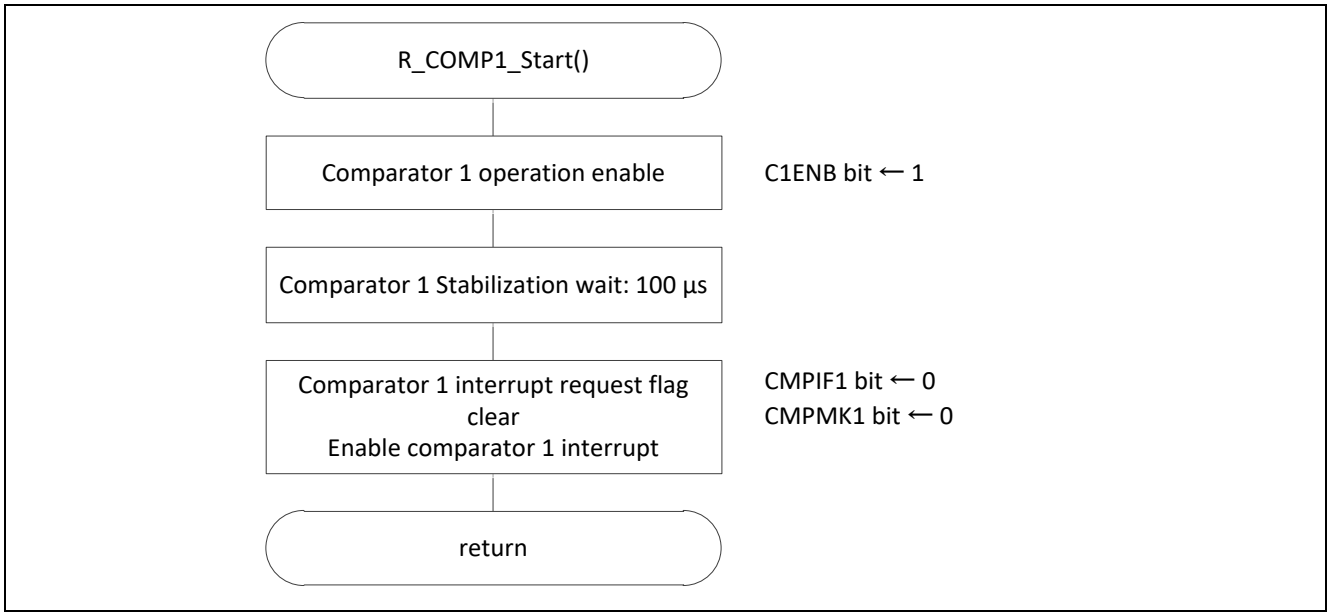

Figure 5.18 Starting Comparator 1 Operation

5.7.18 Comparator 0 Interrupt Operation

Figure 5.19 shows the flowchart of comparator 0 interrupt operation.

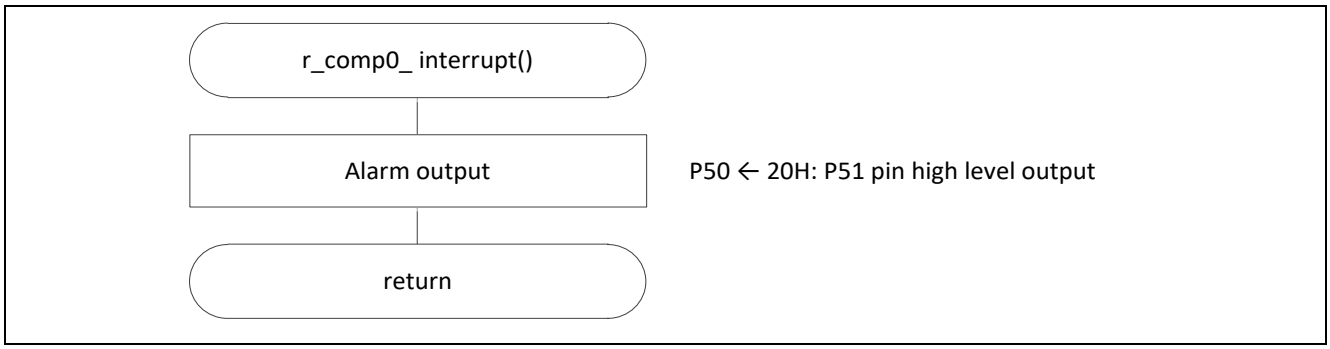

Figure 5.19 Comparator 0 Interrupt Operation

5.7.19 Comparator 1 Interrupt Operation

Figure 5.20 shows the flowchart of comparator 1 interrupt operation.

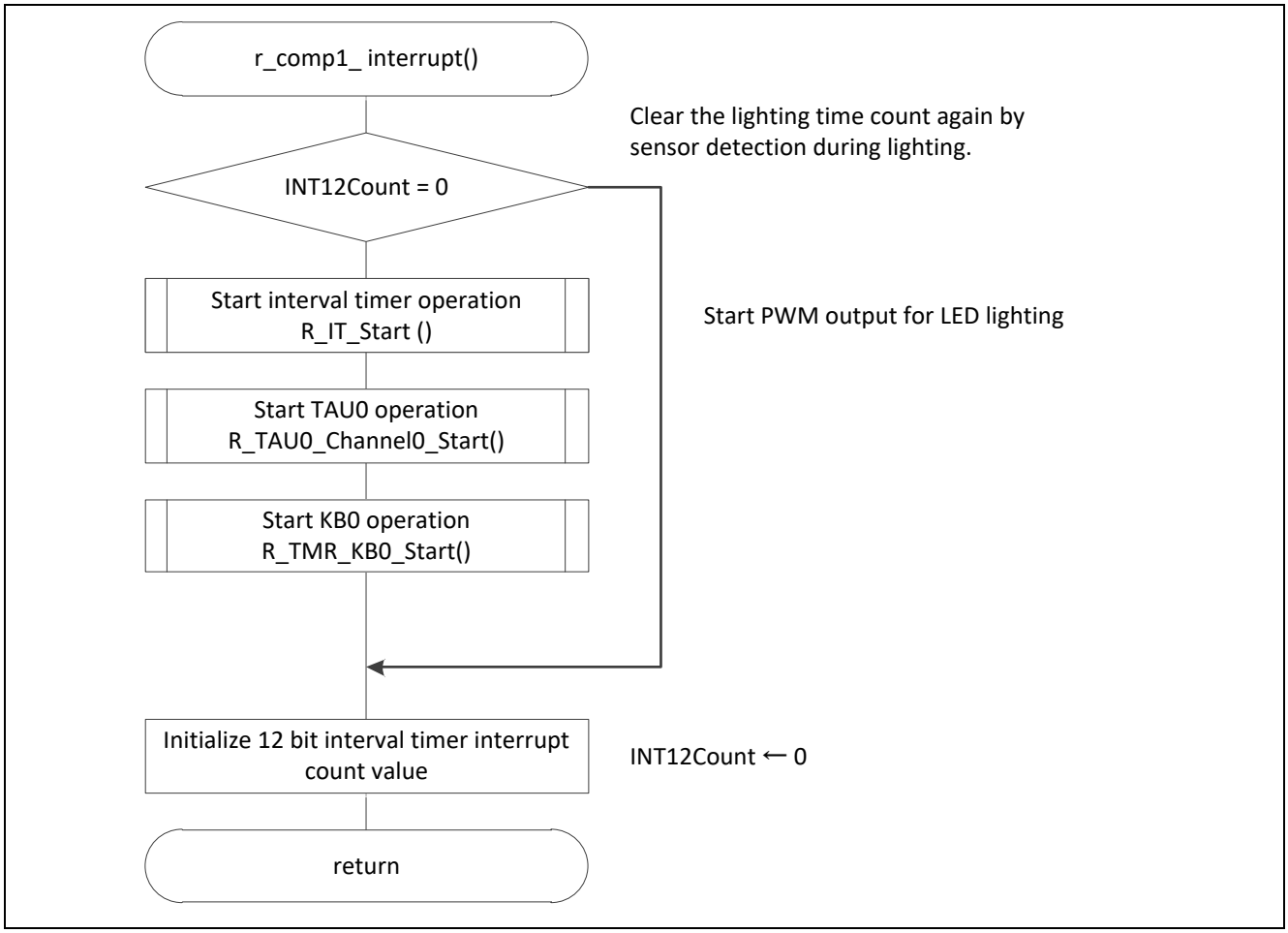

Figure 5.20 Comparator 1 Interrupt Operation

5.7.20 Starting Interval Timer Operation

Figure 5.21 shows the flowchart for starting interval timer operation.

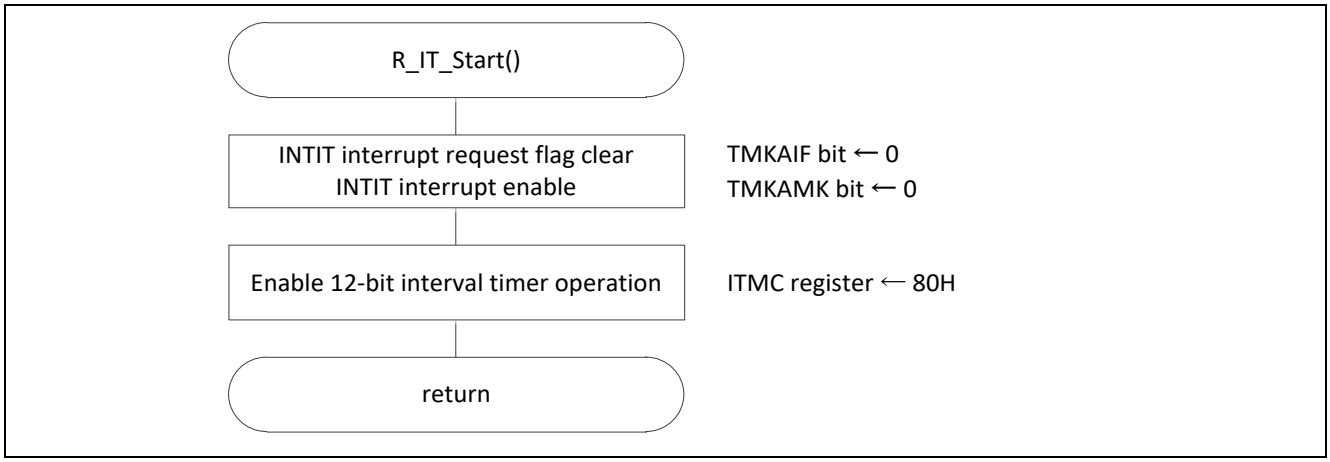

Figure 5.21 Starting Interval Timer Operation

5.7.21 Starting Timer Array Unit Operation

Figure 5.22 shows the flowchart for starting timer array unit operation.

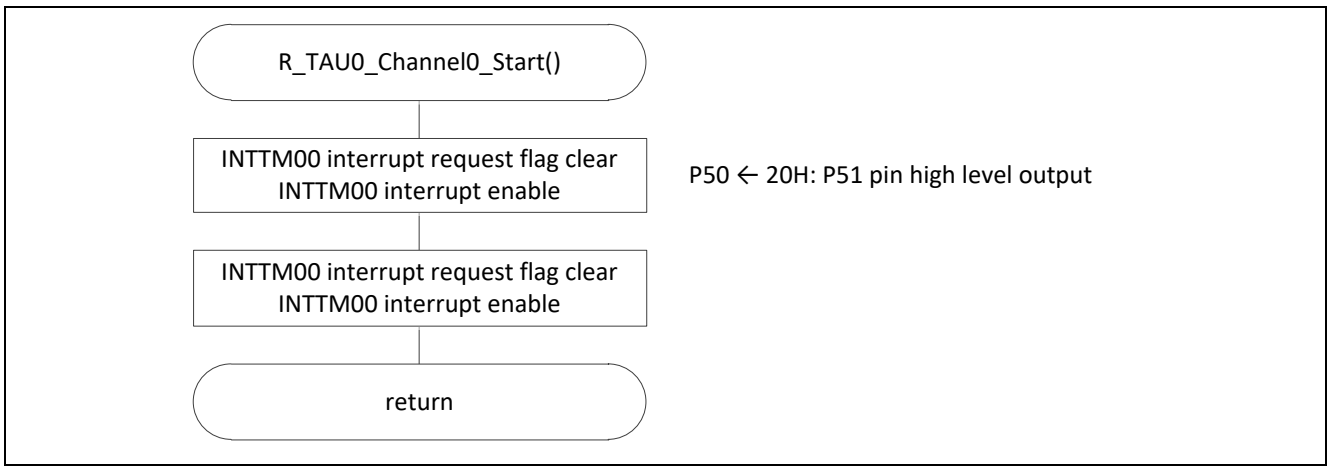

Figure 5.22 Starting Timer Array Unit Operation

5.7.22 Starting Timer KB Operation

Figure 5.23 shows the flowchart for starting timer KB operation.

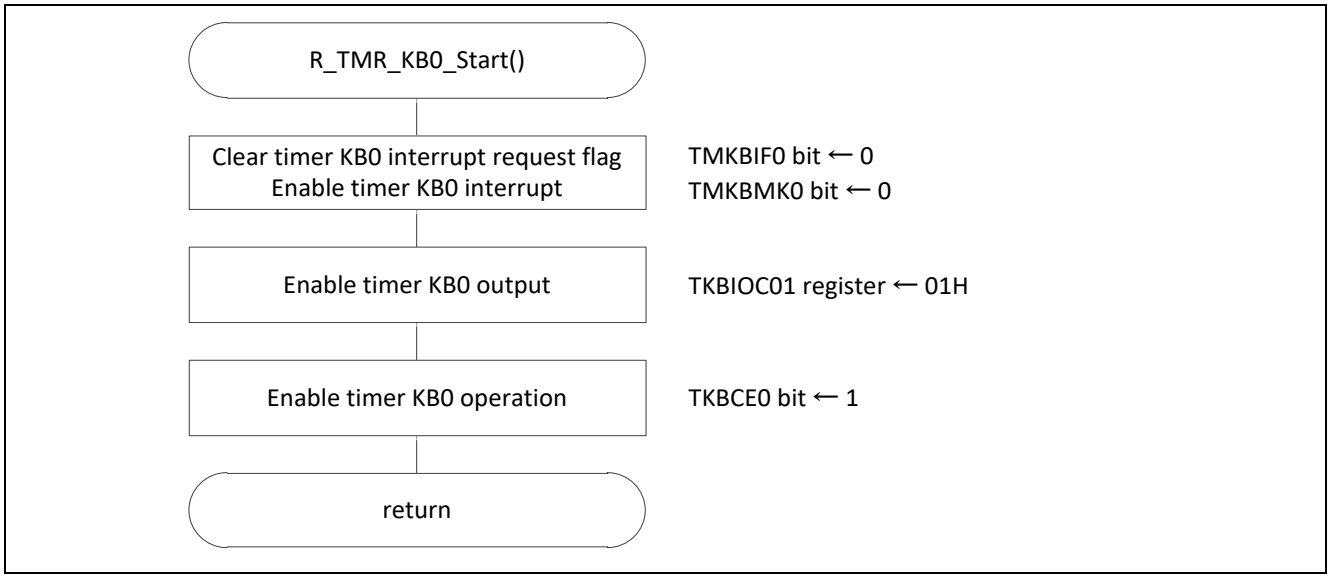

Figure 5.23 Starting Timer KB0 Operation

5.7.23 Interval Timer Interrupt Operation

Figure 5.24 shows the flowchart of interval timer interrupt operation.

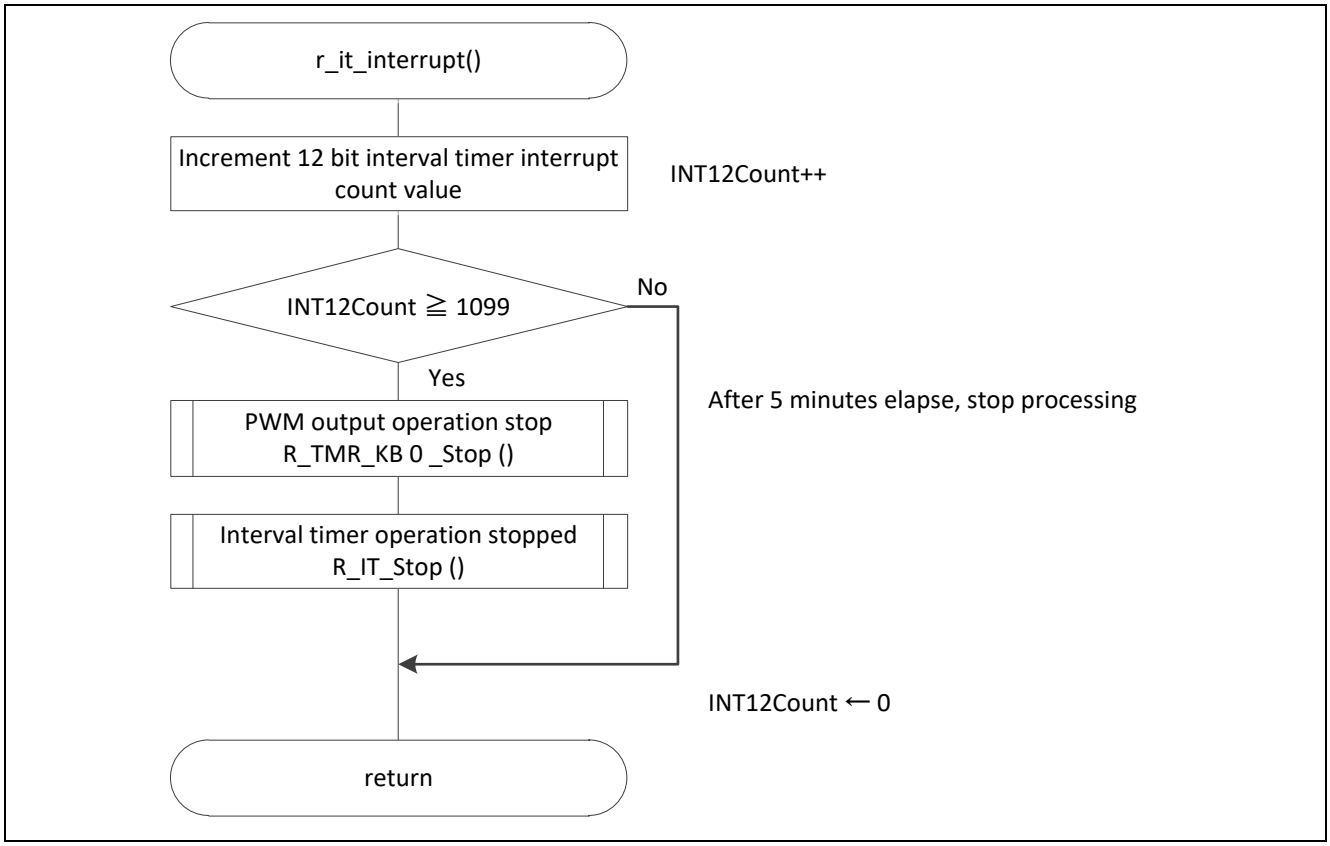

Figure 5.24 Starting Interval Timer Operation

5.7.24 Stopping Timer KB Operation

Figure 5.25 shows the flowchart for stopping timer KB operation.

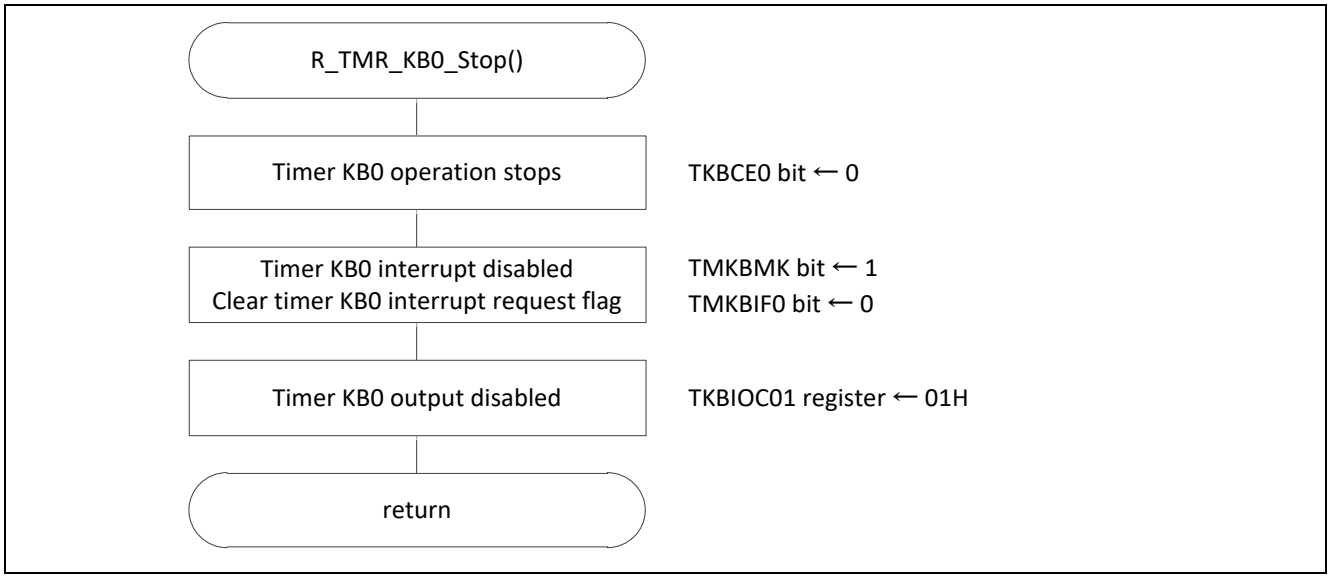

Figure 5.25 Stopping Timer KB0 Operation

5.7.25 Stopping Interval Timer Operation

Figure 5.26 shows the flowchart for stopping interval timer operation.

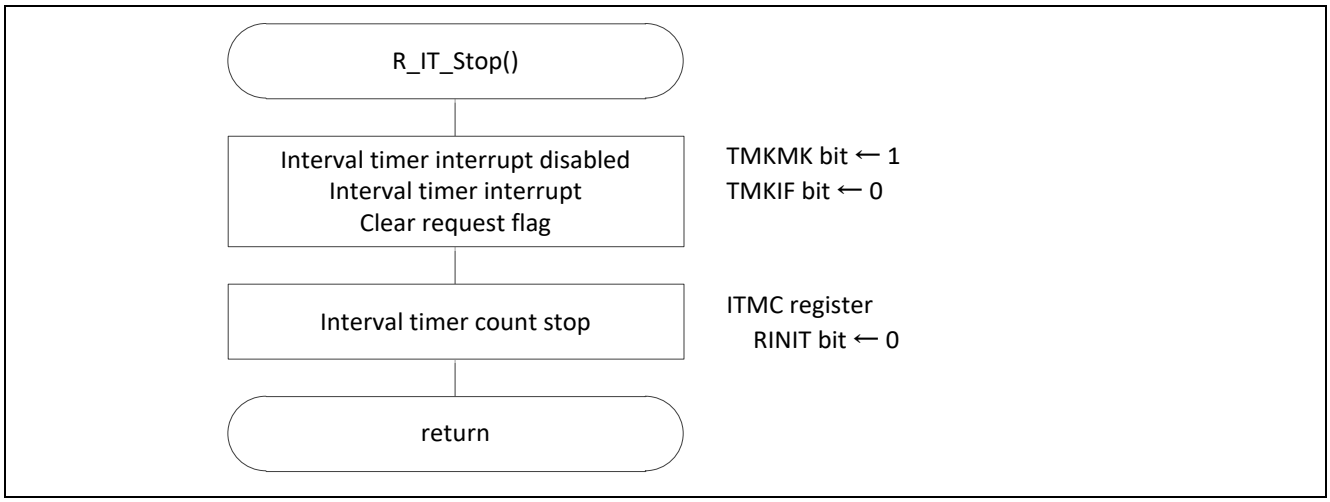

Figure 5.26 Stopping Interval Timer Operation

5.7.26 Timer Array Unit Interrupt Operation

Figure 5.27 shows the flowchart of timer array unit interrupt operation.

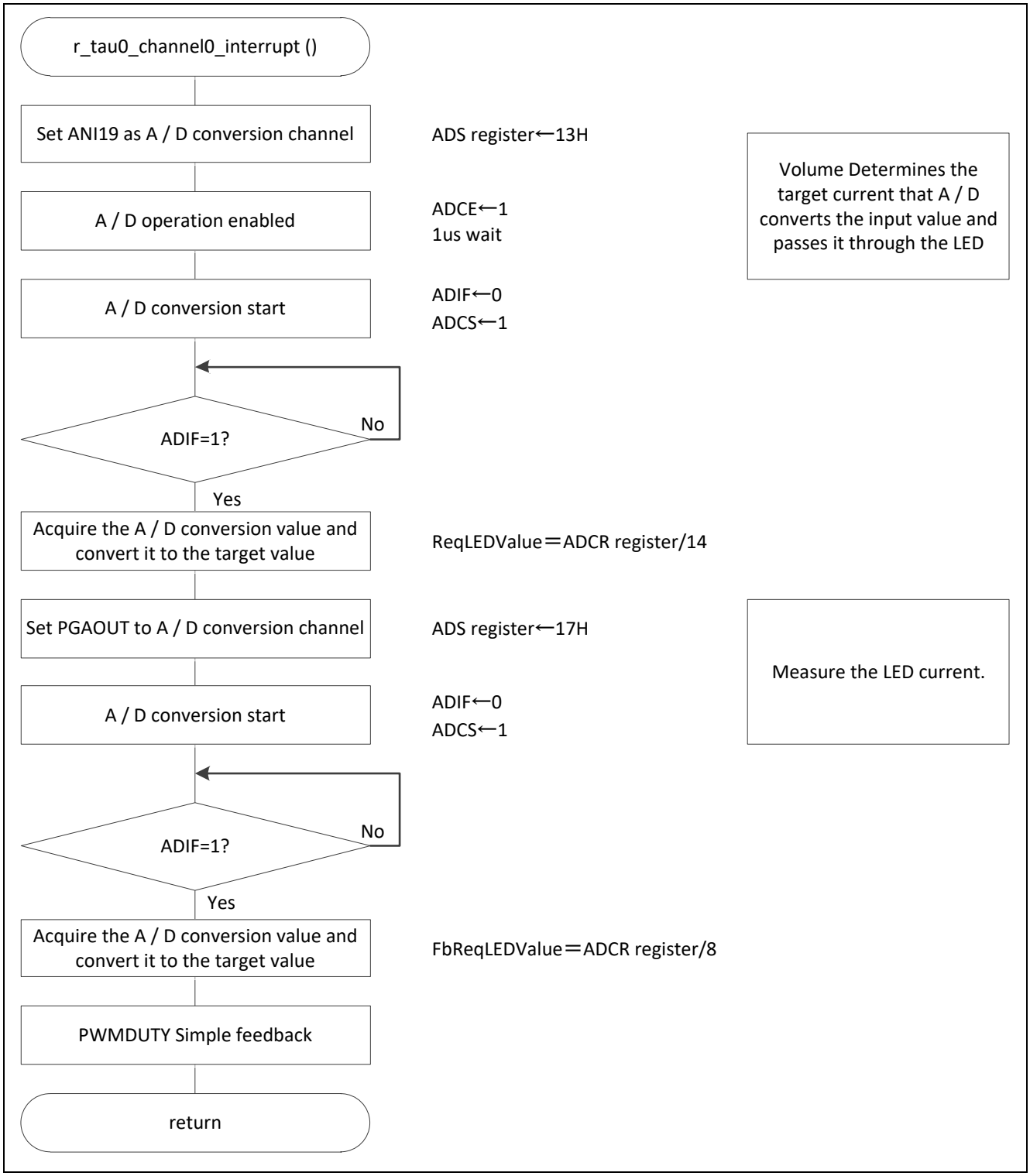

Figure 5.27 Timer Array Unit Interrupt Operation

6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

RL78/G11 User's Manual: Hardware（R01UH0637E）

RL78 Family User's Manual: Software（R01US0015E）

LED Control Using RL78/I1A (R01AN1087E)

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website
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Inquiries
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REVISION HISTORY	RL78/G11 LED Control by Using 16-Bit Timer KB0 CC-RL

Rev.	Date	Description	
		Page	Summary
1.00	Apr. 27, 2018	-	First edition issued
2.00	Jan.31, 2019	19, 20, 36	Fixed typo.

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   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
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