RAA604S00

Guidelines for two-layer board for RF part

R01AN4426EJ0200
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Introduction

This document states guidelines to be observed when designing RF board with two-layer substrate.

Target Device

RAA604S00

Note: The contents of this document are provided as an example for reference and do not guarantee the signal quality in systems. When implementing this example into an existing system, thoroughly evaluate the product in the overall system and apply the contents of this document at your own responsibility.

Contents

1. Overview

This document uses the pin names of the RAA604S00. Table 1 briefly describes the pins used in the RAA604S00.

Table 1 Description of the RAA604S00 Pins

Pin Number	Pin Name	I/O	Function
1	STANDBY	Input	Power down control input of the transceiver
2	OSCDRVSEL	Input	This signal is for switching the driving ability of the buffer for the 48-MHz crystal oscillator.
3	SIN	Input	Serial input
4	SOUT	Output	Serial output
5	SCLK	Input	Serial input/output clock
6	SEN	Input	Serial enable
7	GPIO0	Input/output	Transceiver I/O port 0 or CLKOUT
8	GPIO1/ANTSELOUT0	Input/output	Transceiver I/O port 1 or ANTSELOUT0
9	INTOUT	Output	Transceiver interrupt output
10	GPIO2/ANTSELOUT1	Input/output	Transceiver I/O port 2 or ANTSELOUT1
11	GPIO3	Input/output	Transceiver I/O port 3
12	GPIO4/ANTSW	Input/output	Transceiver I/O port 4 or ANTSW
13	RFRESETB	Input	Reset
14	DON	Input	DC-DC converter enable
15	VREGO2	—	Stabilizing capacitor connection for VCO (1.1 V)
16	VREGO3	—	Power supply stabilizing capacitor connection for PLL (1.1 V)
17	MODE2	Input	Mode switch 2
18	MODE1	Input	Mode switch 1
19	RFIN	—	Transceiver ground
20	RFIP	Input	RF input
21	AGNDRF1	—	Transceiver ground
22	RFOUT	Output	RF output
23	AGNDRF2	—	Transceiver ground
24	REXT	—	External reference resistor connecting pin
25	VREGO1	—	Power supply stabilizing capacitor connection for the RF section (1.1 to 1.25 V)
26	XIN	Input	48-MHz crystal resonator input
27	XOUT/REFCLKIN	Input/output	48-MHz crystal resonator output or external clock input
28	VCCRF	—	3-V power supply input (1.8 to 3.6 V)
29	REGIN	—	Power supply input for the analog section (1.4 to 1.6 V), for external connection with DDCOUT
30	VSSDDC	—	DCDC converter ground
31	DDCOUT	—	DCDC converter output (1.4 to 1.6 V), for external connection with REGIN
32	VCCDDC	—	DCDC converter power supply (1.8 to 3.6 V)
Reverse side	DIEGND	—	Ground

1.1 Related Documents

The following document is related to this application note. Also refer to this document when using this application note.

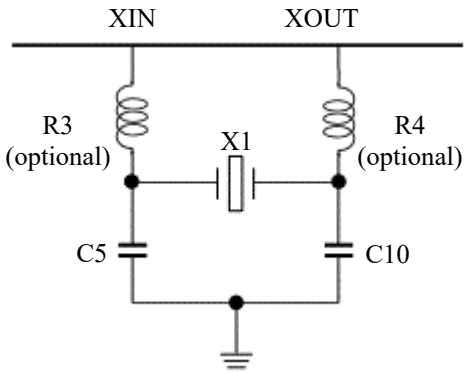
- RAA604S00 User's Manual: Hardware (R01UH0567EJ)

2. Oscillator

Note the following points for design in relation to the oscillator.

- Place the load capacitor close to the crystal resonator electrode.
- Separate the signal lines for the crystal resonator's pins 26 (XIN) and 27 (XOUT) from those for pin 22 (RFOUT) by at least 4.5 mm because a narrower separation may lead to an unacceptable level of intermodulation interference.
- We recommend not placing signal lines other than pin 26 (XIN) and pin 27 (XOUT) in the vicinity of the crystal resonator.
- Separate the ground area for the crystal resonator and load capacitors C5 and C10 from the other ground areas on the surface layer of the board.
- Connect the wiring between pins 26 (XIN) and 27 (XOUT) on the back of the board through the via holes.
- Before using a crystal resonator, contact the resonator manufacturer to determine its circuit constants.
- When using a neighboring channel of an integral multiple (864 MHz, 912 MHz) of the crystal frequency of 48 MHz, or when if the distance between pin46(XIN) and pin 47 (XOUT) to pin 43 (RFOUT) can not be increased, insert the inductor arbitrarily into R3 and R4 according to the clock spurious condition.

Figure 1 shows an example of how to connect a crystal resonator. Figure 2 shows an example of the layout pattern.



The constants of the load capacitors (C5 and C10) depend on the characteristics of the crystal resonator in use. Evaluate the oscillation characteristics of the crystal resonator to determine the constants.

Figure 1 Example of How to Connect a Crystal Resonator

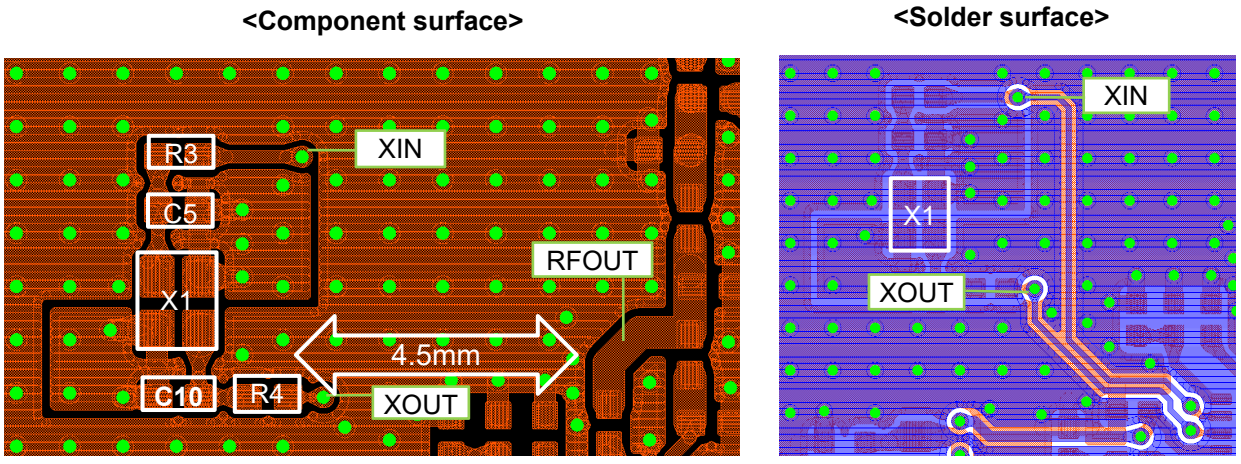


Figure 2 Example of Layout Pattern in the Vicinity of the Crystal Resonator

3. External Circuit for DC-DC Converter

Note the following points for design in relation to the feedback loop of the DC-DC converter.

- We recommend not placing signal lines in the vicinity of pins 29 (REGIN), 30 (VSSDDC), and 31 (DDCOUT).
- Keep the length of the wiring run between pins 29 (REGIN) and 31 (DDCOUT) as short as possible.
- Place C3 as close to pin 32 (VCCDDC) as is possible.
- C3 and C46 hold the positional relationship of this layout and arrange so that C46 does not get too close to C3.
- Place the board ground from Pin 50 (VSSDDC) in the loop of Pin 49 (REGIN) and Pin 51 (DDCOUT), and place one or more via.
- Insert the ferrite beads (FB1) arbitrarily according to the noise condition caused by the DC-DC converter.

Figure 3 shows an example of the feedback loop circuit of the DC-DC converter. Figure 4 shows an example of the layout pattern.

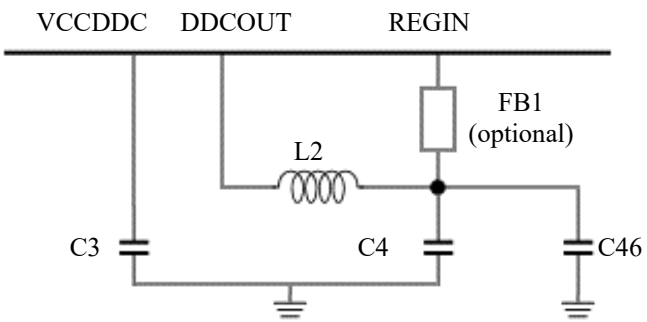


Figure 3 Example of the Feedback Loop Circuit of the DC-DC Converter

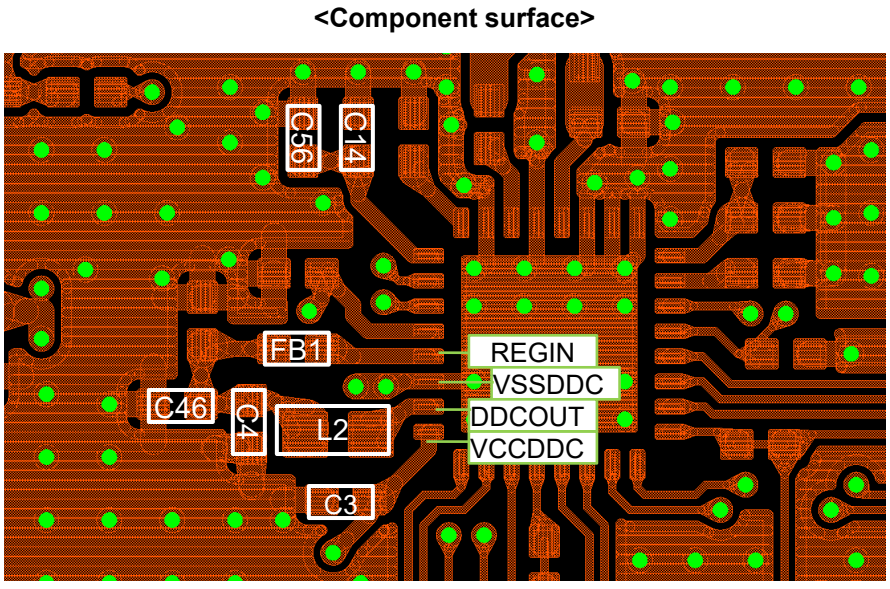


Figure 4 Example of the Layout Pattern of the Feedback Loop of the DC-DC Converter

4. RF Signal Lines

Note the following points for design in relation to the circuit in the vicinity of the RF signal lines.

- Design the RF signal lines as coplanar lines and also as having an impedance of 50 Ω.
- Place as many via holes around the coplanar lines as is possible. The areas around and between the coplanar lines should be solid stretches of ground with no signal connections.
- The ground for C16, C17, and C18 should be isolated from those for pins 26 (XIN) and 27 (XOUT), so C16, C17 and C18 should be connected to the same stretch of ground as pin 21 (AGNDRF1) or 19 (RFIN). The ground of C15 should be taken from pin 23 (AGNDRF2) side.
- Pin 21 (AGNDRF1) should be connected to the board ground between pins 20 (RFIP) and 22 (RFOUT).

Figure 5 shows an example of the layout pattern in the vicinity of the RF signal lines.

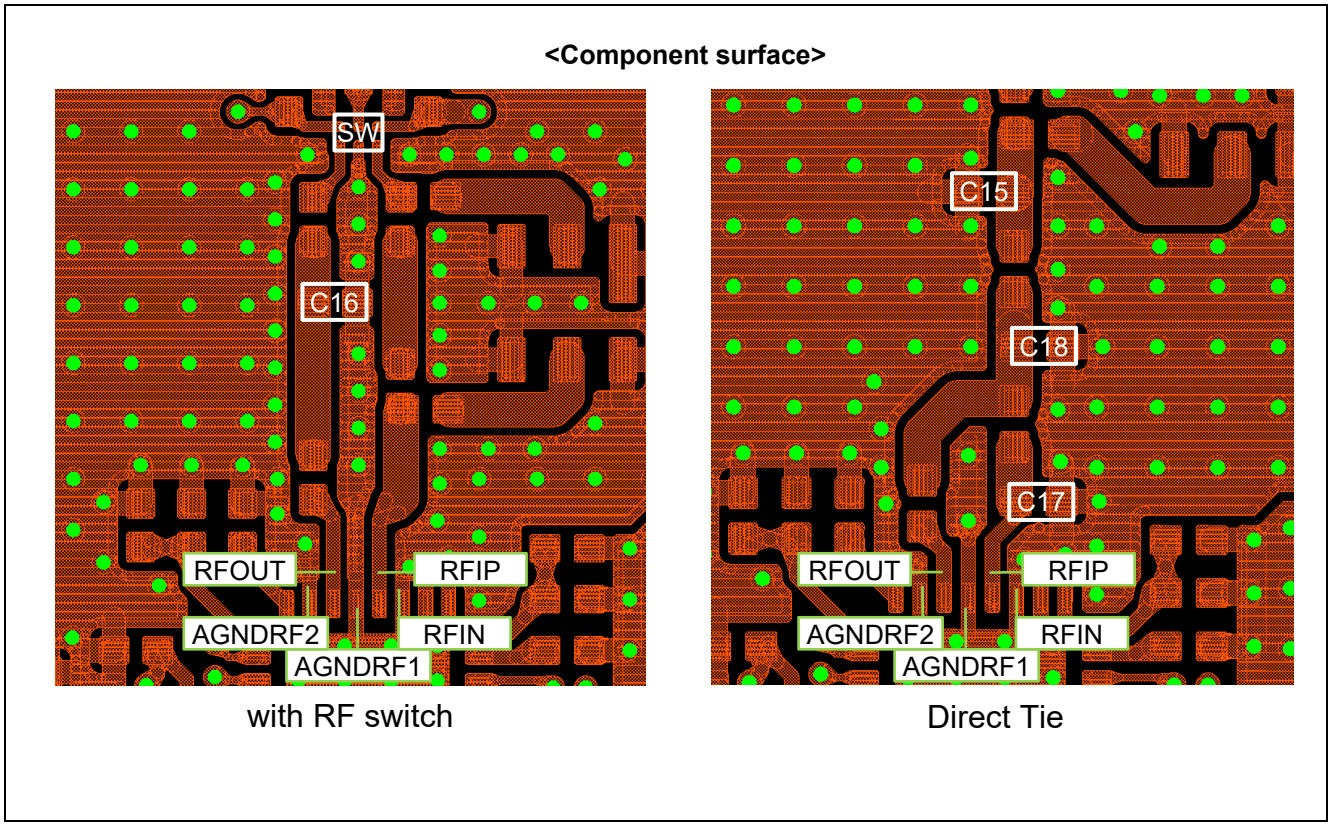


Figure 5 Example of the Layout Pattern in the Vicinity of the RF Signal Lines

5. Digital Signal Lines

Note the following points for design in relation to the circuit in the vicinity of the digital signal lines.

- We recommend not placing wiring for pins 3 (SIN), 4 (SOUT), 5 (SCLK), 6 (SEN), and 9 (INTOUT) under the IC, in the vicinity of the RF signal lines, or in the vicinity of pins 29 (REGIN), 30 (VSSDDC), 31 (DDCOUT), and 32 (VCCDDC).
- Keep the digital signal lines as short as possible to reduce digital noise. We recommend inserting series resistors as required. In that case must be placed R16, R18, and R19 on the MCU side and R17 and R20 on the RAA604S00 side.

Figure 6 shows an example of the layout pattern in the vicinity of the digital signal lines.

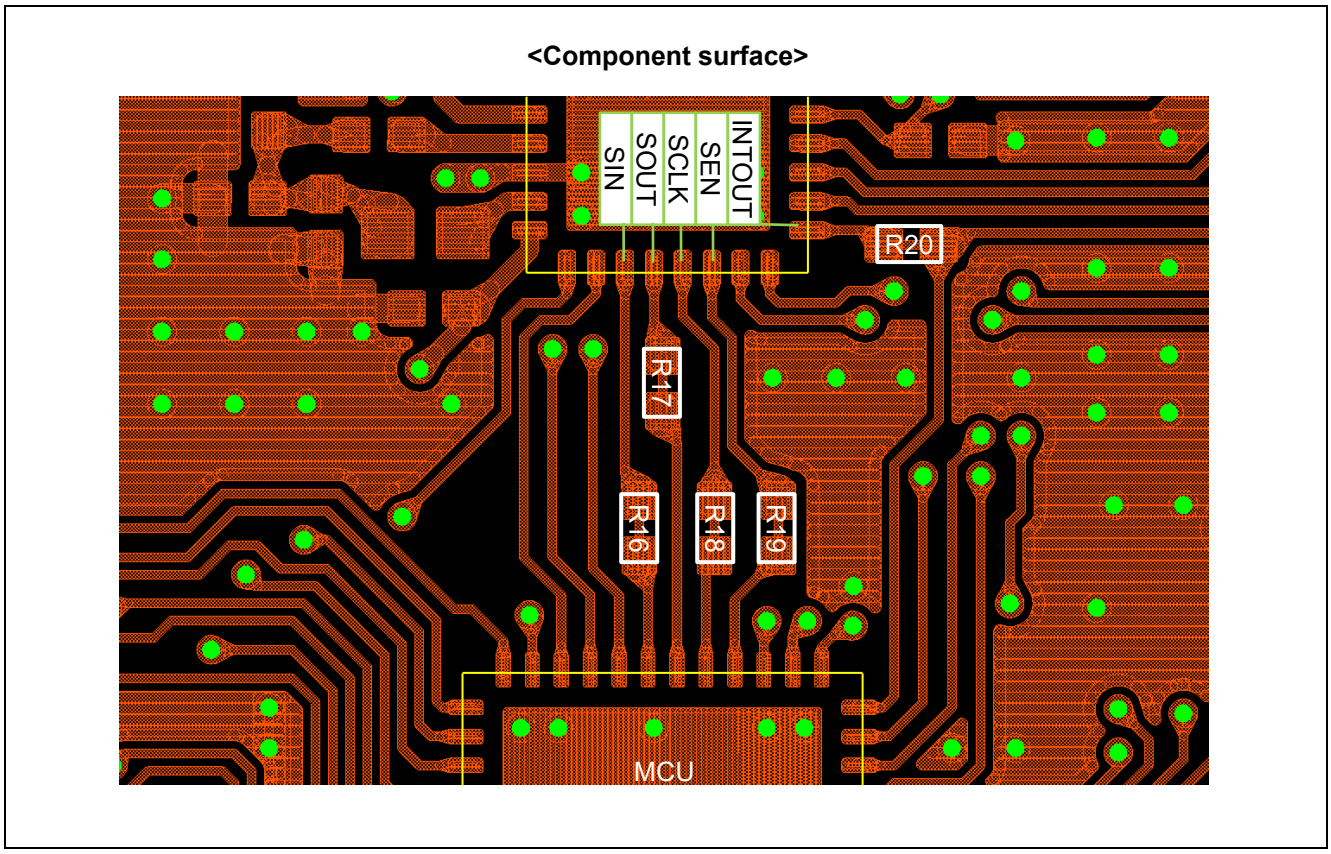


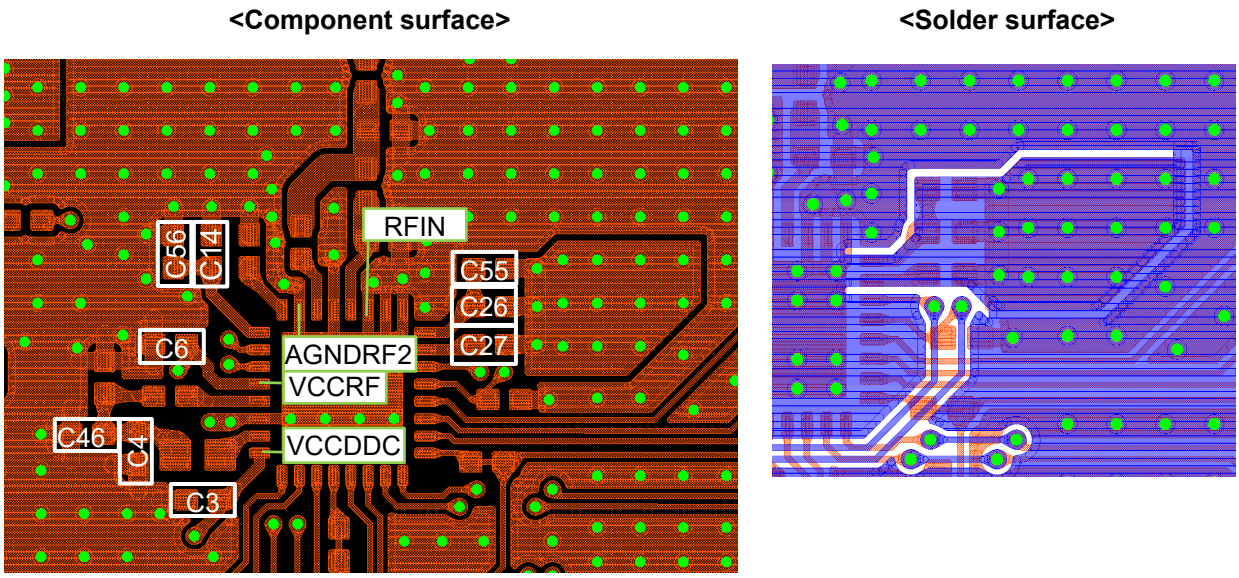
Figure 6 Example of the Layout Pattern in the Vicinity of the Digital Signal Lines

6. Power Supply

Note the following points for design in relation to the power supply circuit.

- Place the bypass capacitors on the surface layer of the board and as close as possible to the pins.
- Place the ground of C14, C56 as closely as possible to pin 23 (AGNDRF2).
- Separate the grounds for C26, C27, and C55 from the surface layer of the board and insert the slit from base of the pins on the back layer, to avoid interference from the signal on pin 20 (RFIN). Place them as far as possible from the RF signal lines.
- We recommend not placing signal lines in the vicinity of pins 28 (VCCRF) and 32 (VCCDDC).
- Make the wiring as thick as possible to keep the impedance low.
- Make sure that the RF GND is not divided by the wiring of the power supply line.
- Place a via hole for each bypass capacitor.
- We recommend not placing via holes between the IC and bypass capacitors.

Figure 7 shows an example of how to place the bypass capacitors.



Note: The level of generated noise depends on the implementation of the board. Add bypass capacitors as required (this figure is merely an example).

Figure 7 Example of How to Place the Bypass Capacitors

7. Ground Pattern

Note the following points for design in relation to the ground pattern.

- Place as many via holes as possible to create short circuits with ground patterns in other layers. This helps keep the impedance low.
- Connect pins 17 (MODE2), 18 (MODE1), 19 (RFIN), 21 (AGNDRF1), 23 (AGNDRF2), and 30 (VSSDDC) to the die pad. Note that the via holes for the ground pattern should not be placed near pin 30 (VSSDDC).
- We recommend not placing signal lines under the die pad if the signals may be active during transmission and reception.

Figure 8 shows an example of the layout pattern of the die pad.

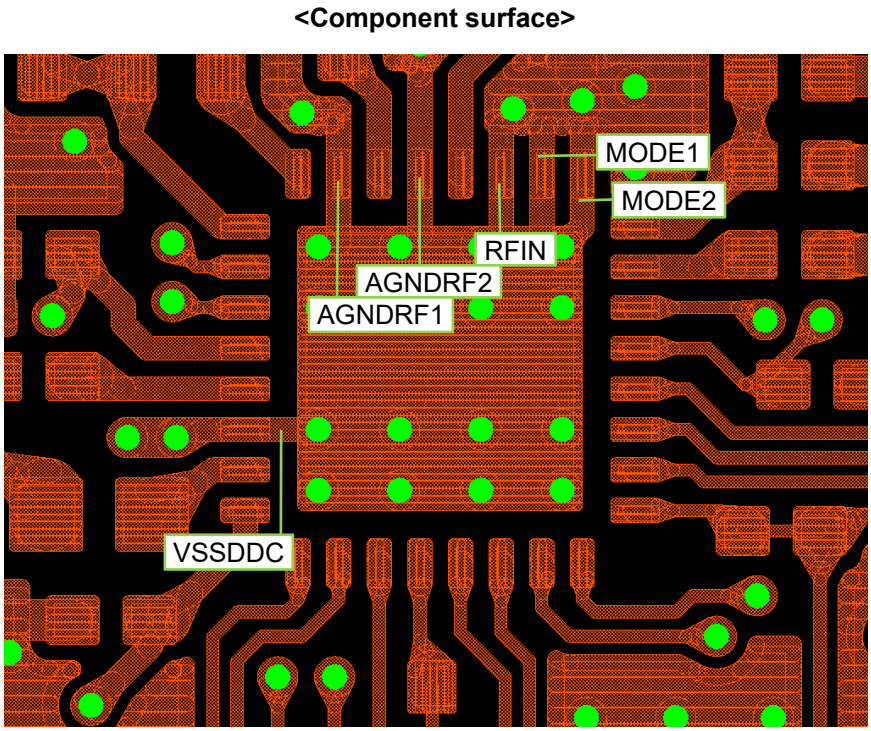


Figure 8 Example of Layout Pattern of the Die Pad

8. Circuit Diagram for Reference

Figure 9 and Figure 10 are circuit diagram for reference.

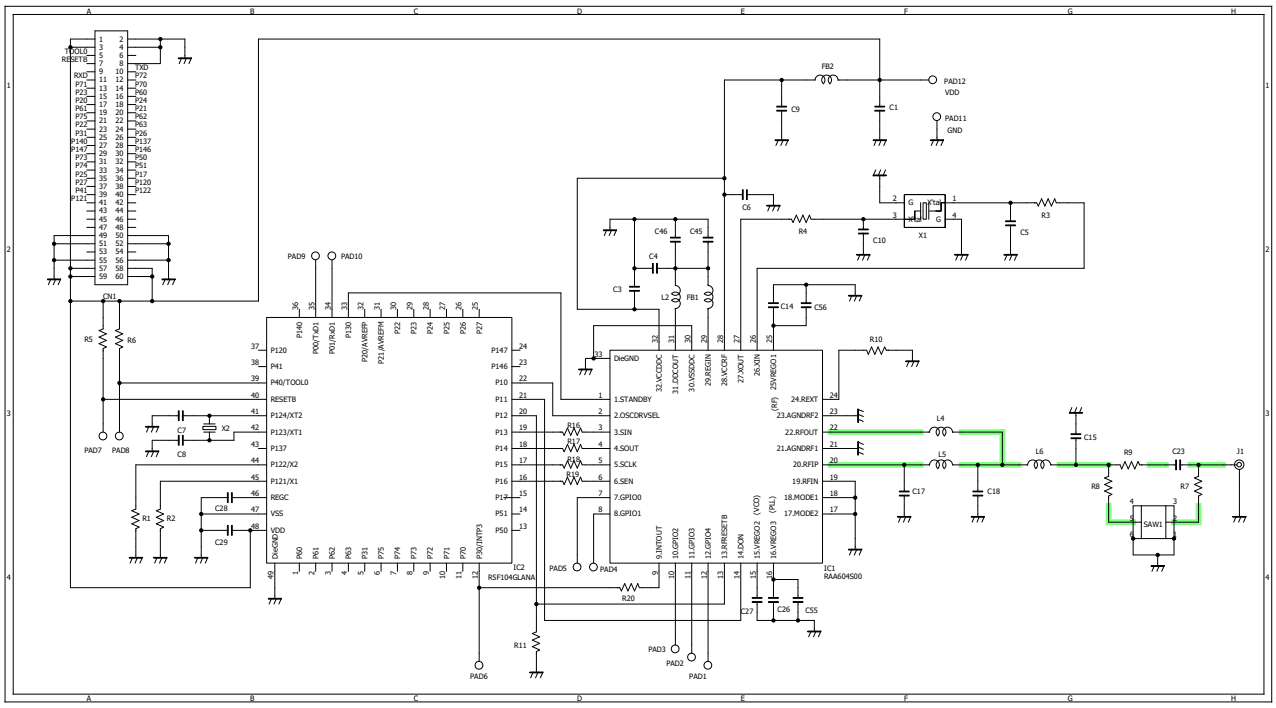


Figure 9 Circuit diagram for direct tie

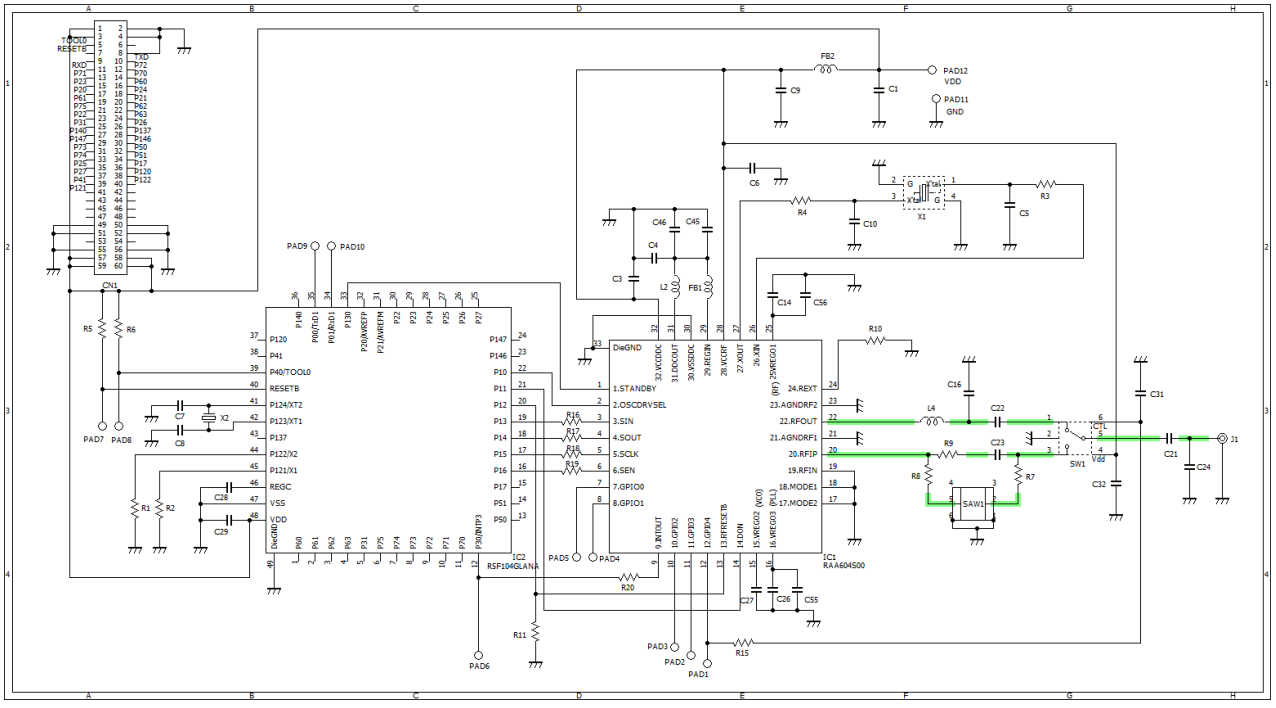


Figure 10 Circuit diagram with RF switch

9. List of Parts for Reference

Table 2 lists parts for reference.

Table 2 List of Parts for Reference (1/2)

Parts ID	Description	Parts number	Remarks
C1	1uF	GRM155B31C105KA12D	We recommend a tolerance of ± 10%.
C3	1uF	GRM155B31C105KA12D	We recommend a tolerance of ± 10%.
C4	Not mounted		
C5, C10	9pF	→	This provides a load capacitance for the crystal resonator and its value depends on the parasitic capacitance of the combination of the crystal resonator and the board on which it is mounted.
C6	1uF	GRM155B31C105KA12D	We recommend a tolerance of ± 10%.
C7, C8	Not mounted	→	This provides a load capacitance for the crystal resonator and its value depends on the parasitic capacitance of the combination of the crystal resonator and the board on which it is mounted.
C9	10uF	GRM188D71A106MA73	We recommend a tolerance of ± 10%.
C14	1uF	GRM155B31C105KA12D	We recommend a tolerance of ± 10%.
C15	3.3pF	GRM1553C1H3R3CZ01D	We recommend a tolerance equivalent to ± 0.25 pF.
C16*1	6pF*2 4.7pF*3*4*5	GRM1552C1H6R0CA01D GRM1552C1H4R7CZ01D	We recommend a tolerance equivalent to ± 0.25 pF.
C17	4.7pF	GRM1552C1H4R7CZ01D	We recommend a tolerance equivalent to ± 0.25 pF.
C18	5.6pF	GRM1552C1H5R6CA01D	We recommend a tolerance equivalent to ± 0.25 pF.
C21*1	47pF	GRM1552C1H470JA01D	DC blocking capacitor
C22*1	47pF*2 8.2nH*3*4*5	GRM1552C1H470JA01D LQW15AN8N2C10	DC blocking capacitor Mounting an inductor here is a way of reducing harmonics during signal transmission.
C23	47pF	GRM1552C1H470JA01D	DC blocking capacitor
C24	Not mounted		
C26	1uF	GRM155B31C105KA12D	We recommend a tolerance of ± 10%.
C27	1uF	GRM155B31C105KA12D	We recommend a tolerance of ± 10%.
C28	1uF	GRM155B31C105KA12D	We recommend a tolerance of ± 10%.
C29	1uF	GRM155B31C105KA12D	We recommend a tolerance of ± 10%.
C31*1	1000pF	GRM1552C1H102JA01D	Decoupling capacitor
C32*1	1000pF	GRM1552C1H102JA01D	Decoupling capacitor
C45	Not mounted		Mounting a capacitor here is a way of reducing noise in received signals. Example value: 47 pF (self-resonance frequency of about 1 GHz)
C46	1uF	GRM155B31C105KA12D	We recommend a tolerance of ± 10%.
C55	Not mounted		Mounting a capacitor here is a way of reducing noise in received signals. Example value: 12 pF (self-resonance frequency of about 2.5 GHz)
C56	Not mounted		Mounting a capacitor here is a way of reducing spurious emissions during signal transmission. Example value: 2.2 nF (self-resonance frequency of about 200 MHz)
CN1	Connector	DF17(2.0)-60DP-0.5V(57)	
PAD	Test-pin	9-146278-0	

*1 with RF switch, *2 for ARIB, *3 for ETSI, *4 for FCC, *5 for World/Wide

Table 2 List of Parts for Reference (2/2)

Parts ID	Description	Parts number	Remarks
L2	10uH	MLZ1608M100WT	We recommend an MLZ1608M100WT (with a tolerance of ± 20%). The inductor is required to have good DC superposition characteristics, so we recommend an inductor with a low loss (a low DC resistance and a low AC impedance at the operating frequency). The current running through the MLZ1608M100WT is about 100 mA when the transmission output is at its maximum amplitude.
L4	2.2nH 4.7nH*1*2 7.3nH*1*3*4*5	LQW15AN2N2C10 LQW15AN4N7C10 LQW15AN7N3C10	We recommend a tolerance equivalent to ±0.2 nH. Using a chip inductor intended for high frequencies is essential. The inductor is required to have high Q values across the 1-GHz band and a self-resonance frequency above 1 GHz.
L5, L6	5.6nH	LQW15AN5N6C10	We recommend a tolerance equivalent to ± 0.2 nH. Using a chip inductor intended for high frequencies is essential. The inductor is required to have high Q values across the 1-GHz band and a self-resonance frequency above 1 GHz.
R1, R2	100kΩ	RK73H1ETTP1003F	Pull-down resistor
R3, R4	0Ω*2*4 22nH*3*5	MCR01MZPJ000 LQG15HS22NJ02D	It can reduce spurious caused by clock. Example value: 22 nH (self-resonance frequency of about 1.8 GHz)
R5, R6	10kΩ	RK73H1ETTP1002F	Pull-up resistor
R7	Not mounted		When using the SAW filter, mount it instead of C23.
R8	Not mounted		When using the SAW filter, mount it instead of R9.
R9	0Ω	MCR01MZPJ000	
R10	56kΩ	RK73H1ETTP5602F	It is required to have a tolerance of ± 1%.
R11	10kΩ	RK73H1ETTP1002F	Pull-down resistor
R15*1	1kΩ	RK73B1ETTP102J	It can reduce the noise component of the RF switch control line.
R16	0Ω	MCR01MZPJ000	
R17	300Ω	RK73B1ETTP301J	It can reduce the noise of the digital signal line
R18	0Ω	MCR01MZPJ000	
R19	0Ω	MCR01MZPJ000	
R20	300Ω	RK73B1ETTP301J	It can reduce the noise of the digital signal line
FB1	0Ω	MCR01MZPJ000	Usually, 0Ω is placed. Insert the ferrite beads (FB1) arbitrarily according to the noise condition caused by the DC-DC converter. In that case, use the ferrite bead with an impedance of about 10Ω. If the impedance is too high, the power circuit inside the IC may oscillate. Example: BLM15PG100SN1D (Impedance of about 10Ω@100MHz)
FB2	Ferrite Beads	BLM15AX102SN1	It can reduce the noise component of the power supply line.
J1	SMA	73251-1150	
SAW	SAW filter		Example: B3717*3, B3926*2 from EPSOS
SW*1	RF switch	BGS12SN6	We recommend the SPDT of single control.
X1	Crystal resonator 48 MHz	→	We recommend using a crystal resonator* with CL = 6 pF and ESR ≤ 50 Ω. Note: We recommend the NX2016SA (CHP-CZS-43) from NDK, CX1612DB48000B0WPNC1 from KYOCERA, or XRCMD48M000FXQ60R0 from Murata.
X2	Crystal resonator 32.768 kHz	Not mounted	Subsystem Clock for MCU Example: SSP-T7-FL from Seiko Instruments
IC2	MCU	R5F104GLANA	RL78/G14 from Renesas Electronics

*1 with RF switch, *2 for ARIB, *3 for ETSI, *4 for FCC, *5 for World/Wide

9.1 Main parts list

Table 3 lists constants for main parts. It is necessary to mount parts according to the radio law of the region to be used.

Table 3 Parts constants corresponding to each radio law

Region	Radio low	Circuit configuration	Capacitor[pF]						Inductor[nH]			Resistor[Ω]	
			C15	C16	C17	C18	C21	C22	L4	L5	L6	R3	R4
Japan	ARIB	Direct Tie	3.3	-	4.7	5.6	-		2.2	5.6	5.6	0	0
		with RF switch	-	6	-	-	47	47	4.7	-	-	0	0
EU	ETSI	Direct Tie	3.3	-	4.7	5.6	-	-	2.2	5.6	5.6	22nH	22nH
		with RF switch	-	4.7	-	-	47	8.2nH	7.3	-	-	22nH	22nH
US	FCC	Direct Tie	3.3	-	4.7	5.6	-	-	2.2	5.6	5.6	0	0
		with RF switch	-	4.7	-	-	47	8.2nH	7.3	-	-	0	0
W/W	ALL	Direct Tie	3.3	-	4.7	5.6	-	-	2.2	5.6	5.6	22nH	22nH
		with RF switch	-	4.7	-	-	47	8.2nH	7.3	-	-	22nH	22nH

Website and Support

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Dec 21, 2018		First edition issued
2.00	Dec 16, 2022	10	Updated Table 2 (1/2).
		11	Updated Table 2 (2/2).
		12	Updated Table 3.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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