
R8C/M12A Group

Timer RB2 in Timer Mode

R01AN0089EJ0101

Rev.1.01

Mar. 10, 2011

1. Abstract

This document describes a setting method and an application example for timer RB2 in timer mode in the R8C/M12A Group.

2. Introduction

The application example described in this document applies to the following microcomputer (MCU) and parameter:

- MCU: R8C/M12A Group
- XIN clock frequency: 20 MHz

This application note can be used with other R8C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Application Example

3.1 Program Outline

Generate the timer RB2 interrupt every 1 ms using timer RB2 in timer mode.

Settings

- Set the count source as f2 (10 MHz).
- Set the timer RB counter to an 8-bit timer with an 8-bit prescaler.
- Set the timer RB write control bit to 0 (write to reload register and counter).
- Use the timer RB2 interrupt.

Calculating setting time

$$\begin{aligned}
 1 \text{ ms} &= 1 \div \text{XIN} \times 2 \times (\text{TRBPRE} + 1) \times (\text{TRBPR} + 1) \\
 &= 1 \div 20 \text{ MHz} \times 2 \times (199 + 1) \times (49 + 1) \\
 &= 50 \text{ ns} \times 2 \times 200 \times 50
 \end{aligned}$$

Figure 3.1 shows a Block Diagram and Figure 3.2 shows a Timing Diagram.

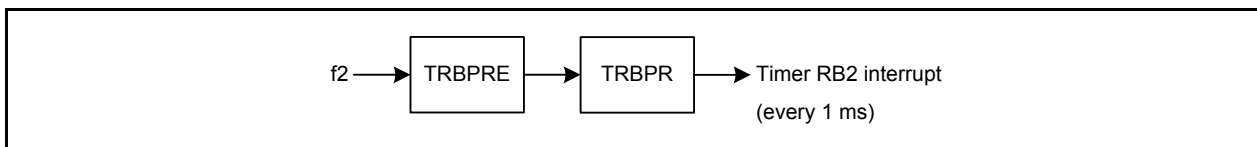


Figure 3.1 Block Diagram

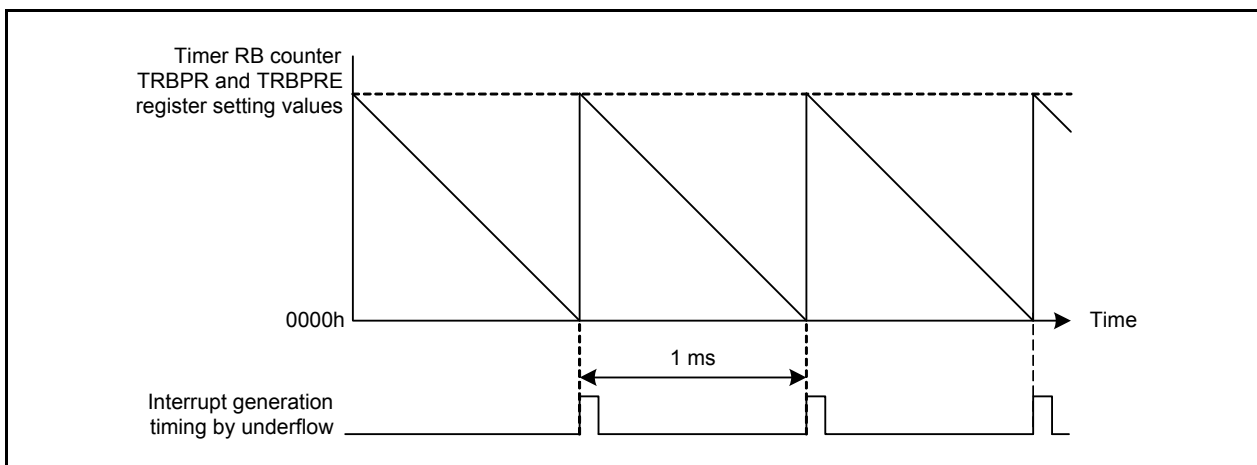


Figure 3.2 Timing Diagram

3.2 Memory

Table 3.1 Memory

Memory	Size	Remarks
ROM	165 bytes	In the r01an0089_src.c module
RAM	0 bytes	In the r01an0089_src.c module
Maximum user stack	10 bytes	
Maximum interrupt stack	18 bytes	

Memory size varies depending on the C compiler version and compile options.

The above applies to the following conditions:

C compiler: M16C Series, R8C Family C Compiler V.5.45 Release 01

Compile options: -c -finfo -dir "\$(CONFIGDIR)" -R8C

4. Software

This section shows the initial setting procedures and values to set the example described in section 3. **Application Example.** Refer to the latest **R8C/M12A Group** hardware user's manual for details on individual registers.

The × in the register's Setting Value represents bits not used in this application, blank spaces represent bits that do not change, and the dash represents reserved bits or bits that have nothing assigned.

4.1 Function Tables

Declaration	void main (void)		
Outline	Main function		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Initialize the system clock and timer RB2.		

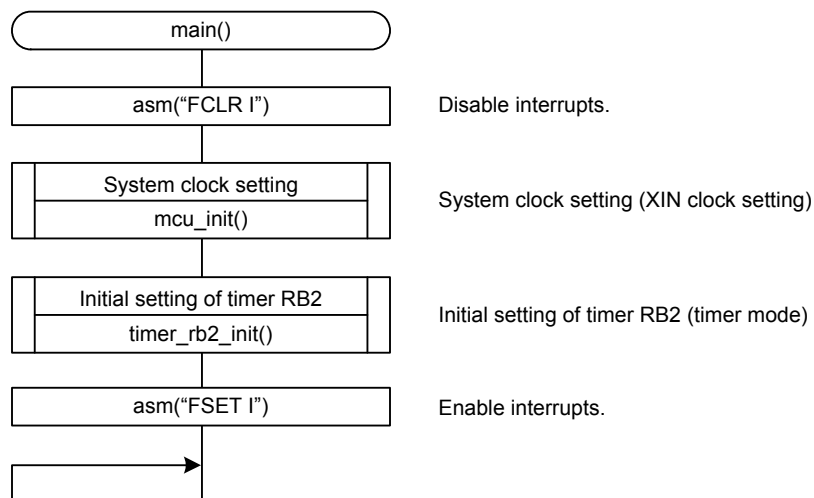
Declaration	void mcu_init (void)		
Outline	System clock setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Set the system clock (XIN clock).		

Declaration	void timer_rb2_init (void)		
Outline	Initial setting of timer RB2		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Initialize SFRs to use timer RB2 in timer mode.		

Declaration	void _timer_rb2 (void)		
Outline	Timer RB2 interrupt handling		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Perform timer RB2 interrupt handling.		

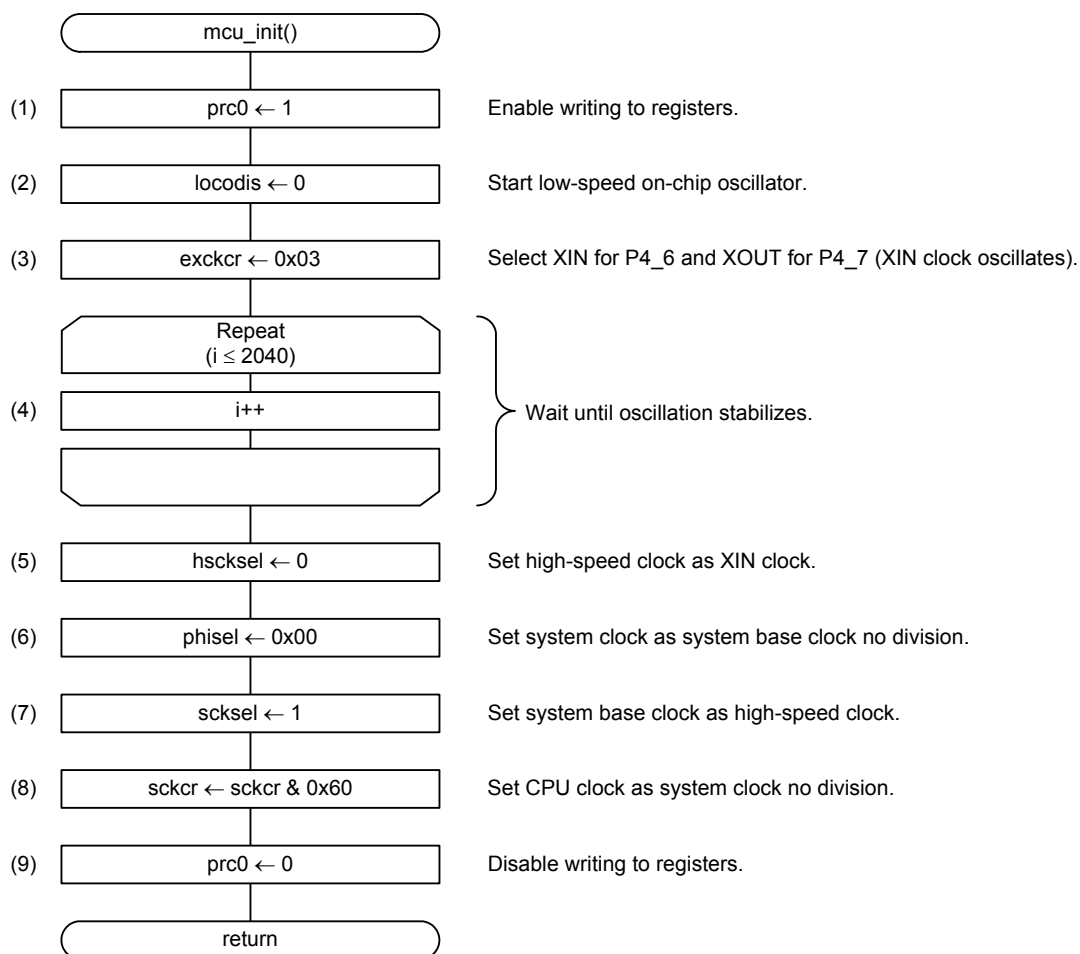
4.2 Main Function

• Flowchart



4.3 System Clock Setting

• Flowchart



- Register settings

- (1) Enable writing to registers EXCKCR, OCOCR, SCKCR, PHISEL, CKSTPR, CKRSCR, BAKCR, FRV1, and FRV2.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	x	x	—	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers EXCKCR, OCOCR, SCKCR, PHISEL, CKSTPR, CKRSCR, BAKCR, FRV1, and FRV2 1: Enabled	R/W

- (2) Start the low-speed on-chip oscillator.

High-Speed/Low-Speed On-Chip Oscillator Control Register (OCOCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	—	—	0	x

Bit	Symbol	Bit Name	Function	R/W
b1	LOCODIS	Low-speed on-chip oscillator oscillation stop bit	0: Low-speed on-chip oscillator on	R/W

- (3) Oscillate the XIN clock.

External Clock Control Register (EXCKCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	x	—	—	—	—	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	CKPT0	Port P4_6 and P4_7 pin function select bits	P4_6 pin b1 b0	P4_7 pin b1 b0
b1	CKPT1		1 1: XIN	1 1: XOUT

- (4) Wait until the XIN clock oscillation stabilizes.

- (5) Set the high-speed clock as the XIN clock.

System Clock f Control Register (SCKCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	0	x	—	—			

Bit	Symbol	Bit Name	Function	R/W
b6	HSCKSEL	High-speed on-chip oscillator/XIN clock select bit	0: XIN clock	R/W

- (6) Set the system clock as the system base clock with no division.

System Clock f Select Register (PHISEL)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PHISEL0	System clock division select bits	These bits used to set the division ratio of the system base clock (fBASE) to generate the system clock (f) System clock (f) $f = fBASE/(n + 1)$ n: Binary value set by the PHISEL register	R/W
b1	PHISEL1			R/W
b2	PHISEL2			R/W
b3	PHISEL3			R/W
b4	PHISEL4			R/W
b5	PHISEL5			R/W
b6	PHISEL6			R/W
b7	PHISEL7			R/W

- (7) Set the system base clock as the high-speed clock.

Clock Stop Control Register (CKSTPR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	—	—	—	—	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b7	SCKSEL	System base clock select bit	1: fHSCK	R/W

- (8) Set the CPU clock as the system clock with no division.

System Clock f Control Register (SCKCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	x	—	—	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PHISSEL0	CPU clock division select bits	b2 b1 b0 0 0 0: fs = System clock with no division	R/W
b1	PHISSEL1			R/W
b2	PHISSEL2			R/W

- (9) Disable writing to registers EXCKCR, OCOCR, SCKCR, PHISEL, CKSTPR, CKRSCR, BAKCR, FRV1, and FRV2.

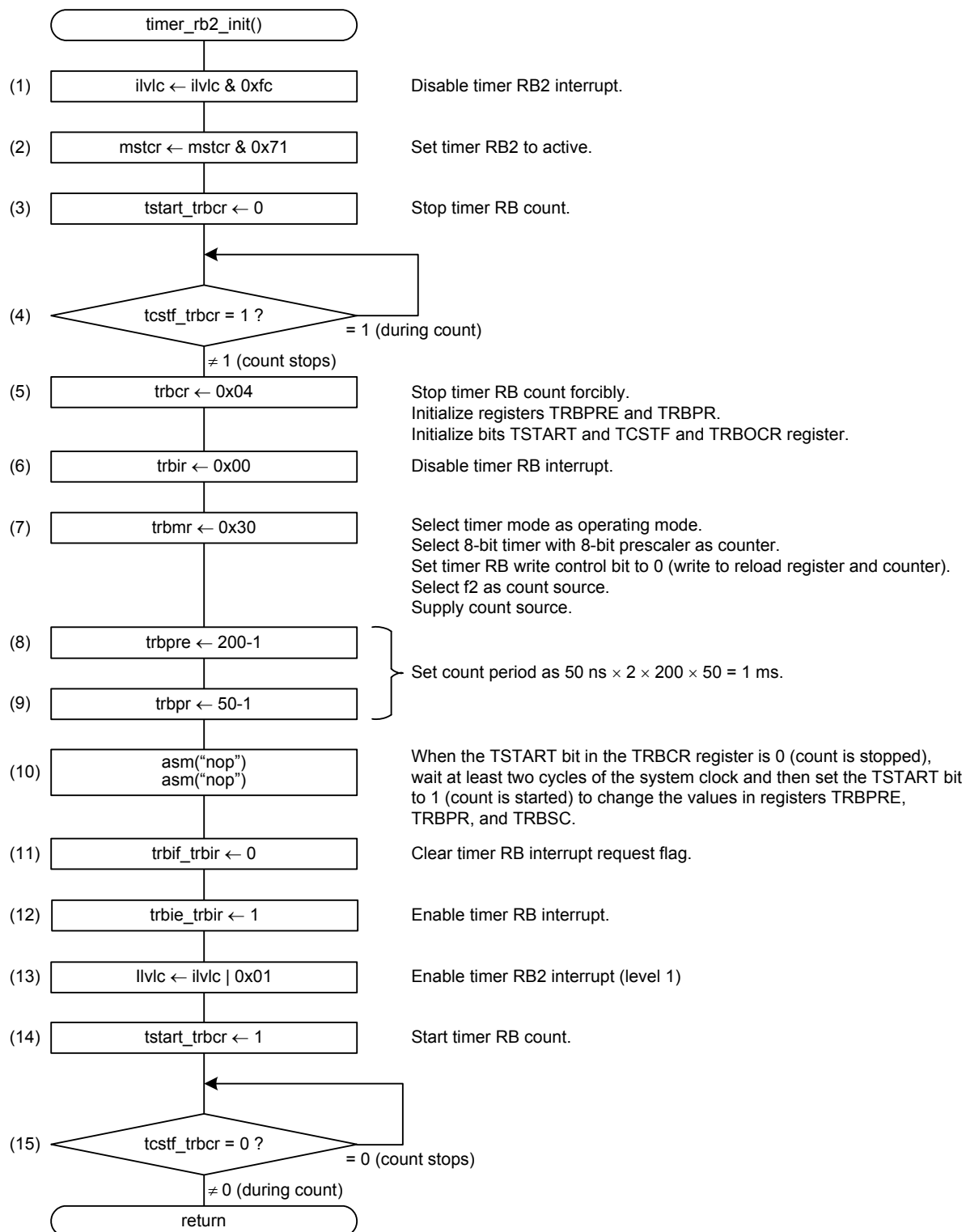
Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	x	x	—	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers EXCKCR, OCOCR, SCKCR, PHISEL, CKSTPR, CKRSCR, BAKCR, FRV1, and FRV2 0: Disabled	R/W

4.4 Initial Setting of Timer RB2

• Flowchart



- Register settings

(1) Disable the timer RB2 interrupt.

Interrupt Priority Level Register C (ILVLC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	x	x	—	—	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVLC0	Interrupt priority level setting bits	b1 b0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVLC1			R/W

(2) Set timer RB2 to active.

Module Standby Control Register (MSTCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	x	x	x	—	—	0	x

Bit	Symbol	Bit Name	Function	R/W
b1	MSTTRB	Timer RB2 standby bit	0: Active	R/W

(3) Stop the timer RB count.

Timer RB Control Register (TRBCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	—			0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RB count start bit	0: Count is stopped	R/W

(4) Wait until the timer RB count stops.

Timer RB Control Register (TRBCR)

Bit	Symbol	Bit Name	Function	R/W
b1	TCSTF	Timer RB count status flag	0: Count is stopped 1: Count is in progress	R

- (5) Initialize the counter, registers TRBPRES and TRBPR, and bits TSTART and TCSTF.

Timer RB Control Register (TRBCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	—	1		

Bit	Symbol	Bit Name	Function	R/W
b2	TSTOP	Timer RB count forced stop bit	When 1 is written to this bit, the count is forcibly stopped. The read value is 0.	R/W

- (6) Disable the timer RB interrupt.

Timer RB Interrupt Control Register (TRBIR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0		—	—	—	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b7	TRBIE	Timer RB interrupt enable bit	0: Interrupt disabled	R/W

- (7) Set the timer RB mode register.

Timer RB Mode Register (TRBMR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	1	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RB operating mode select bits	b1 b0 0 0: Timer mode	R/W
b1	TMOD1			R/W
b2	TCNT16	Timer RB counter select bit	0: 8-bit timer with 8-bit prescaler	R/W
b3	TWRC	Timer RB write control bit	0: Write to reload register and counter	R/W
b4	TCK0	Timer RB count source select bits	b6 b5 b4 0 1 1: f2	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	TCKCUT	Timer RB count source cutoff bit	0: Count source is supplied	R/W

- (8) Set 200-1 (C7h) to the timer RB prescaler register.

Timer RB Prescaler Register (TRBPRES)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	1	0	0	0	1	1	1

Bit	Function	Setting Range	R/W
b7 to b0	An internal count source is counted	00h to FFh	R/W

(9) Set 50-1 (31h) to the timer RB primary register.

Timer RB Primary Register (TRBPR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	1	1	0	0	0	1

Bit	Function	Setting Range	R/W
b7 to b0	Timer RB prescaler underflow is counted.	00h to FFh	R/W

(10) Wait for at least two cycles of the system clock.

(11) Initialize the timer RB interrupt request flag.

Timer RB Interrupt Control Register (TRBIR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value		0	—	—	—	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b6	TRBIF	Timer RB interrupt request flag	0: No interrupt requested	R/W

(12) Enable the timer RB interrupt.

Timer RB Interrupt Control Register (TRBIR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1		—	—	—	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b7	TRBIE	Timer RB interrupt enable bit	1: Interrupt enabled	R/W

(13) Enable the timer RB2 interrupt (level 1).

Interrupt Priority Level Register C (ILVLC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	x	x	—	—	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	ILVLC0	Interrupt priority level setting bits	b1 b0 0 1: Level 1	R/W
b1	ILVLC1			R/W

(14) Start the timer RB count.

Timer RB Control Register (TRBCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	—	—	—	1

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RB count start bit	1: Count is started	R/W

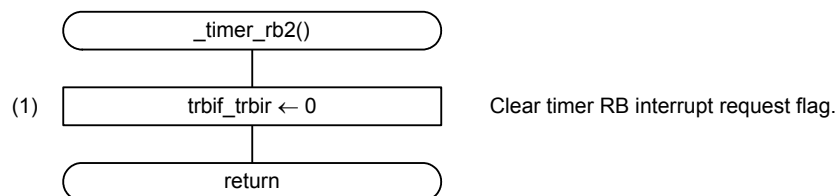
(15) Wait until the timer RB count starts.

Timer RB Control Register (TRBCR)

Bit	Symbol	Bit Name	Function	R/W
b1	TCSTF	Timer RB count status flag	0: Count is stopped 1: Count is in progress	R

4.5 Timer RB2 Interrupt Handling

• Flowchart



• Register setting

(1) Initialize the timer RB interrupt request flag.

Timer RB Interrupt Control Register (TRBIR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	0	—	—	—	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b6	TRBIF	Timer RB interrupt request flag	0: No interrupt requested	R/W

5. Sample Program

A sample program can be downloaded from the Renesas Electronics website.

To download, click “Application Notes” in the left-hand side menu of the R8C Family page.

6. Reference Documents

R8C/M12A Group User's Manual: Hardware Rev.1.00

The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

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Revision History	R8C/M12A Group Timer RB2 in Timer Mode
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Rev.	Date	Description	
		Page	Summary
1.00	Nov. 24, 2010	—	First edition issued
1.01	Mar. 10, 2011	—	R8C/M12A Group hardware user's manual Rev.1.00 reviewed
		6	High-speed/low-speed on-chip oscillator control register (OCOCR) revised External clock control register (EXCKCR) revised
		7	System clock f select register (PHISEL) revised System clock f control register (SCKCR) revised
		10, 11, 12	Timer RB interrupt control register (TRBIR) revised

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1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
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3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

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