R8C/35C Group

Flash Memory Low-Current-Consumption Read Mode

R01AN0080EJ0100
Rev.1.00
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1. Abstract

This document describes a setting method and an application example for flash memory low-current-consumption read mode. Power consumption can be reduced using low-speed on-chip oscillator mode (XIN clock stops) and low-current-consumption read mode.

2. Introduction

The application example described in this document applies to the following microcomputer (MCU) and parameter:

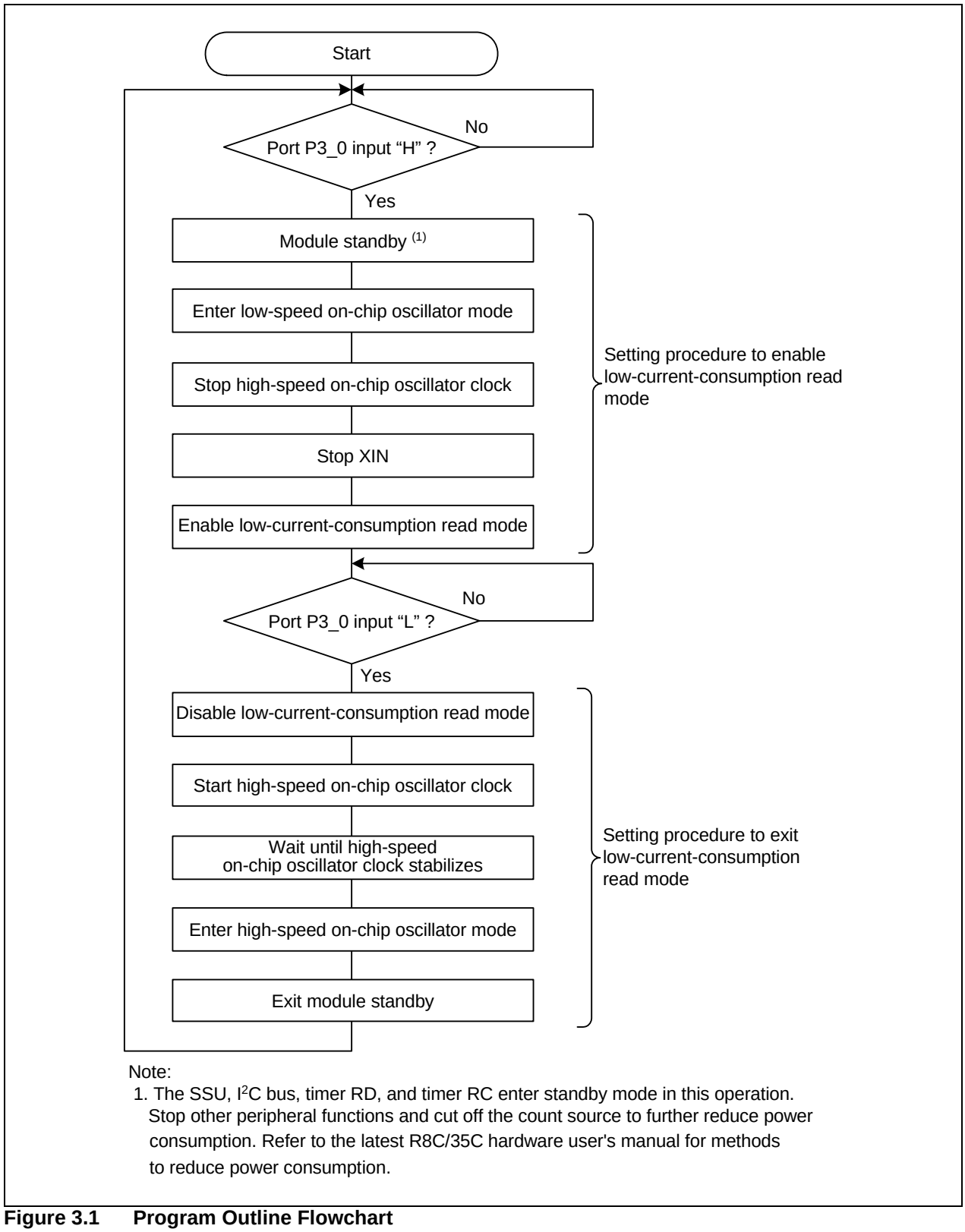
- MCU: R8C/35C Group
- Oscillator stop detect function: Disable

This application note can be used with other R8C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Application Example

3.1 Program Outline

Use port P3_0 input to switch between enabling and disabling low-current-consumption read mode.
Figure 3.1 shows the Program Outline Flowchart.



Note:
1. The SSU, I²C bus, timer RD, and timer RC enter standby mode in this operation. Stop other peripheral functions and cut off the count source to further reduce power consumption. Refer to the latest R8C/35C hardware user's manual for methods to reduce power consumption.

Figure 3.1 Program Outline Flowchart

3.2 Pin Used

Table 3.1 Pin used and its function

Pin Name	I/O	Function
P3_0	Input	Switch between enabling and disabling low-current-consumption read mode.

3.3 Memory

Table 3.2 Memory

Memory	Size	Remarks
ROM	207 bytes	In the r01an0080_src.c module
RAM	0 bytes	In the r01an0080_src.c module
Maximum user stack	10 bytes	main function: 3 bytes mcu_init function: 7 bytes low_current_enable function: 3 bytes low_current_disable function: 7 bytes
Maximum interrupt stack	0 bytes	Not used

Memory size varies depending on the C compiler version and compile options.
The above applies to the following conditions:
C compiler: M16C Series, R8C Family C Compiler V.5.45 Release 01
Compile options: -c -finfo -dir “$(CONFIGDIR)” -R8C

3.4 Power Supply Current in Low-Current-Consumption Read Mode

Table 3.3 Power Supply Current
(Electrical Characteristics in R8C/35C Group hardware user's manual Rev.1.00)
Topr = – 20 to 85 °C (N version) / – 40 to 85 °C (D version)

Parameter	Condition		Standard	
			Typ. (μA)	Max. (μA)
Power supply current (3.3 V ≤ Vcc ≤ 5.5 V) Single-chip mode, output pins are open, other pins are Vss	Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	90	400
	Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division, FMR27 = 1, VCA20 = 0	85	400
Power supply current (2.7 V ≤ Vcc < 3.3 V) Single-chip mode, output pins are open, other pins are Vss	Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	90	390
	Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division, FMR27 = 1, VCA20 = 0	80	400
Power supply current (1.8 V ≤ Vcc < 2.7 V) Single-chip mode, output pins are open, other pins are Vss	Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	90	300
	Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division, FMR27 = 1, VCA20 = 0	80	350

4. Settings

This section shows the initial setting procedures and values to set the example described in section **3. Application Example**. Refer to the latest **R8C/35C Group hardware user's manual** for details on individual registers. The × in the register's Setting Value represents bits not used in this application, and blank spaces represent bits that do not change, and the dash represents reserved bits or bits that have nothing assigned.

4.1 System Clock Setting

(1) Enable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

Protect Register (PRCR)

Address 000Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PRC3	PRC2	PRC1	PRC0
Setting Value					x	x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 1: Write enabled	R/W

(2) Start the low-speed on-chip oscillator.

System Clock Control Register 1 (CM1)

Address 0007h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM17	CM16	—	CM14	CM13	CM12	CM11	CM10
Setting Value				0	x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b4	CM14	Low-speed on-chip oscillator stop bit	0: Low-speed on-chip oscillator on	R/W

Rewrite the CM1 register after setting the PRC0 bit in the PRCR register to 1 (write enabled).

(3) Set the division ratio of the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 2 (FRA2)

Address 0025h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	FRA22	FRA21	FRA20
Setting Value	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA20	High-speed on-chip oscillator frequency switching bit	Division selection These bits select the division ratio for the high-speed on-chip oscillator clock. b2 b1 b0 0 0 0: Divide-by-2 mode	R/W
b1	FRA21			R/W
b2	FRA22			R/W
b3	—	Reserved bits	Set to 0.	R/W
b4	—			
b5	—			
b6	—			
b7	—			

Rewrite the FRA2 register after setting the PRC0 bit in the PRCR register to 1 (write enabled).

(4) Start the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Address 0023h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	FRA03	—	FRA01	FRA00
Setting Value					x			1

Bit	Symbol	Bit Name	Function	R/W
b0	FRA00	High-speed on-chip oscillator enable bit	1: High-speed on-chip oscillator on	R/W

Rewrite the FRA0 register after setting the PRC0 bit in the PRCR register to 1 (write enabled).

(5) Wait until oscillation stabilizes.

(6) Set the oscillation stop detection register.

Oscillation Stop Detection Register (OCD)

Address 000Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	OCD3	OCD2	OCD1	OCD0
Setting Value	0	0	0	0	0	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	OCD0	Oscillation stop detection enable bit	0: Oscillation stop detection function disabled	R/W
b1	OCD1	Oscillation stop detection interrupt enable bit	0: Disabled	R/W
b2	OCD2	System clock select bit	1: On-chip oscillator clock selected	R/W
b3	OCD3	Clock monitor bit	0: XIN clock oscillates	R
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Rewrite the OCD register after setting the PRC0 bit in the PRCR register to 1 (write enabled).

(7) Stop the XIN clock.

System Clock Control Register 0 (CM0)

Address 0006h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM07	CM06	CM05	CM04	CM03	CM02	—	—
Setting Value	x		1	x	x	x		

Bit	Symbol	Bit Name	Function	R/W
b5	CM05	XIN clock (XIN-XOUT) stop bit	1: XIN clock stops	R/W

Rewrite the CM0 register after setting the PRC0 bit in the PRCR register to 1 (write enabled).

(8) Select the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Address 0023h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	FRA03	—	FRA01	FRA00
Setting Value					x		1	

Bit	Symbol	Bit Name	Function	R/W
b1	FRA01	High-speed on-chip oscillator select bit	1: High-speed on-chip oscillator selected	R/W

Rewrite the FRA0 register after setting the PRC0 bit in the PRCR register to 1 (write enabled).

(9) Set CPU clock division select bit 1.

System Clock Control Register 1 (CM1)

Address 0007h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM17	CM16	—	CM14	CM13	CM12	CM11	CM10
Setting value	0	0			x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b6	CM16	CPU clock division select bit 1	b7 b6 0 0: No division mode	R/W
b7	CM17			R/W

Rewrite the CM1 register after setting the PRC0 bit in the PRCR register to 1 (write enabled)

(10) Set CPU clock division select bit 0.

System Clock Control Register 0 (CM0)

Address 0006h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM07	CM06	CM05	CM04	CM03	CM02	—	—
Setting Value	x	0		x	x	x		

Bit	Symbol	Bit Name	Function	R/W
b6	CM06	CPU clock division select bit 0	0: Bits CM16 and CM17 in CM1 register enabled	R/W

Rewrite the CM0 register after setting the PRC0 bit in the PRCR register to 1 (write enabled).

(11) Disable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

Protect Register (PRCR)

Address 000Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PRC3	PRC2	PRC1	PRC0
Setting Value					x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 0: Write disabled	R/W

4.2 Port P3_0 Input Setting

(1) Set the port P3_0 direction bit to input mode.

Port P3 Direction Register (PD3)

Address 00E7h (PD3)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PD3_7	PD3_6	PD3_5	PD3_4	PD3_3	PD3_2	PD3_1	PD3_0
Setting Value	x	x	x	x	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PD3_0	Port P3_0 direction bit	0: Input mode (functions as an input port)	R/W

4.3 Setting Procedure to Enable Low-Current-Consumption Read Mode

(1) Set the SSU, I^2C bus standby bit, timer RD standby bit, and timer RC standby bit to standby.

Module Standby Control Register (MSTCR)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	MSTTRC	MSTTRD	MSTIIC	—	—	—
Setting Value	0	0	1	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	MSTIIC	SSU, I^2C bus standby bit	1: Standby	R/W
b4	MSTTRD	Timer RD standby bit	1: Standby	R/W
b5	MSTTRC	Timer RC standby bit	1: Standby	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

(2) Enable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

Protect Register (PRCR)

Address 000Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PRC3	PRC2	PRC1	PRC0
Setting Value					x	x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 1: Write enabled	R/W

(3) Select the system clock as the on-chip oscillator clock.

Oscillation Stop Detection Register (OCD)

Address 000Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	OCD3	OCD2	OCD1	OCD0
Setting Value						1		

Bit	Symbol	Bit Name	Function	R/W
b2	OCD2	System clock select bit	1: On-chip oscillator clock selected	R/W

Rewrite the OCD register after setting the PRC0 bit in the PRCR register to 1 (write enabled).

(4) Select the low-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Address 0023h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	FRA03	—	FRA01	FRA00
Setting Value					x		0	

Bit	Symbol	Bit Name	Function	R/W
b1	FRA01	High-speed on-chip oscillator select bit	0: Low-speed on-chip oscillator selected	R/W

Rewrite the FRA0 register after setting the PRC0 bit in the PRCR register to 1 (write enabled).

(5) Stop the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Address 0023h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	FRA03	—	FRA01	FRA00
Setting Value					x			0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA00	High-speed on-chip oscillator enable bit	0: High-speed on-chip oscillator off	R/W

Rewrite the FRA0 register after setting the PRC0 bit in the PRCR register to 1 (write enabled).

(6) Stop the XIN clock.

System Clock Control Register 0 (CM0)

Address 0006h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM07	CM06	CM05	CM04	CM03	CM02	—	—
After Reset	x		1	x	x	x		

Bit	Symbol	Bit Name	Function	R/W
b5	CM05	XIN clock (XIN-XOUT) stop bit	1: XIN clock stops	R/W

Rewrite the CM0 register after setting the PRC0 bit in the PRCR register to 1 (write enabled).

(7) Set the CPU clock division ratio to divide-by-8 mode.

System Clock Control Register 0 (CM0)

Address 0006h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM07	CM06	CM05	CM04	CM03	CM02	—	—
After Reset	x	1		x	x	x		

Bit	Symbol	Bit Name	Function	R/W
b6	CM06	CPU clock division select bit 0	1: Divide-by-8 mode	R/W

Rewrite the CM0 register after setting the PRC0 bit in the PRCR register to 1 (write enabled).

(8) Disable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

Protect Register (PRCR)

Address 000Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PRC3	PRC2	PRC1	PRC0
Setting Value					x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 0: Write Disabled	R/W

(9) Disable CPU rewrite mode.

Flash Memory Control Register 0 (FMR0)

Address 01B4h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RDYSTIE	BSYAEIE	CMDERIE	CMDRST	FMSTP	FMR02	FMR01	—
Setting Value	x	x	x	x	x	x	0	

Bit	Symbol	Bit Name	Function	R/W
b1	FMR01	CPU rewrite mode select bit	0: CPU rewrite mode disabled	R/W

(10) Clear the I flag to disable the interrupt.

(11) Enable low-current-consumption read mode.

Flash Memory Control Register 2 (FMR2)

Address 01B6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FMR27	—	—	—	—	FMR22	FMR21	FMR20
Setting Value	1					x	x	x

Bit	Symbol	Bit Name	Function	R/W
b7	FMR27	Low-consumption-current read mode enable bit	1: Low-consumption-current read mode enabled	R/W

(12) Set the I flag to enable the interrupt.

4.4 Disable Low-Current-Consumption Read Mode

(1) Disable low-current-consumption read mode.

Flash Memory Control Register 2 (FMR2)

Address 01B6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FMR27	—	—	—	—	FMR22	FMR21	FMR20
Setting Value	0					x	x	x

Bit	Symbol	Bit Name	Function	R/W
b7	FMR27	Low-consumption-current read mode enable bit	0: Low-consumption-current read mode disabled	R/W

(2) Enable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

Protect Register (PRCR)

Address 000Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PRC3	PRC2	PRC1	PRC0
Setting Value					x	x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 1: Write enabled	R/W

(3) Set CPU clock division select bit 1.

System Clock Control Register 1 (CM1)

Address 0007h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM17	CM16	—	CM14	CM13	CM12	CM11	CM10
After Reset	0	0			x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b6	CM16	CPU clock division select bit 1	b7 b6 0 0: No division mode	R/W
b7	CM17			R/W

Rewrite the CM1 register after setting the PRC0 bit in the PRCR register to 1 (write enabled).

(4) Set CPU clock division select bit 0.

System Clock Control Register 0 (CM0)

Address 0006h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM07	CM06	CM05	CM04	CM03	CM02	—	—
After Reset	x	0		x	x	x		

Bit	Symbol	Bit Name	Function	R/W
b6	CM06	CPU clock division select bit 0	0: Bits CM16 and CM17 in CM1 register enabled	R/W

Rewrite the CM0 register after setting the PRC0 bit in the PRCR register to 1 (write enabled).

(5) Start the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Address 0023h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	FRA03	—	FRA01	FRA00
Setting Value					x			1

Bit	Symbol	Bit Name	Function	R/W
b0	FRA00	High-speed on-chip oscillator enable bit	1: High-speed on-chip oscillator on	R/W

Rewrite the FRA0 register after setting the PRC0 bit in the PRCR register to 1 (write enabled).

(6) Wait until oscillation stabilizes.

(7) Select the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Address 0023h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	FRA03	—	FRA01	FRA00
Setting Value					x		1	

Bit	Symbol	Bit Name	Function	R/W
b1	FRA01	High-speed on-chip oscillator select bit	1: High-speed on-chip oscillator selected	R/W

Rewrite the FRA0 register after setting the PRC0 bit in the PRCR register to 1 (write enabled).

(8) Disable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

Protect Register (PRCR)

Address 000Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PRC3	PRC2	PRC1	PRC0
Setting Value					x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 0: Write disabled	R/W

(9) Set the SSU, I^2C bus standby bit, timer RD standby bit, and timer RC standby bit to active.

Module Standby Control Register (MSTCR)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	MSTTRC	MSTTRD	MSTIIC	—	—	—
Setting Value	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	MSTIIC	SSU, I^2C-bus standby bit	0: Active	R/W
b4	MSTTRD	Timer RD standby bit	0: Active	R/W
b5	MSTTRC	Timer RC standby bit	0: Active	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

5. Software

5.1 Function Tables

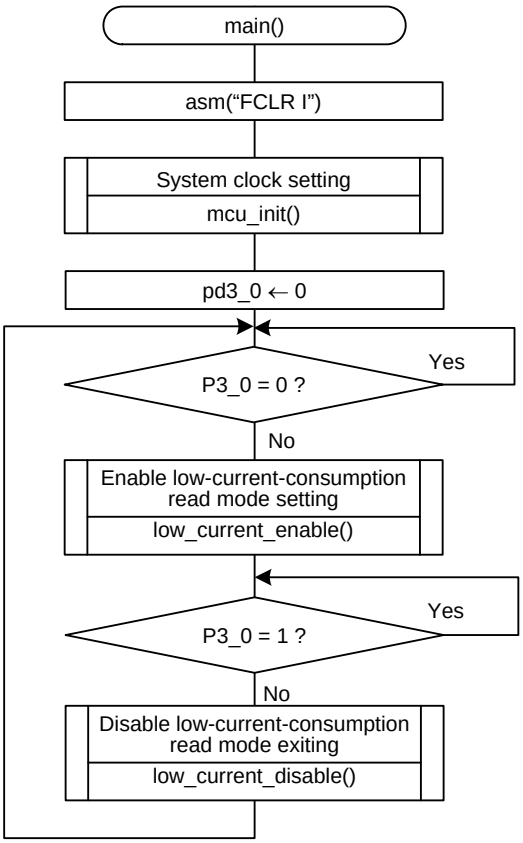
Declaration	void mcu_init (void)		
Outline	System clock setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Set system clock (high-speed on-chip oscillator).		

Declaration	void low_current_enable (void)		
Outline	Setting procedure to enable low-current-consumption read mode		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Switch the system clock to the low-speed on-chip oscillator to enable low-current-consumption read mode.		

Declaration	void low_current_disable (void)		
Outline	Setting procedure to disable low-current-consumption read mode		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Switch the system clock to the high-speed on-chip oscillator after disabling low-current-consumption read mode.		

5.2 Flowcharts

5.2.1 Main Function



Disable interrupts.

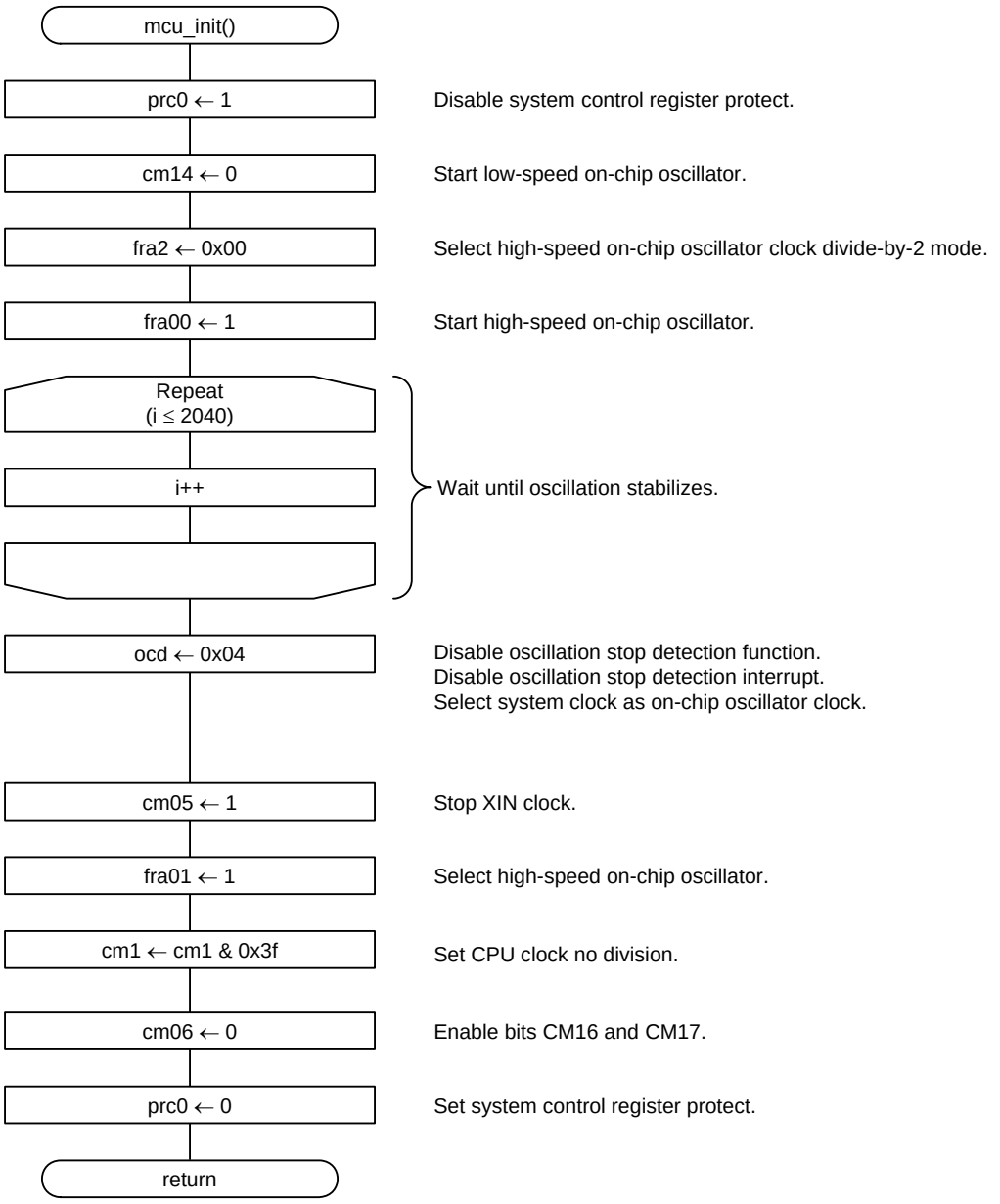
System clock setting (high-speed on-chip oscillator setting)

Set port P3_0 input mode.

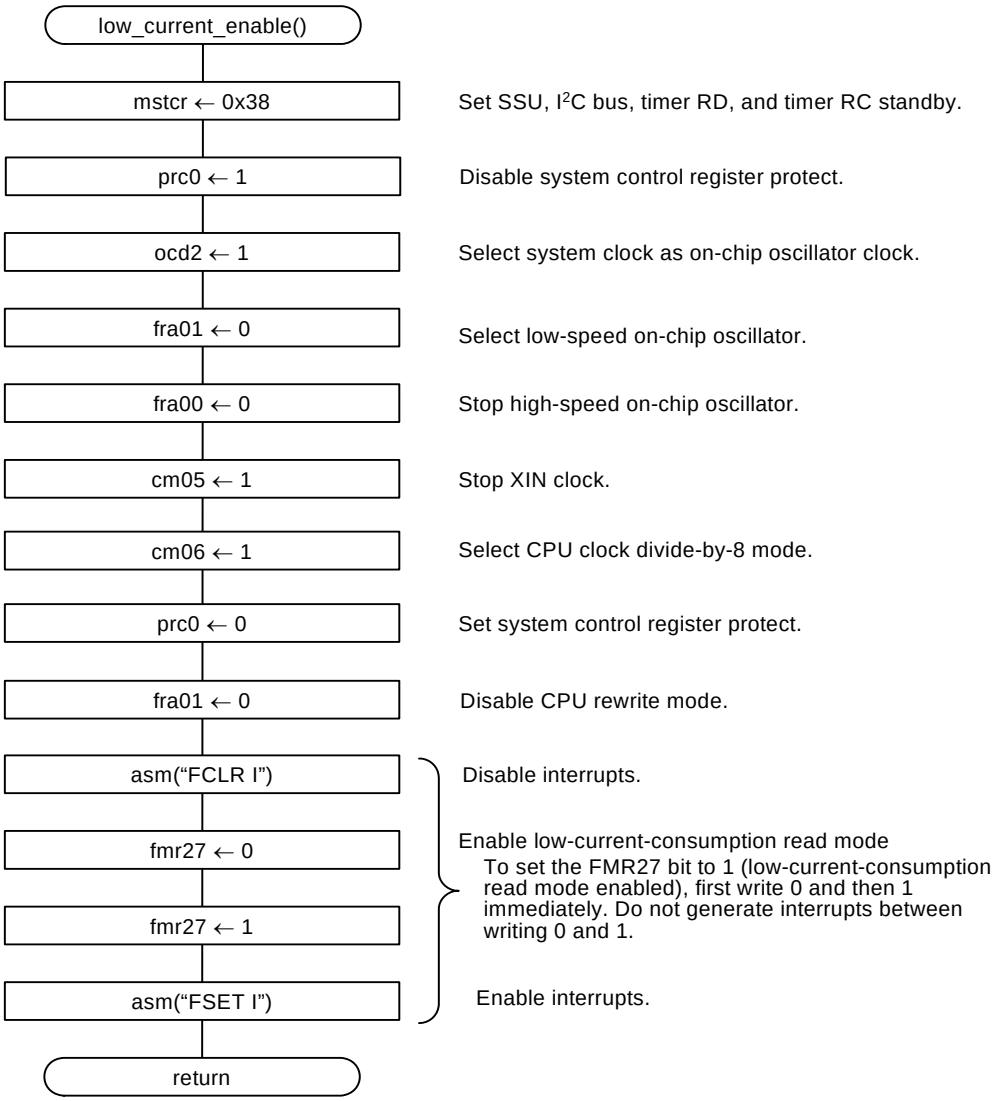
Wait until "H" is input to port P3_0.

Wait until "L" is input to port P3_0.

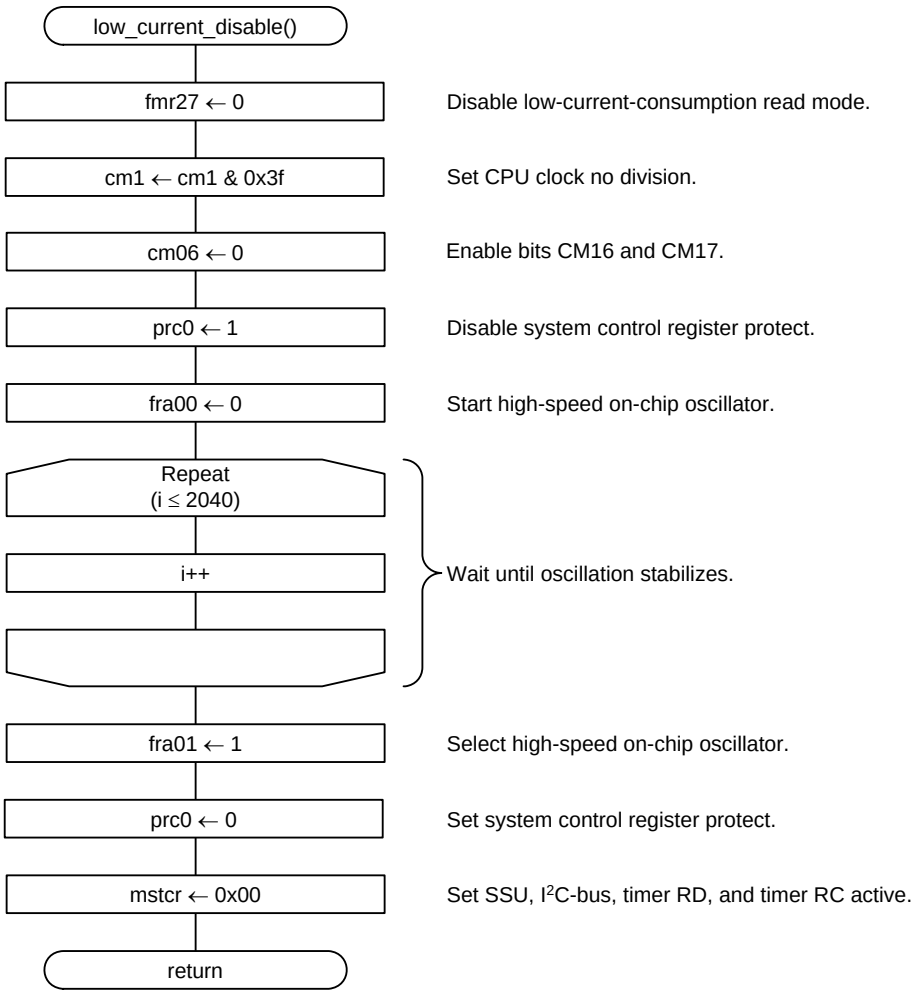
5.2.2 System Clock Setting



5.2.3 Setting Procedure to Enable Low-Current-Consumption Read Mode



5.2.4 Setting Procedure to Disable Low-Current-Consumption Read Mode



6. Sample Program

A sample program can be downloaded from the Renesas Electronics website.
To download, click “Application Notes” in the left-hand side menu of the R8C Family page.

7. Reference Documents

R8C/35C Group User’s Manual: Hardware Rev.1.00
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry

Revision History	R8C/35C Group Flash Memory Low-Current-Consumption Read Mode

Rev.	Date	Description	
		Page	Summary
1.00	Dec. 6, 2010	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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