R8C/2D Group

Clock Synchronous Serial I/O with Chip Select (SSU)

REJ05B1153-0101
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1. Abstract

This document describes a program for clock synchronous serial data communication using clock synchronous serial I/O with chip select (SSU).

2. Introduction

The application example described in this document applies to the following MCU:

- MCU : R8C/2D Group

This program can be used with other R8C/Tiny Series MCUs which have the same special function registers (SFRs) as the R8C/2D Group. Careful evaluation is recommended before using this application note.

3. Application Example

SSU has three modes: clock synchronous communication mode, 4-wire bus communication mode, and bidirectional communication mode. It can use MCUs as a master device and a slave device. This document provides an explanation about each bus communication mode between two MCUs (R8C/2D Group).

In this application example, the master device starts master transmission/reception after an $\overline{\text{INT0}}$ interrupt request is accepted. The slave device waits for data in a receive state until it receives data from the master device.

The following four pins are used during communication:
- SSCK: Clock I/O pin
- SSI: Data I/O pin
- $\overline{\text{SSO}}$: Data I/O pin
- $\overline{\text{SCS}}$: Chip-select I/O pin

When transmitting, the master device outputs a clock from the SSCK pin, data from the SSO pin, and a low signal from the $\overline{\text{SCS}}$ pin. When receiving, it outputs a clock from the SSCK pin, a low signal from the $\overline{\text{SCS}}$ pin, and data from the SSI pin.

Specifications of transmission/reception are as follows:
- Transfer clocks: Internal clock
- Data transfer direction: MSB first
- SSCK clock phase: Change data at odd edge

Figure 3.1 to Figure 3.3 show the connection diagram in each communication mode.

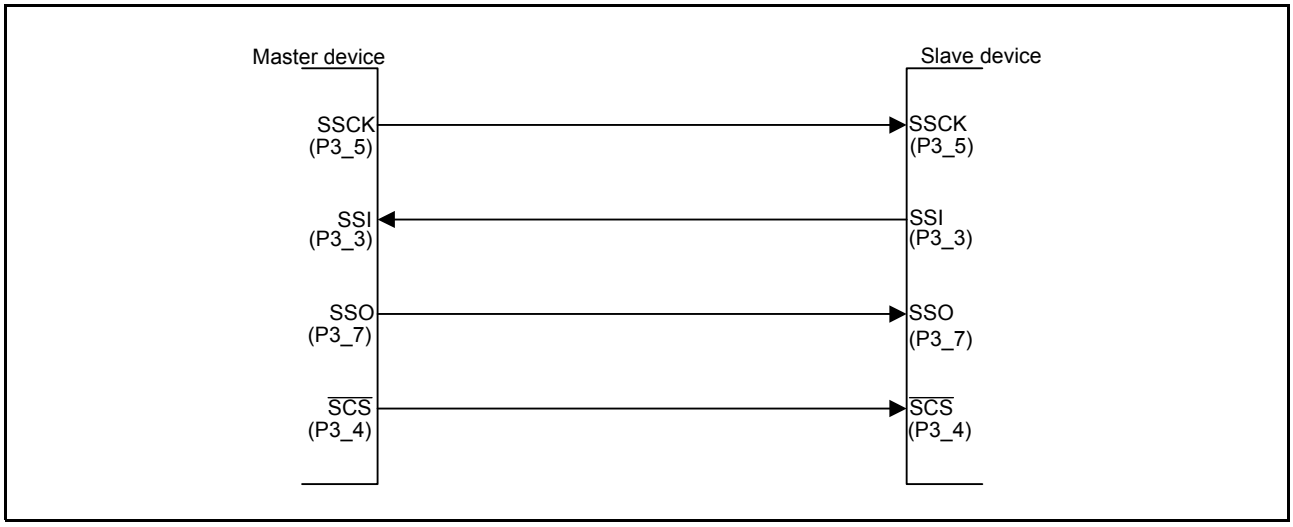


Figure 3.1 Connections in 4-Wire Bus Communication Mode

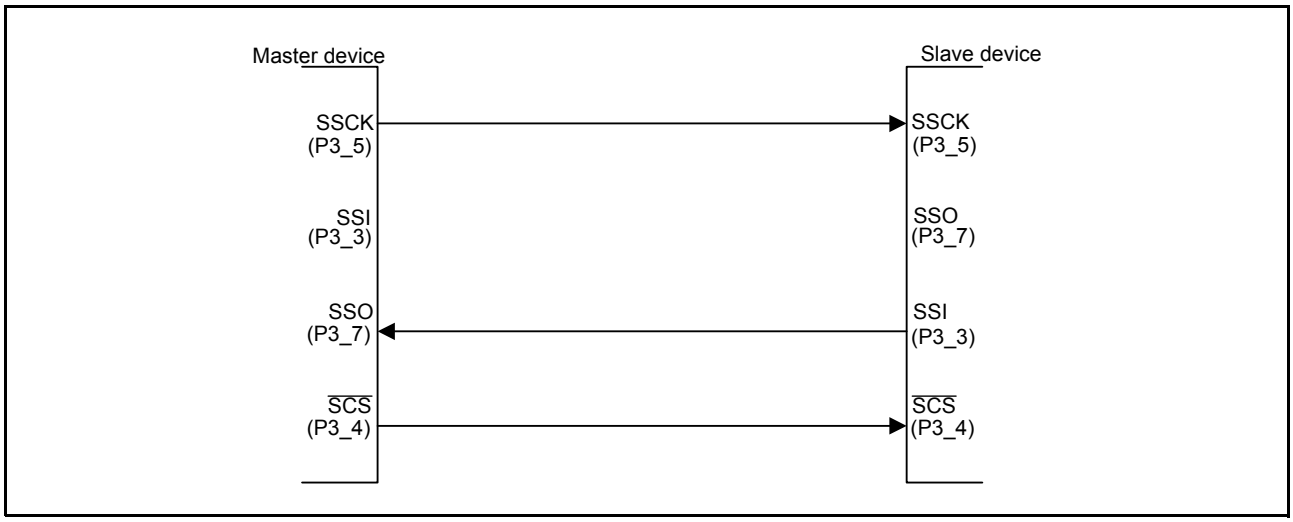


Figure 3.2 Connections in 4-Wire Bus Communication (Bidirectional) Mode

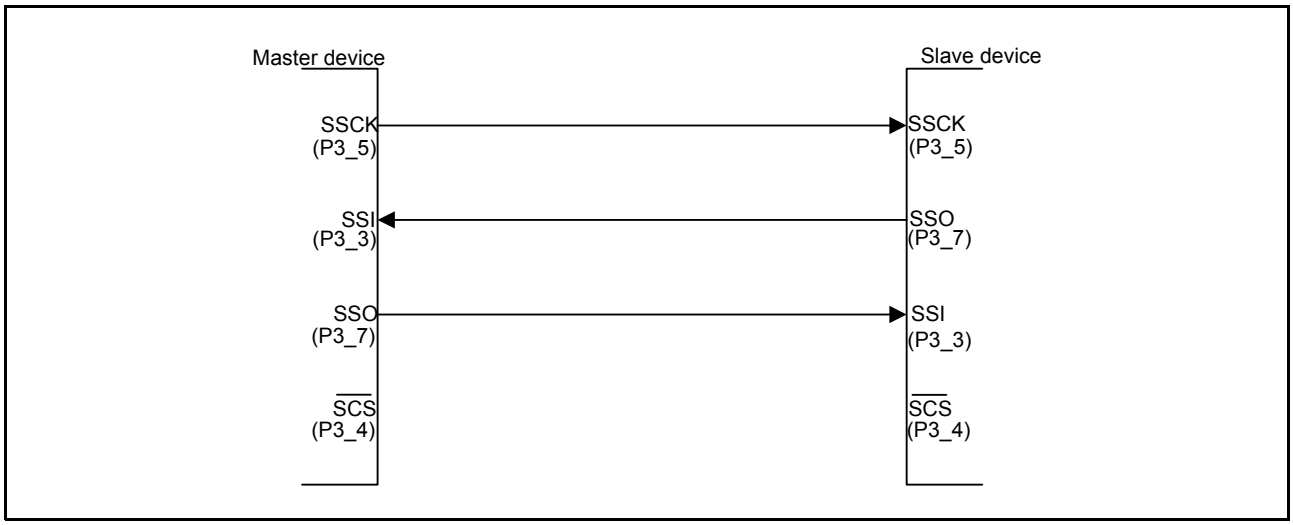


Figure 3.3 Connections in Clock Synchronous Communication Mode

3.1 Pins

Table 3.1 Pin and Function

Pin	I/O	Function
P3_5/SSCK	I/O pin	Clock I/O pin
P3_7/SSO	I/O pin	Data I/O pin
P3_3/SSI	I/O pin	Data I/O pin
P3_4/$\overline{\text{SCS}}$	I/O pin	Chip select I/O pin

3.2 Memory

Table 3.2 Memory

Memory	Size		Remarks
	Master	Slave	
ROM (Program only)	309 bytes	266 bytes	Only in the rej05b1153_src_master.c module or rej05b1153_src_slave.c module
RAM	6 bytes	6 bytes	
Maximum user stack	13 bytes	13 bytes	main function: 7 bytes (master) 7 bytes (slave) sfr_init function: 3 bytes (master) 6 bytes (slave) cs_communication function: 6 bytes
Maximum interrupt stack	0 bytes		Not used

Table 3.3 RAM and Definition (Master Transmit/Receive Mode)

Symbol	Type	Size	Content
_data	unsigned char	3 bytes	Transmit data
_data_store	unsigned char	3 bytes	Receive data

Table 3.4 RAM and Definition (Slave Transmit/Receive Mode)

Symbol	Type	Size	Content
_data	unsigned char	3 bytes	Transmit data
_data_store	unsigned char	3 bytes	Receive data

4. Setup

This section shows the initial setting procedures and values to set the example described in 3. Application Example. Refer to the R8C/2D Group Hardware Manual for details on individual registers.

4.1 Setting the System Clock

(1) Enable writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2.

Protect Register

b7							b0		
							1	PRCR	Address 000Ah
								PRC0	Protect bit 0
									Writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2 is enabled.

(2) Start the low-speed on-chip oscillator.

System Clock Control Register 1

b7							b0		
			0					CM1	Address 0007h
								CM14	Low-speed on-chip oscillation stop bit
									Low-speed on-chip oscillator on

(3) Set the division ratio of the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 2

b7							b0		
0	0	0	0	0	0	0	0	FRA2	Address 0025h
								FRA22 - FRA20	High-speed on-chip oscillator frequency switching bits
									Divide-by-2 mode
								($\overline{b7}$-$\overline{b3}$)	Reserved bits
									Set to 0.

(4) Start the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0

b7							b0		
							1	FRA0	Address 0023h
								FRA00	High-speed on-chip oscillator enable bit
									High-speed on-chip oscillator on

(5)Wait until oscillation stabilizes.

(6) Select the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0

b7							b0
						1	

FRA0 Address 0023h

FRA01 High-speed on-chip oscillator select bit

Selects high-speed on-chip oscillator

(7) Set the system clock division select bits 1.

System Clock Control Register 1

b7							b0
0	0						

CM1 Address 0007h

CM17, CM16 System clock division select bits 1

No division mode

(8) Set the system clock division select bit 0.

System Clock Control Register 0

b7							b0
	0						

CM0 Address 0006h

CM06 System clock division select bit 0

CM16, CM17 enabled

(9) Disable writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2.

Protect Register

b7							b0
							0

PRCR Address 000Ah

PRC0 Protect bit 0

Writing to registers CM0, CM1, OCD, FRA0, FRA1, and FRA2 is disabled.

4.2 Setting $\overline{\text{INT0}}$ Interrupt Request

(1) Set the external input enable register.

External Input Enable Register

b7							b0	
0	0	0	0	0	0	0	1	INTEN Address 00F9h

- INT0EN — $\overline{\text{INT0}}$ input enable bit
  - Enable
- INT0PL — $\overline{\text{INT0}}$ input polarity select bit
  - One edge
- INT1EN — $\overline{\text{INT1}}$ input enable bit
  - Unused bit. Set to 0.
- INT1PL — $\overline{\text{INT1}}$ input polarity select bit
  - Unused bit. Set to 0.
- INT2EN — $\overline{\text{INT2}}$ input enable bit
  - Unused bit. Set to 0.
- INT2PL — $\overline{\text{INT2}}$ input polarity select bit
  - Unused bit. Set to 0.
- INT3EN — $\overline{\text{INT3}}$ input enable bit
  - Unused bit. Set to 0.
- INT3PL — $\overline{\text{INT3}}$ input polarity select bit
  - Unused bit. Set to 0.

(2) Set the $\overline{\text{INT}}$ input filter select register.

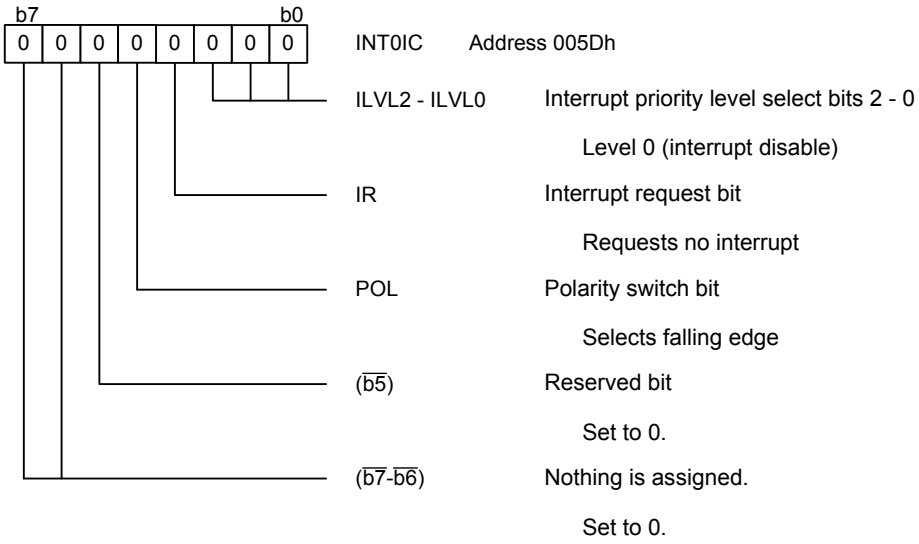
$\overline{\text{INT}}$ Input Filter Select Register

b7							b0	
0	0	0	0	0	0	0	0	INTF Address 00FAh

- INT0F1 - INT0F0 — $\overline{\text{INT0}}$ input filter select bits
  - No filter
- INT1F1 - INT1F0 — $\overline{\text{INT1}}$ input filter select bits
  - Unused bit. Set to 0.
- INT2F1 - INT2F0 — $\overline{\text{INT2}}$ input filter select bits
  - Unused bit. Set to 0.
- INT3F1 - INT3F0 — $\overline{\text{INT3}}$ input filter select bits
  - Unused bit. Set to 0.

(3) Set the INT0 interrupt control register.

INT0 Interrupt Control Register



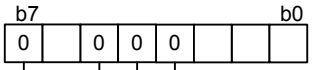
4.3 Setting Master Transmit/Receive Mode

4.3.1 Initial Setting

Enable transferring and set the transfer clock and transfer format.

(1) Set the port P3_7, P3_5, P3_4, and P3_3 direction bits as input ports.

Port P3 Direction Register



PD3 Address 00E7h

PD3_3 Port P3_3 direction bit
Input mode

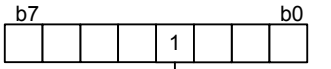
PD3_4 Port P3_4 direction bit
Input mode

PD3_5 Port P3_5 direction bit
Input mode

PD3_7 Port P3_7 direction bit
Input mode

(2) Set the SSU bus operation enable bit.

Module Operation Enable Register

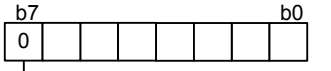


MSTCR Address 0008h

MSTIIC SSU, I²C bus operation enable bit
Enable

(3) Set the SSU/I²C bus switch bit.

Port Mode Register

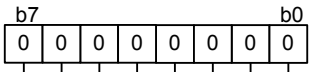


PMR Address 00F8h

IICSEL SSU / I²C bus switch bit
Selects SSU function

(4) Disable reception and transmission.

SS Enable Register



SSER Address 00BBh

CEIE Conflict error interrupt enable bit
Disables conflict error interrupt request

($\overline{b2}$-$\overline{b1}$) Nothing is assigned.
Set to 0.

RE Receive enable bit
Disables receive

TE Transmit enable bit
Disables transmit

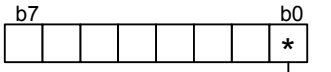
RIE Receive interrupt enable bit
Disables receive data full and overrun error interrupt request

TEIE Transmit end interrupt enable bit
Disables transmit end interrupt request

TIE Transmit interrupt enable bit
Disables transmit data empty interrupt request

(5) Select the communication mode.

SS Mode Register 2

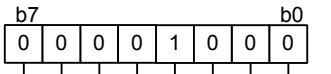


SSMR2 Address 00BDh

SSUMS Clock synchronous serial I/O with chip select mode select bit
- Set to 1 to use 4-wire bus communication mode or bidirectional communication mode.
- Set to 0 to use clock synchronous communication mode.

(6) Select MSB first.

SS Mode Register

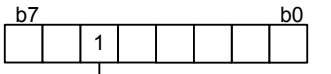


SSMR Address 00BAh

BC2 - BC0	Bits counter 2 to 0
	Unused bit. Set to 0.
($\overline{b3}$)	Reserved bit
	Set to 1.
($\overline{b4}$)	Nothing is assigned.
	Set to 0.
CPHS	SSCK clock phase select bit
	Change data at odd edge (download data at even edge)
CPOS	SSCK clock polarity select bit
	High when clock stops
MLS	MSB first/LSB first select bit
	Transfers data MSB first

(7) Select master device.

SS Control Register H

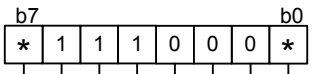


SSCRH Address 00B8h

MSS	Master/slave device select bit
	Operates as master device

(8) Set the bidirectional mode enable bit, SSCK pin select bit, and $\overline{SCS}$ pin select bit.

SS Mode Register 2

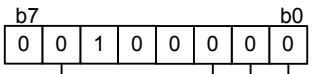


SSMR2 Address 00BDh

SSUMS	Clock synchronous serial I/O with chip select mode select bit • Set to 1 to use 4-wire bus communication mode or bidirectional communication mode. • Set to 0 to use clock synchronous communication mode.
CSOS	$\overline{SCS}$ pin open drain output select bit Unused bit. Set to 0.
SOOS	Serial data pin open output drain select bit Unused bit. Set to 0.
SCKOS	SSCK pin open drain output select bit Unused bit. Set to 0.
CSS1 - CSS0	$\overline{SCS}$ pin select bits Functions as $\overline{SCS}$ output pin (Functions as a port, regardless of the values of the bits when using clock synchronous communication mode).
SCKS	SSCK pin select bit Functions as serial clock pin
BIDE	Bidirectional mode enable bit • Set to 1 to use bidirectional communication mode. • Set to 0 to use 4-wire bus communication mode or clock synchronous communication mode.

(9) Set the RSSTP bit and transfer clock rate select bits.

SS Control Register H

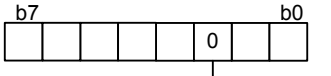


SSCRH Address 00B8h

CKS2 - CKS0	Transfer clock rate select bits f1/256
RSSTP	Receive single stop bit Maintains receive operation after receiving 1 byte of data

(10) Set the ORER bit in the SSSR register to 0.

SS Status Register



SSSR Address 00BCh

ORER	Overrun error flag No overrun errors generated

(11) Enable transmission and disable reception.

SS Enable Register

b7							b0		
0	0	0	1	0	0	0	0	SSER	Address 00BBh

CEIE	Conflict error interrupt enable bit Disables conflict error interrupt request
($\overline{b2}$-$\overline{b1}$)	Nothing is assigned. Set to 0.
RE	Receive enable bit Disables receive
TE	Transmit enable bit Enables transmit
RIE	Receive interrupt enable bit Disables receive data full and overrun error interrupt request
TEIE	Transmit end interrupt enable bit Disables transmit end interrupt request
TIE	Transmit interrupt enable bit Disables transmit data empty interrupt request

4.3.2 Master Transmission

(1) Read the TDRE bit in the SSSR register to confirm that the TDRE bit is 1 (data is transferred from the SSTDR register to the SSTRSR register).

(2) After confirming that the TDRE bit is 1, write transmit data to the SSTDR register. When data is written to the SSTDR register, the TDRE bit becomes 0 (data is not transferred from the SSTDR register to the SSTRSR register), and the data is transferred from the SSTDR register to the SSTRSR register. Then, the TDRE bit becomes 1 and data transmission starts.

SS Transmit Data Register

b7							b0		
								SSTDR	Address 00BEh
									Write transmit data

(3) After the second byte of the transmit data, write to the SSTDR register each time the TDRE bit becomes 1.

(4) The TEND bit in the SSSR register becomes 1 when data transmission is completed.

(5) Set the TEND bit in the SSSR register to 0.

SS Status Register

b7							b0		
	0							SSSR	Address 00BCh
								TEND	Transmit end The TDRE bit is set to 0 when transmitting the last bit of transmit data

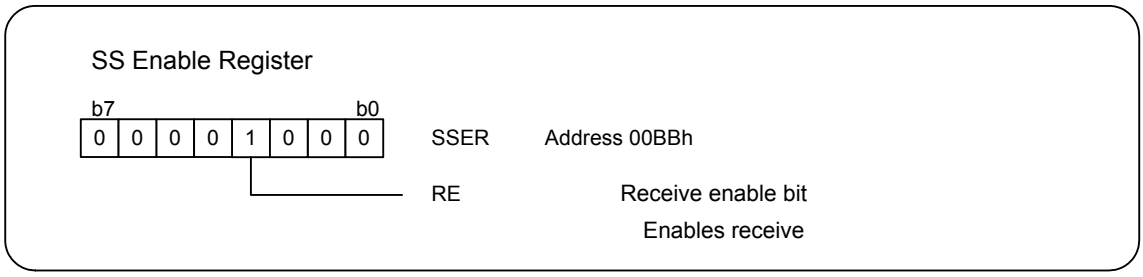
(6) Disable transmission.

SS Enable Register

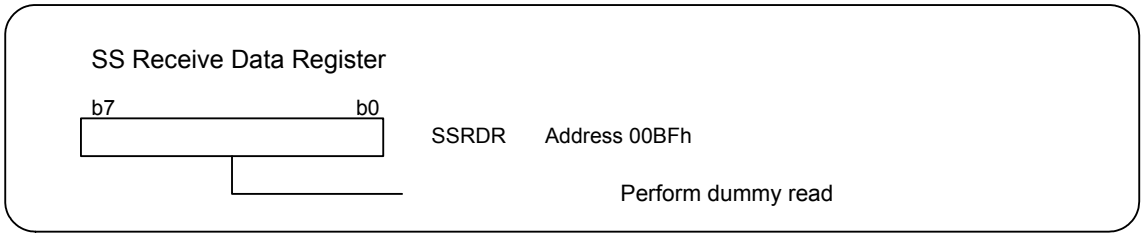
b7							b0		
0	0	0	0	0	0	0	0	SSER	Address 00BBh
								TE	Transmit enable bit Disables transmit

4.3.3 Master Reception

(1) Enable receiption.



(2) Perform a dummy read on the SSRDR register.

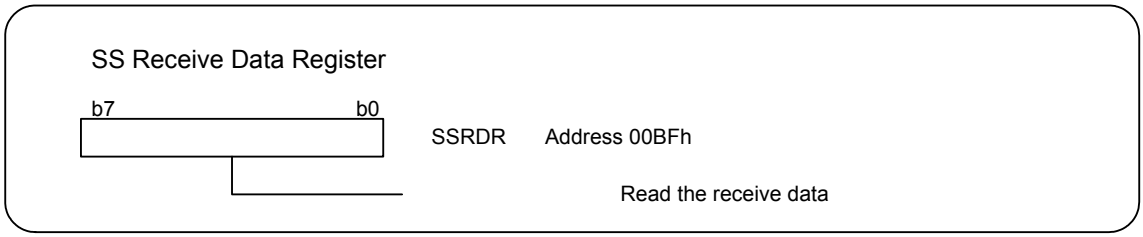


(3) Determine whether the receive data is the last data. If so, jump to the procedure in 4.3.4 Master Reception (When Receiving the Last Byte).

(4) Confirm that the ORER bit in the SSSR register is 0 (no overrun errors generated) to determine if an overrun error occurred. If an overrun error occurred, jump to the procedure in 4.3.5 Master Reception (Overrun Error).

(5) Read the RDRF bit in the SSSR register and confirm that the RDRF bit is 1 (data present in the SSRDR register).

(6) After confirming that the RDRF bit is 1, read the receive data from the SSRDR register. After reading the receive data from the SSRDR register, the RDRF bit becomes 0 (no data present in the SSRDR register).



4.3.4 Master Reception (When Receiving the Last Byte)

(1) Set the RSSTP bit in the SS control register H to 1.

SS Control Register H

b7							b0
0	1	1	0	0	0	0	0

SSCRH Address 00B8h

RSSTP Receive single stop bit
Completes receive operation after receiving 1 byte of data

(2) Confirm that the ORER bit in the SSSR register is 0 (no overrun errors generated) to determine if an overrun error occurred. If an overrun error occurred, jump to the procedure in 4.3.5 Master Reception (Overrun Error).

(3) Read the RDRF bit in the SSSR register and confirm that the RDRF bit is 1 (data present in the SSRDR register).

(4) Set the RSSTP bit in the SS control register H to 0.

SS Control Register H

b7							b0
0	0	1	0	0	0	0	0

SSCRH Address 00B8h

RSSTP Receive single stop bit
Maintains receive operation after receiving 1 byte of data

(5) Disable reception.

SS Enable Register

b7							b0
0	0	0	0	0	0	0	0

SSER Address 00BBh

RE Receive enable bit
Disables receive

(6) Read the receive data from the SSRDR register. The RDRF bit becomes 0.

SS Receive Data Register

b7							b0

SSRDR Address 00BFh

Read the receive data

(7) Next, enable the master transmission.

SS Enable Register

b7							b0	
0	0	0	1	0	0	0	0	SSER

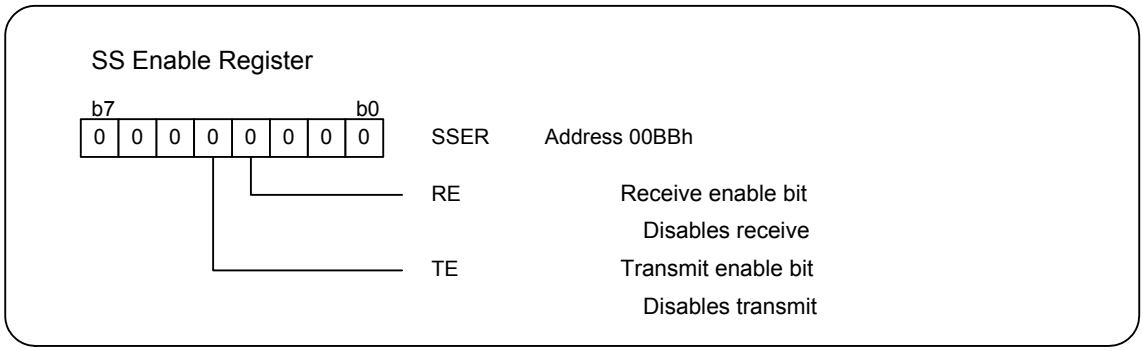
Address 00BBh

TE — Transmit enable bit

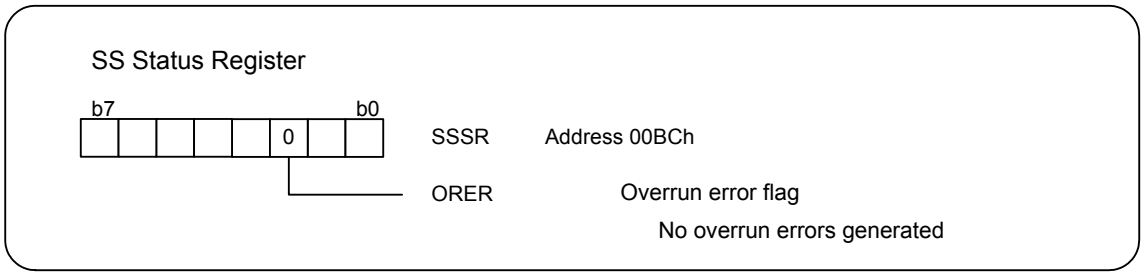
Enables transmit

4.3.5 Master Reception (Overrun Error)

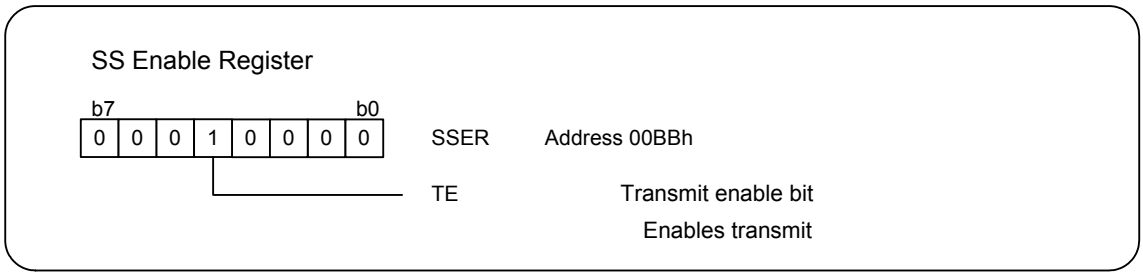
(1) Disable reception and transmission.



(2) Set the ORER bit in the SSSR register to 0.



(3) Next, enable the master transmission.



4.4 Setting Slave Transmit/Receive Mode

4.4.1 Initial Setting

Enable transferring and set the transfer clock and transfer format.

(1) Set the port P3_7, P3_5, P3_4, and P3_3 direction bits as input ports.

Port P3 Direction Register

b7							b0		
0		0	0	0				PD3	Address 00E7h
								PD3_3	Port P3_3 direction bit Input mode
								PD3_4	Port P3_4 direction bit Input mode
								PD3_5	Port P3_5 direction bit Input mode
								PD3_7	Port P3_7 direction bit Input mode

(2) Set the SSU bus operation enable bit.

Module Operation Enable Register

b7							b0		
				1				MSTCR	Address 0008h
								MSTIIC	SSU, I²C bus operation enable bit Enable

(3) Set SSU/I²C bus switch bit.

Port Mode Register

b7							b0		
0								PMR	Address 00F8h
								IICSEL	SSU / I²C bus switch bit Selects SSU function

(4) Disable reception and transmission.

SS Enable Register

b7							b0		
0	0	0	0	0	0	0	0	SSER	Address 00BBh
								CEIE	Conflict error interrupt enable bit Disables conflict error interrupt request
								($\overline{b2}$-$\overline{b1}$)	Nothing is assigned. Set to 0.
								RE	Receive enable bit Disables receive
								TE	Transmit enable bit Disables transmit
								RIE	Receive interrupt enable bit Disables receive data full and overrun error interrupt request
								TEIE	Transmit end interrupt enable bit Disables transmit end interrupt request
								TIE	Transmit interrupt enable bit Disables transmit data empty interrupt request

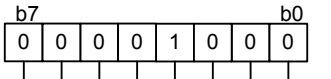
(5) Select the communication mode.

SS Mode Register 2

b7							b0		
							*	SSMR2	Address 00BDh
								SSUMS	Clock synchronous serial I/O with chip select mode select bit • Set to 1 to use 4-wire bus communication mode or bidirectional communication mode. • Set to 0 to use clock synchronous communication mode.

(6) Select MSB first.

SS Mode Register

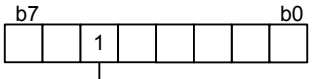


SSMR Address 00BAh

BC2 - BC0	Bits counter 2 to 0 Unused bit. Set to 0.
($\overline{b3}$)	Reserved bit Set to 1.
($\overline{b4}$)	Nothing is assigned. Set to 0.
CPHS	SSCK clock phase select bit Change data at odd edge (download data at even edge)
CPOS	SSCK clock polarity select bit High when clock stops
MLS	MSB first/LSB first select bit Transfers data MSB first

(7) Select the slave device.

SS Control Register H

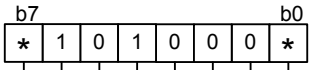


SSCRH Address 00B8h

MSS	Master/slave device select bit Operates as master device

(8) Set the bidirectional mode enable bit, SSCK pin select bit, and $\overline{SCS}$ pin select bit.

SS Mode Register 2

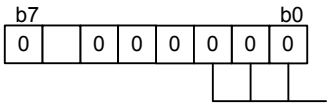


SSMR2 Address 00BDh

SSUMS	Clock synchronous serial I/O with chip select mode select bit • Set to 1 to use 4-wire bus communication mode or bidirectional communication mode. • Set to 0 to use clock synchronous communication mode.
CSOS	$\overline{SCS}$ pin open drain output select bit Unused bit. Set to 0.
SOOS	Serial data pin open output drain select bit Unused bit. Set to 0.
SCKOS	SSCK pin open drain output select bit Unused bit. Set to 0.
CSS1 - CSS0	$\overline{SCS}$ pin select bits Functions as $\overline{SCS}$ input pin (Functions as a port, regardless of the values of the bits when using clock synchronous communication mode).
SCKS	SSCK pin select bit Functions as serial clock pin
BIDE	Bidirectional mode enable bit • Set to 1 to use bidirectional communication mode. • Set to 0 to use 4-wire bus communication mode or clock synchronous communication mode

(9) Set the transfer clock rate select bits.

SS Control Register H

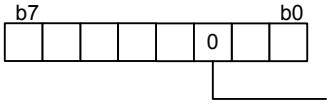


SSCRH Address 00B8h

CKS2 - CKS0	Transfer clock rate select bits f1/256

(10) Set the ORER bit in the SSSR register to 0.

SS Status Register



SSSR Address 00BCh

ORER	Overrun error flag No overrun errors generated

(11) Disable transmission and enable reception.

SS Enable Register

b7							b0		
0	0	0	0	1	0	0	0	SSER	Address 00BBh

CEIE	Conflict error interrupt enable bit Disables conflict error interrupt request
($\overline{b2}$-$\overline{b1}$)	Nothing is assigned. Set to 0.
RE	Receive enable bit Enables receive
TE	Transmit enable bit Disables transmit
RIE	Receive interrupt enable bit Disables receive data full and overrun error interrupt request
TEIE	Transmit end interrupt enable bit Disables transmit end interrupt request
TIE	Transmit interrupt enable bit Disables transmit data empty interrupt request

(12) Perform a dummy read on the SSRDR register.

SS Receive Data Register

b7	b0		
		SSRDR	Address 00BFh

Perform dummy read

4.4.2 Slave Reception

(1) Confirm that the ORER bit in the SSSR register is 0 (no overrun errors generated) to determine if an overrun error occurred. If an overrun error occurred, jump to the procedure in 4.4.3 Slave Reception (Overrun Error).

(2) Read the RDRF bit in the SSSR register and confirm that the RDRF bit is 1 (data present in the SSRDR register).

(3) After confirming that the RDRF bit is 1, read the receive data from the SSRDR register. After reading the receive data from the SSRDR register, the RDRF bit becomes 0 (no data present in the SSRDR register).

SS Receive Data Register

b7							b0		
								SSRDR	Address 00BFh
									Read the receive data

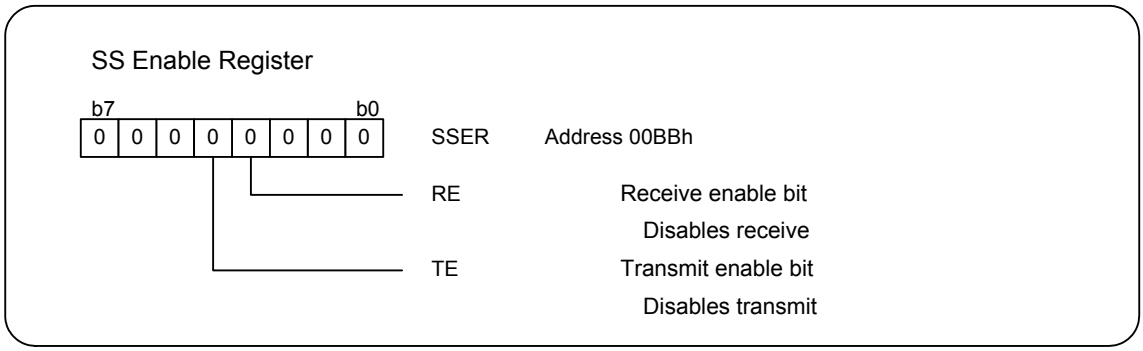
(4) After reading the last byte of the data to be received, disable receiption.

SS Enable Register

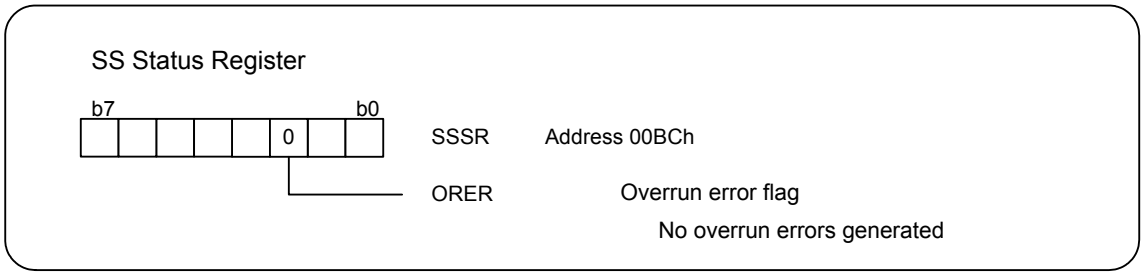
b7							b0		
0	0	0	0	0	0	0	0	SSER	Address 00BBh
								RE	Receive enable bit
									Disables receive

4.4.3 Slave Reception (Overrun Error)

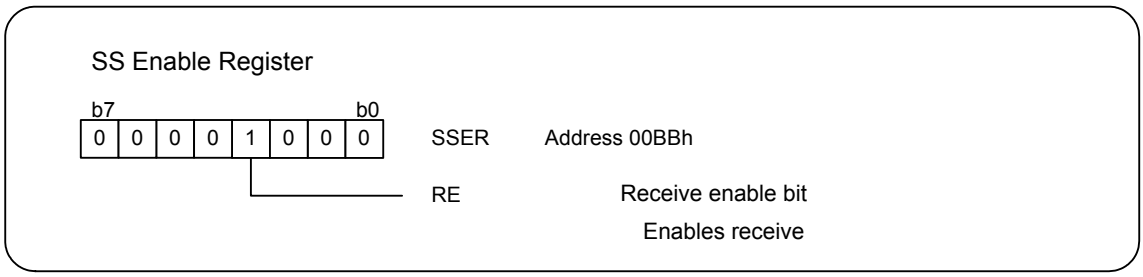
(1) Disable reception and transmission.



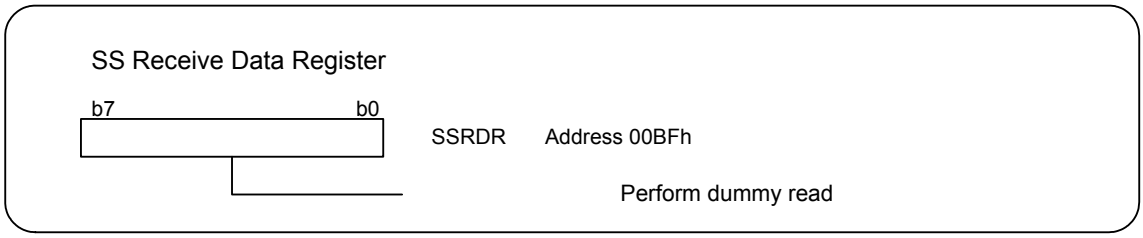
(2) Set the ORER bit in the SSSR register to 0.



(3) Enable receiption.

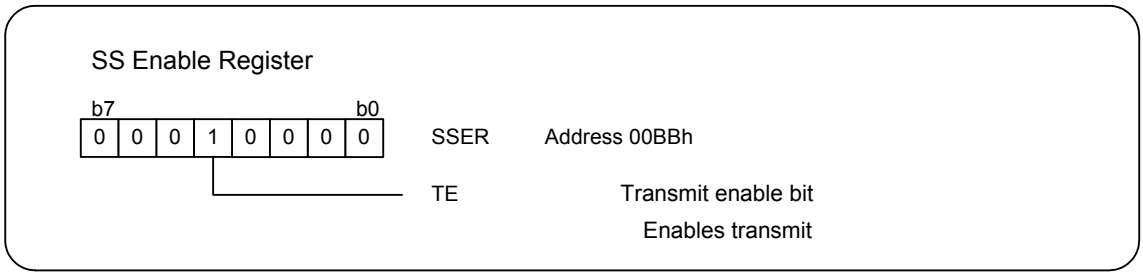


(4) Perform a dummy read on the SSRDR register.



4.4.4 Slave Transmission

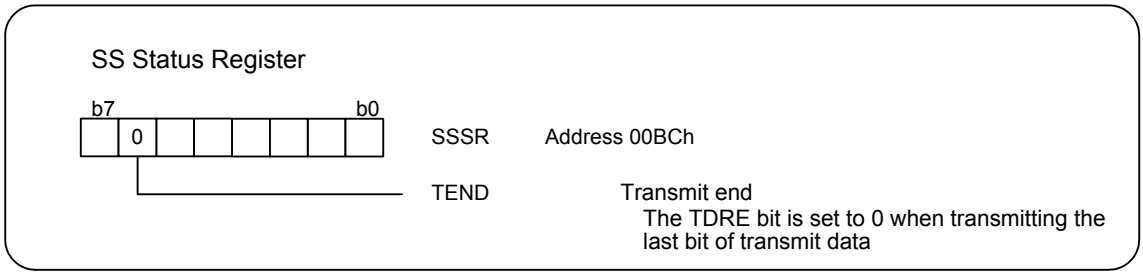
(1) Enable transmission.



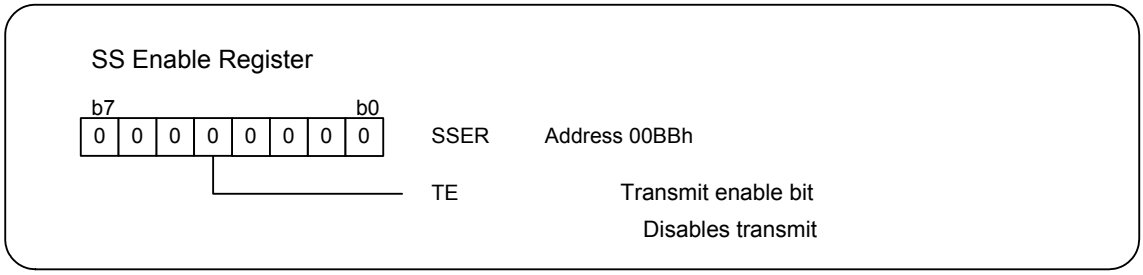
(2) Write the transmit data to the SSTDR register. When data is written to the SSTDR register, the TDRE bit in the SSSR register becomes 0 (data is not transferred from the SSTDR register to the SSTRSR register), and the data is transferred from the SSTDR register to the SSTRSR register. Then, the TDRE bit becomes 1 (data is transferred from the SSTDR register to the SSTRSR register), and data transmission starts.

(3) The TEND bit in the SSSR register becomes 1 (the TDRE bit is 1 when transmitting the last bit of transmit data) when data transmission is completed. After the second byte of the transmit data, write to the SSTDR register after confirming that the TDRE bit is 1.

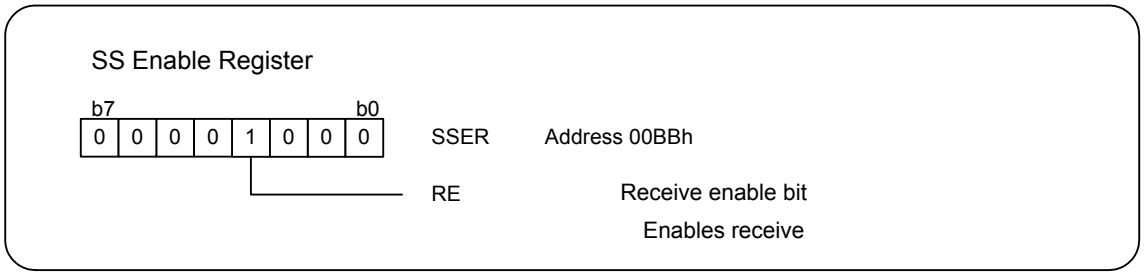
(4) After transmitting a specified number of bytes, check that the TEND bit in the SSSR register is 1 to confirm completion of data transmission. Set the TEND bit in the SSSR register to 0.



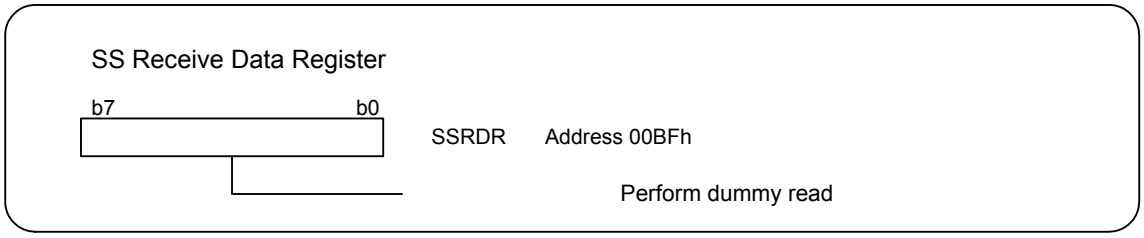
(5) Disable transmission.



(6) Next, enable the slave receiption.



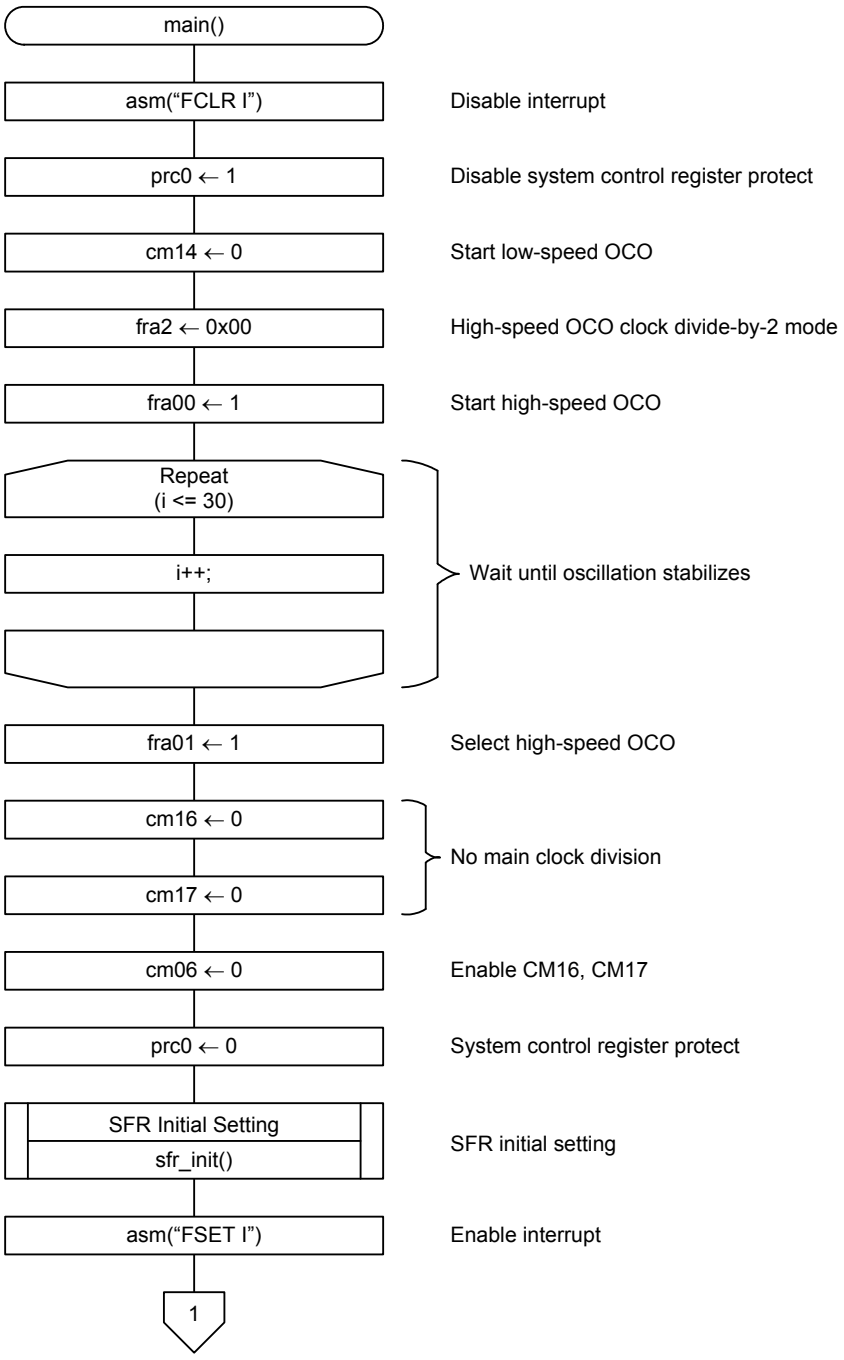
(7) Perform a dummy read on the SSRDR register.

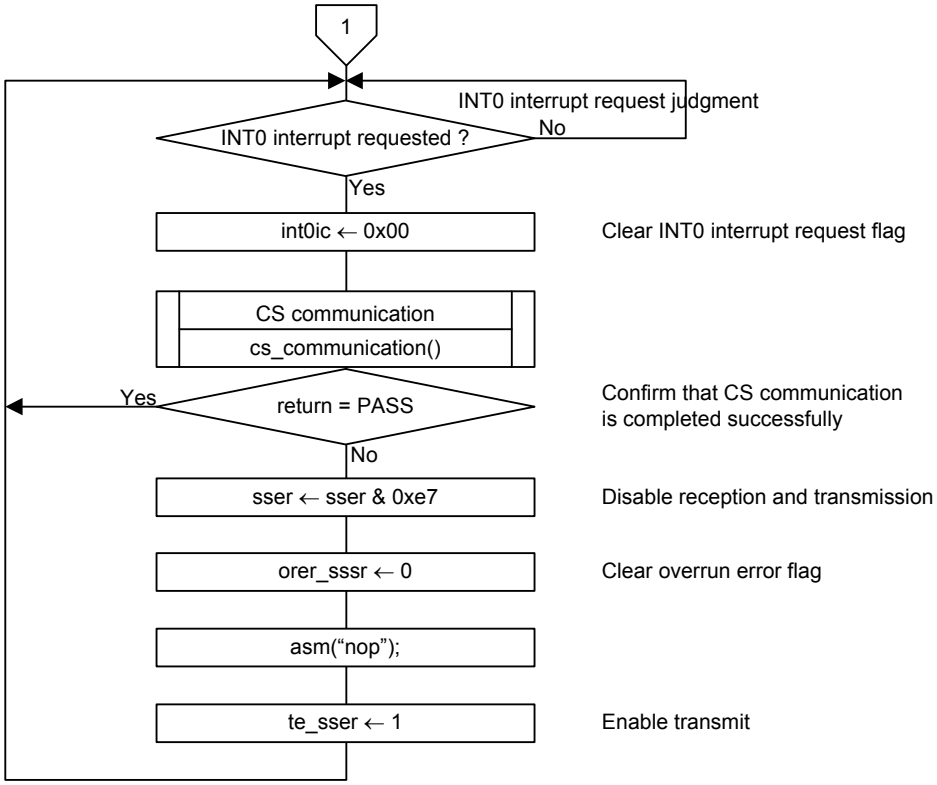


5. Flowcharts

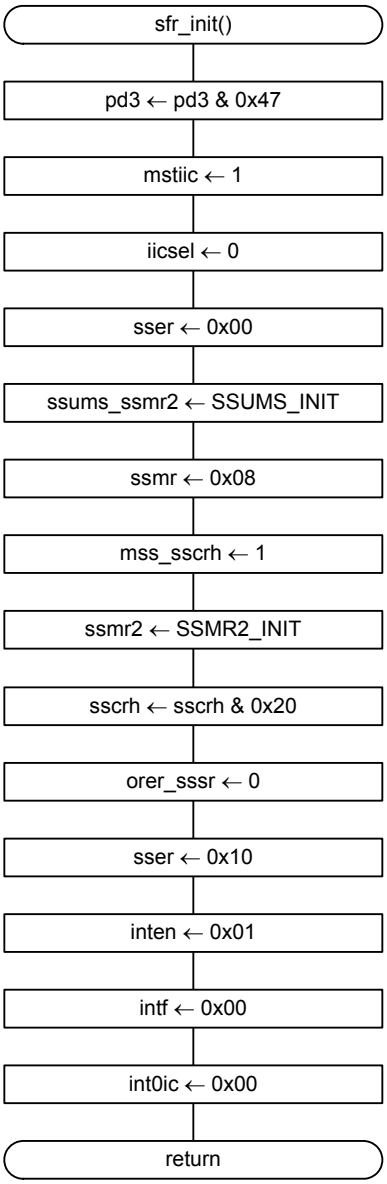
5.1 Master Transmit/Receive Mode

5.1.1 Initial Setting and Main Loop




1
INT0 interrupt request judgment
INT0 interrupt requested ?
No
Yes
int0ic ← 0x00
Clear INT0 interrupt request flag
CS communication
cs_communication()
Yes
return = PASS
Confirm that CS communication is completed successfully
No
sser ← sser & 0xe7
Disable reception and transmission
orer_sssr ← 0
Clear overrun error flag
asm("nop");
te_sser ← 1
Enable transmit

5.1.2 SFR Initial Setting



P3_7(SSO), P3_5(SSCK), P3_4(SCS), P3_3(SSI) input mode setting

Enable SSU operation

Select SSU function

Disable transmission and reception

Mode setting (1)

MSB first setting

Select master device

Set to bidirectional mode enable, SSCK pin select, and $\overline{SCS}$ pin select (2)

Set to maintains receive operation after receiving 1 byte of data and f1/256

Clear overrun error flag

Enable transmission
Disable reception and interrupt request

Select $\overline{INT0}$ input enable and $\overline{INT0}$ input polarity one edge

No $\overline{INT0}$ input filter

Disable INT0 interrupt, clear INT0 interrupt request flag, and select $\overline{INT0}$ input polarity falling edge

Note 1. SSUMS_INIT value in each mode is deified as below.

4-wire bus communication mode: 1

Bidirectional communication mode: 1

Clock synchronous communication mode: 0

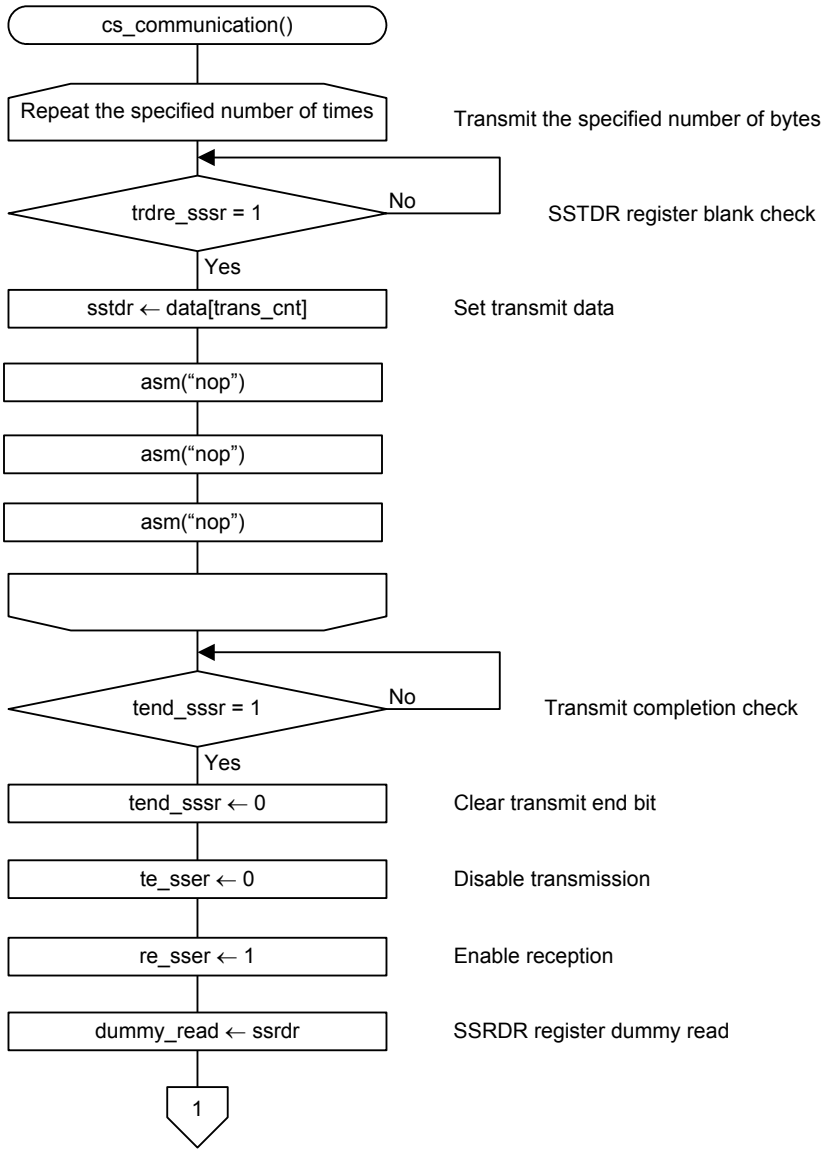
Note 2. SSMR2_INIT value in each mode is deified as below.

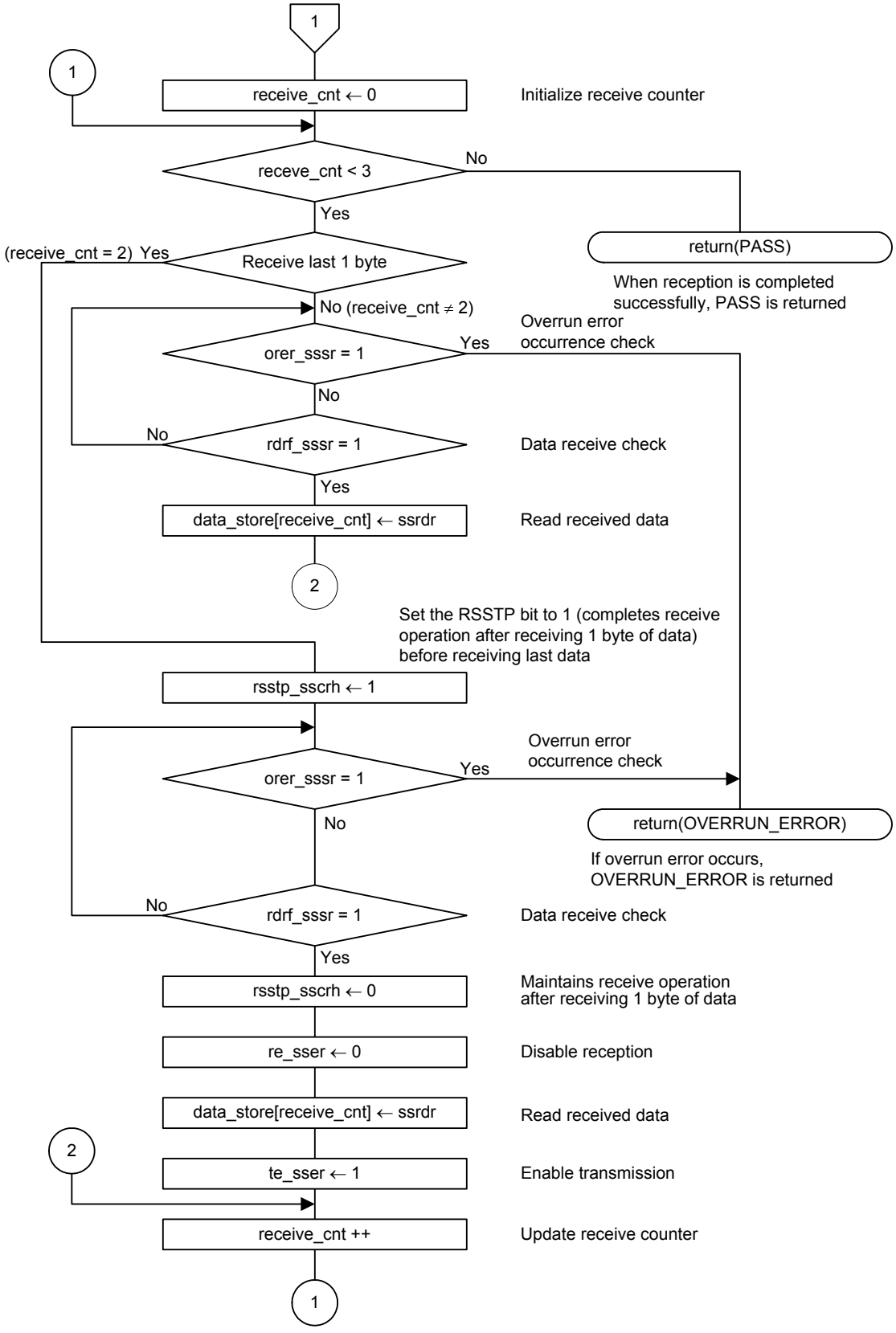
4-wire bus communication mode: 0x71

Bidirectional communication mode: 0xf1

Clock synchronous communication mode: 0x40

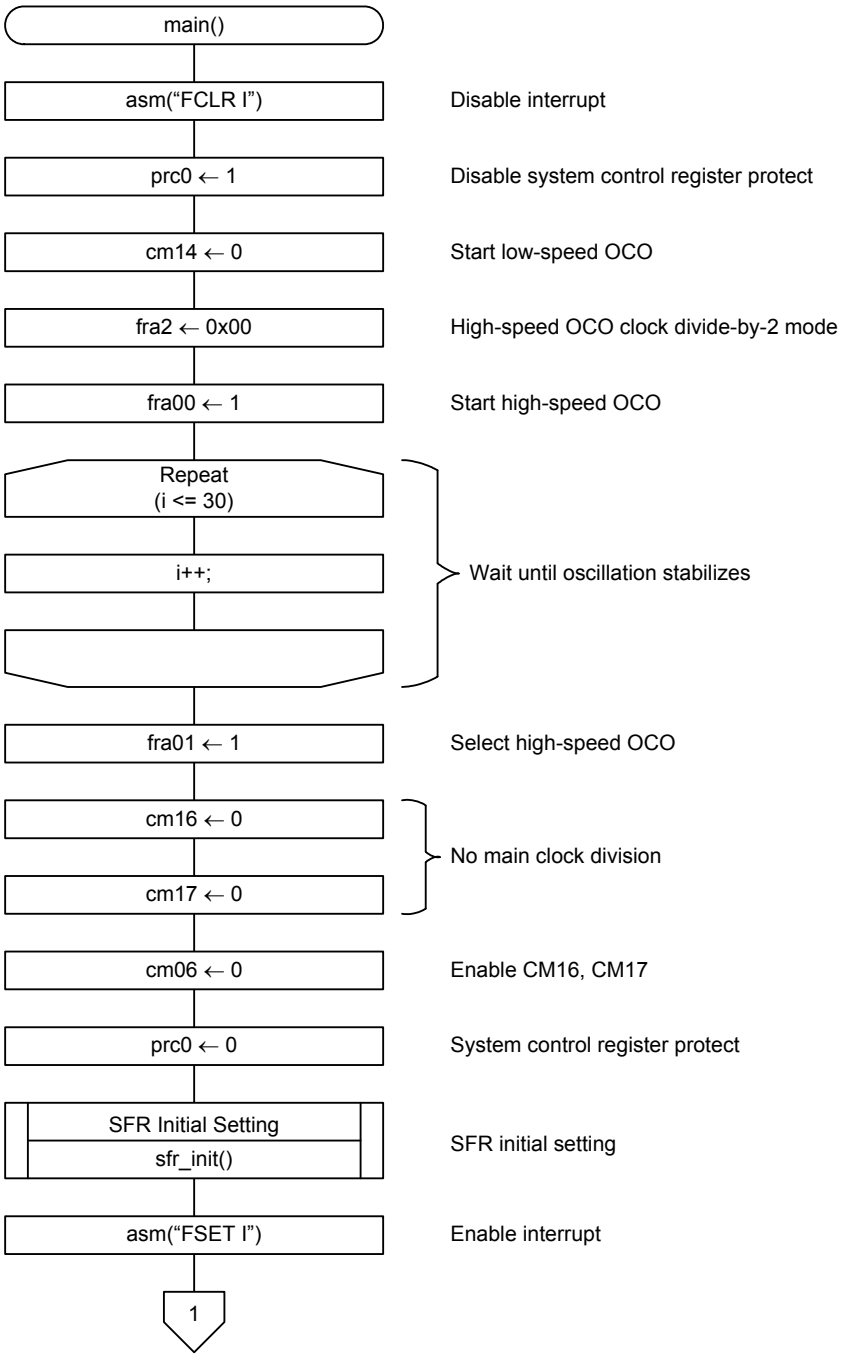
5.1.3 CS Communication Main Routine

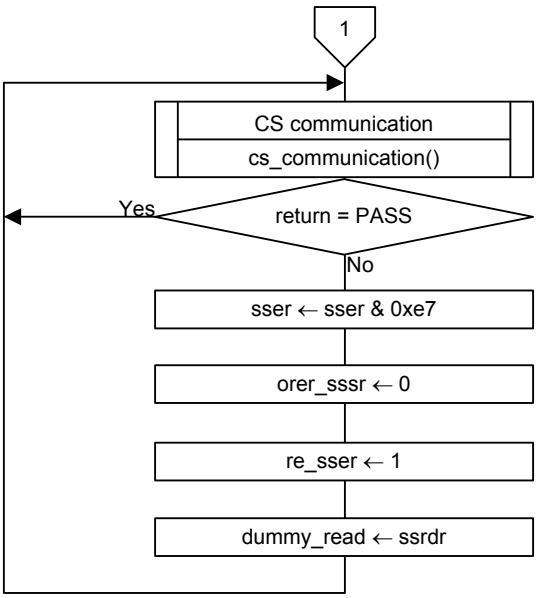



1
1
receive_cnt ← 0
Initialize receive counter
receve_cnt < 3
No
Yes
return(PASS)
When reception is completed successfully, PASS is returned
(receive_cnt = 2) Yes
Receive last 1 byte
No (receive_cnt ≠ 2)
Overrun error occurrence check
orer_sssr = 1
Yes
No
No
rdrf_sssr = 1
Data receive check
Yes
data_store[receive_cnt] ← ssrdr
Read received data
2
Set the RSSTP bit to 1 (completes receive operation after receiving 1 byte of data) before receiving last data
rsstp_sscrh ← 1
Overrun error occurrence check
orer_sssr = 1
Yes
No
return(OVERRUN_ERROR)
If overrun error occurs, OVERRUN_ERROR is returned
No
rdrf_sssr = 1
Data receive check
Yes
rsstp_sscrh ← 0
Maintains receive operation after receiving 1 byte of data
re_sser ← 0
Disable reception
data_store[receive_cnt] ← ssrdr
Read received data
2
te_sser ← 1
Enable transmission
receive_cnt ++
Update receive counter
1

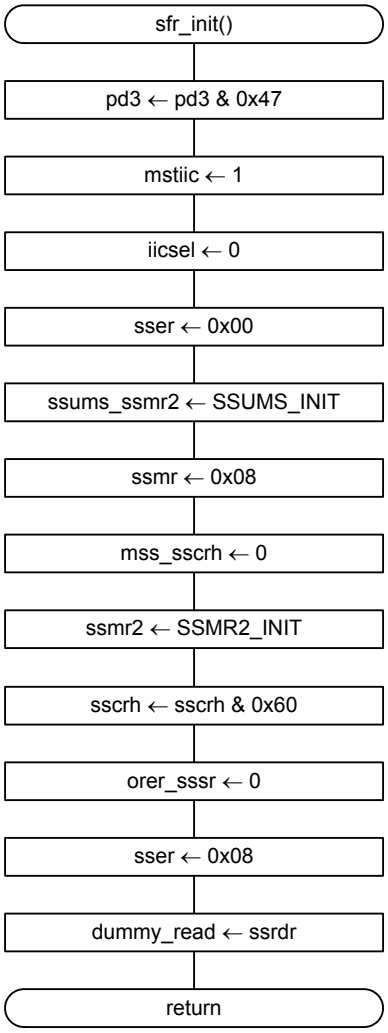
5.2 Slave Transmit/Receive Mode

5.2.1 Initial Setting and Main Loop




1
CS communication
cs_communication()
Yes
return = PASS
No
sser ← sser & 0xe7
orer_sssr ← 0
re_sser ← 1
dummy_read ← ssrdr
Confirm that CS communication is completed successfully
Disable reception and transmission
Clear overrun error flag
Enable transmit
SSRDR register dummy read

5.2.2 SFR Initial Setting



P3_7(SSO), P3_5(SSCK), P3_4($\overline{SCS}$), P3_3(SSI) input mode setting

Enable SSU operation

Select SSU function

Disable transmission and reception

Mode setting (1)

MSB first setting

Select slave device

Set bidirectional mode enable, SSCK pin select, and $\overline{SCS}$ pin select (2)

Set f1/256

Clear overrun error flag

Disable transmission and interrupt request
Enable reception

SSRDR register dummy read

Note 1. SSUMS_INIT value in each mode is deified as below.

4-wire bus communication mode: 1

Bidirectional communication mode: 1

Clock synchronous communication mode: 0

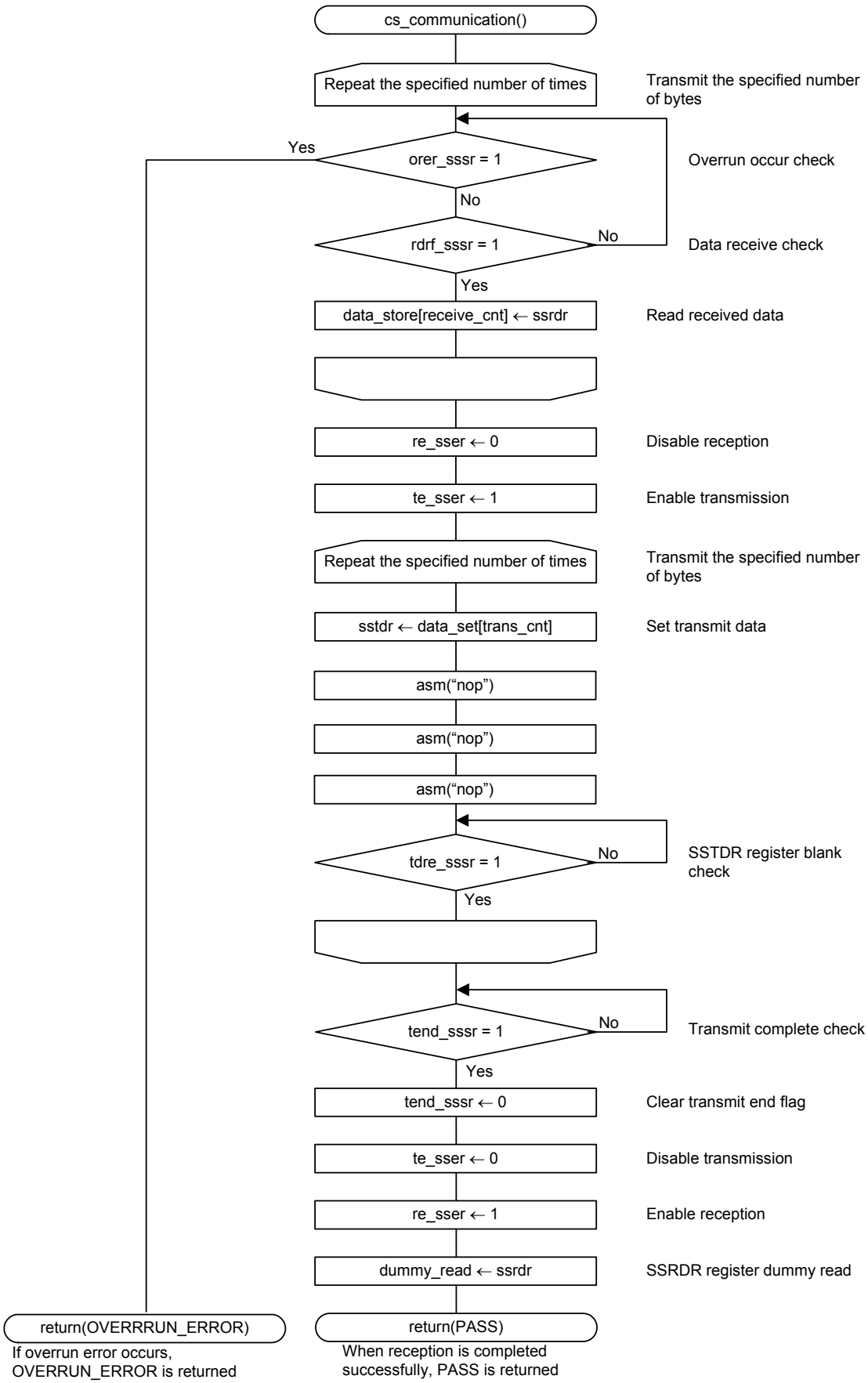
Note 2. SSMR2_INIT value in each mode is deified as below.

4-wire bus communication mode: 0x51

Bidirectional communication mode: 0xd1

Clock synchronous communication mode: 0x40

5.2.3 CS Communication Main Routine



6. Sample Program

A sample program can be downloaded from the Renesas Electronics website.
To download, click “Application Notes” in the left-hand side menu of the R8C Family page.

7. Reference Documents

R8C/2D Group User’s Manual: Hardware
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website
http://www.renesas.com/

Inquiries
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Revision History	R8C/2D Group Clock Synchronous Serial I/O with Chip Select (SSU)

Rev.	Date	Description	
		Page	Summary
1.00	Apr. 29, 2008	—	First edition issued
1.01	Dec. 20, 2010	3	Table 3.2 changed
		30	5.1.3 Procedure of CS Communication Main Routine changed (TN-R8C/A016A/E supported)
		35	5.2.3 Procedure of CS Communication Main Routine changed (TN-R8C/A016A/E supported)

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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