RX65N/RX651 Group, RX64M Group

Points of Difference Between RX65N Group and RX64M Group

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Summary

This application note is intended principally as a reference providing an overview of the peripheral functions of the RX65N Group and RX64M Group, to enable checking of the points of difference between the I/O registers and pin functions of the two groups, and to allow confirmation of key points related to migration.

To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the user's manuals of the products in question.

Target Devices

RX65N Group and RX64M Group

Contents

1. Comparison of Functions of RX65N Group and RX64M Group

A comparison of the functions of the RX65N Group and RX64M Group is provided below. For details of the functions, see 2, Comparative Overview of Functions, and 5, Reference Documents.

Table 1.1 is a comparative listing of the functions of the RX65N and RX64M.

Table 1.1 Comparison of Functions of RX65N and RX64M

Function	RX64M	RX65N Code flash 1.0MB or less	RX65N Code flash more than 1.5 MB
Operating mode	△	△	△
Address Space	△	△	△
Resets	○	○	○
Option-setting memory	△	△	△
Voltage detection circuit (LVDA)	○	○	○
Clock generation circuit	△	△	△
Clock frequency accuracy measurement circuit (CAC)	○	○	○
Low power consumption function	△	△	△
Battery backup function	○	○	○
Register write protection function	○	○	○
Exception Handling	○	○	○
Interrupt Controller	△	△	△
Buses	△	△	△
Memory-protection unit (MPU)	○	○	○
DMA controller (DMACAa)	○	○	○
EXDMA controller (EXDMACa):	○	○	○
Data transfer controller (DTCa): RX64M, (DTCb): RX65N	△	△	△
Event link controller (ELC)	△	△	△
I/O ports	△	△	△
Multi-function pin controller (MPC)	△	△	△
Multi-function timer pulse unit (MTU3a)	○	○	○
Port Output Enable	△	△	△
General PWM Timer (GPTa)	○	×	×
16-bit timer pulse unit (TPUa)	○	○	○
Programmable pulse generator (PPG)	○	○	○
8-bit timer (TMR)	○	○	○
Compare match timer (CMT)	○	○	○
Compare match timer W (CMTW)	○	○	○
Realtime clock (RTCd)	○	○	○
Watchdog timer (WDTA)	○	○	○
Independent watchdog timer (IWDTa)	○	○	○
Ethernet controller (ETHERC)	△	△	△
PTP module for the Ethernet controller (EPTPC)	○	×	×
DMA controller for the ethernet controller (EDMACa)	△	△	△
USB 2.0 FS Host/Function module (USBb)	△	△	△
USB 2.0 Full Speed Host/ Function module (USBA)	○	×	×
Serial Communication Interface	△	△	△
I^2C bus interface (RIICa)	○	○	○

Function	RX64M	RX65N Code flash 1.0MB or less	RX65N Code flash more than 1.5 MB
CAN module (CAN)	△	△	△
Serial peripheral interface (RSPIa): RX64M, (RSPIc): RX65N	△	△	△
Quad serial peripheral interface (QSPI)	○	○	○
CRC calculator (CRC): RX64M, (CRCA): RX65N	△	△	△
Serial sound interface (SSI)	○	×	×
Sampling rate converter (SRC)	○	×	×
SD host interface (SDHI)	△	△	△
SD slave interface (SDSI)	×	○	○
Multimedia card interface (MMCIF)	○	○	○
Parallel data capture unit (PDC)	○	○	○
Boundary scan	○	○	○
AES (AES): RX64M, (AESa): RX65N	○	△	△
DES	○	○	○*
SHA	○	○	○*
RNG (RNG): RX64M, (RNGa): RX65N	△	△	△
12-bit A/D converter (S12ADC): RX64M, (S12ADFa): RX65N	△	△	△
12-Bit D/A Converter	△	△	△
Temperature sensor	○	○	○
Data operation circuit (DOC)	○	○	○
RAM	△	△	△
Standby RAM	○	○	○
Flash Memory (Code Flash)	△	△	△
Flash Memory (Data Flash)	△	×	△
Trusted Secure IP (TSIP)	×	×	○
Graphic LCD Controller (GLCDC)	×	×	○
2D Drawing Engine (DRW2D)	×	×	○
Package (LQFP100/144 only)	△	△	△

Note: ○: Function implemented, ×: Function not implemented, △: Differences exist between implementation of function on RX64M and RX65N.

*:Implementation in Trusted Secure IP

2. Comparative Overview of Functions

2.1 Operating Modes

Table 2.1 shows a comparative overview of the operating mode specifications, and Table 2.2 shows a comparative listing of the operating mode registers.

Table 2.1 Comparative Overview of Operating Modes Specifications

Item	RX64M	RX65N
Operating modes specified by mode setting pins	Single-chip mode	Single-chip mode
	Boot mode (SCI interface)	Boot mode (SCI interface)
	Boot mode (USB interface)	Boot mode (USB interface)
	User boot mode	—
	—	Boot mode (FINE interface)
Operating modes specified by register settings	Single-chip mode	Single-chip mode
	User boot mode	—
	On-chip ROM disabled extended mode	On-chip ROM disabled extended mode
	On-chip ROM enabled extended mode	On-chip ROM enabled extended mode

Table 2.2 Comparative Listing of Operating Mode Registers

Register	Bit	RX64M	RX65N
MDSR	—	Mode status register	—
SYSCR1	ECCRAME	ECCRAM enable bit	—

2.2 Address Space

Figure 2.1 to Figure 2.3 shows the memory maps in the respective operating modes.

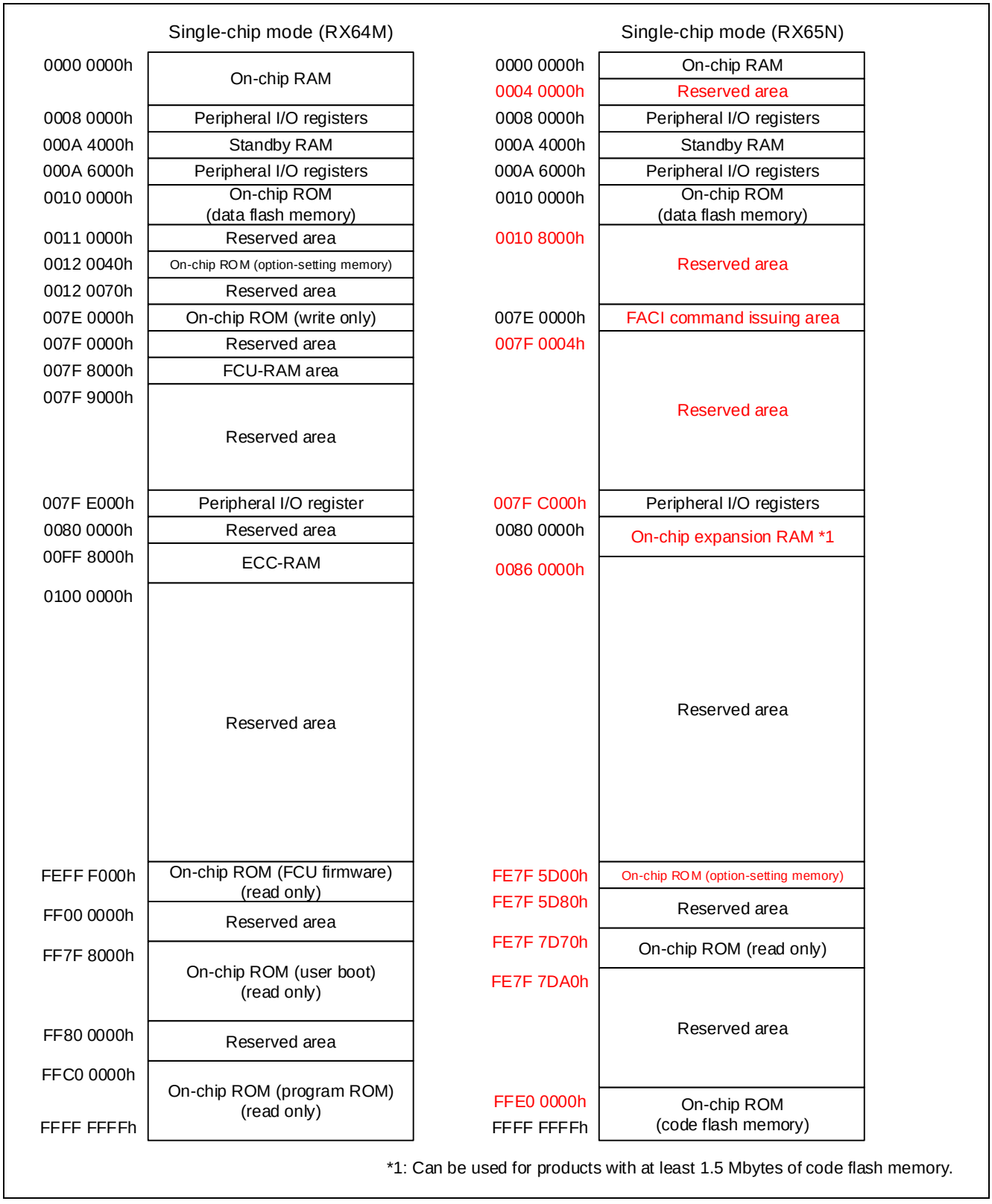

Figure 2.1 Memory Map in Each Operating Mode (Single-chip mode)

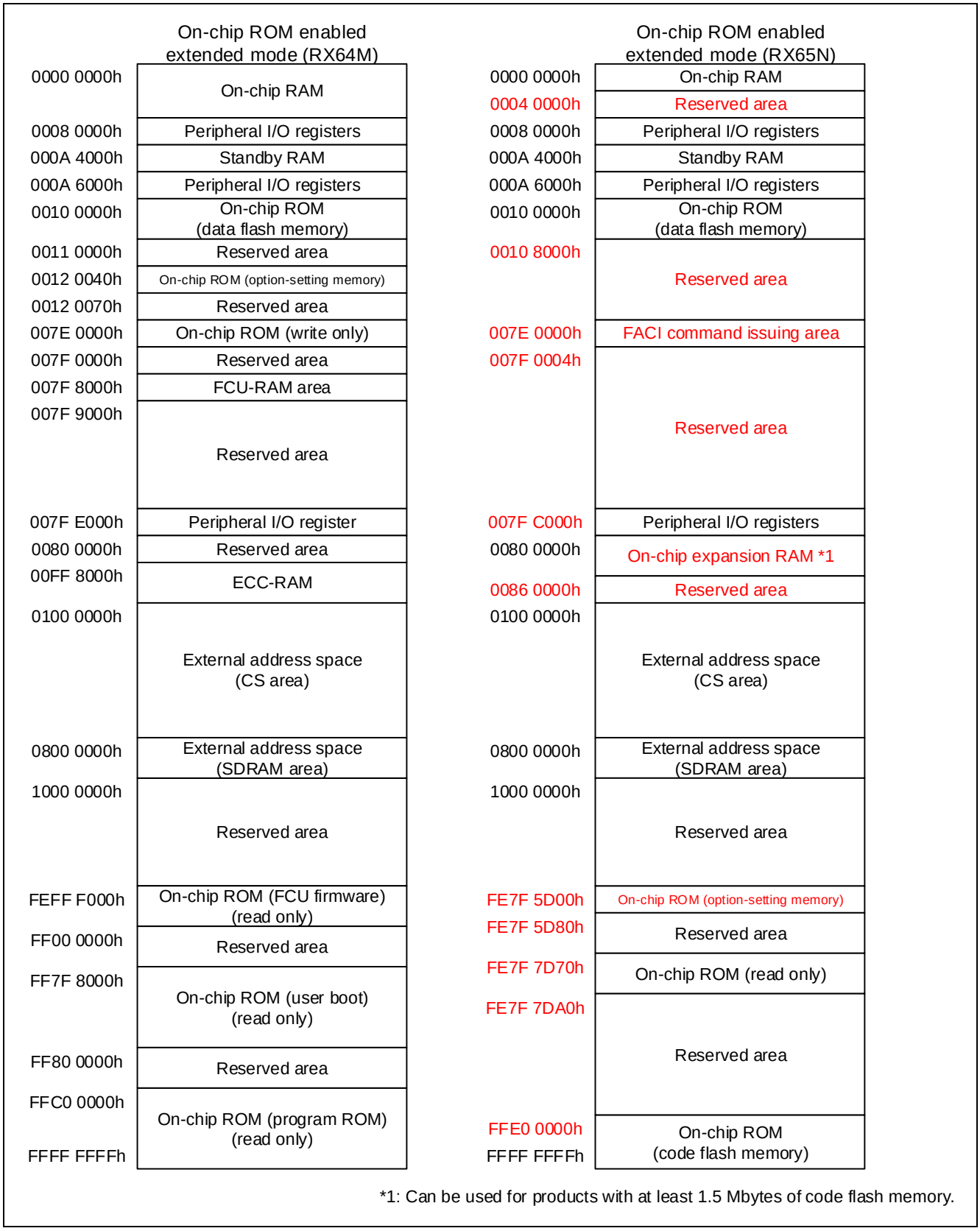

Figure 2.2 Memory Map in Each Operating Mode (On-chip ROM enabled extended mode)

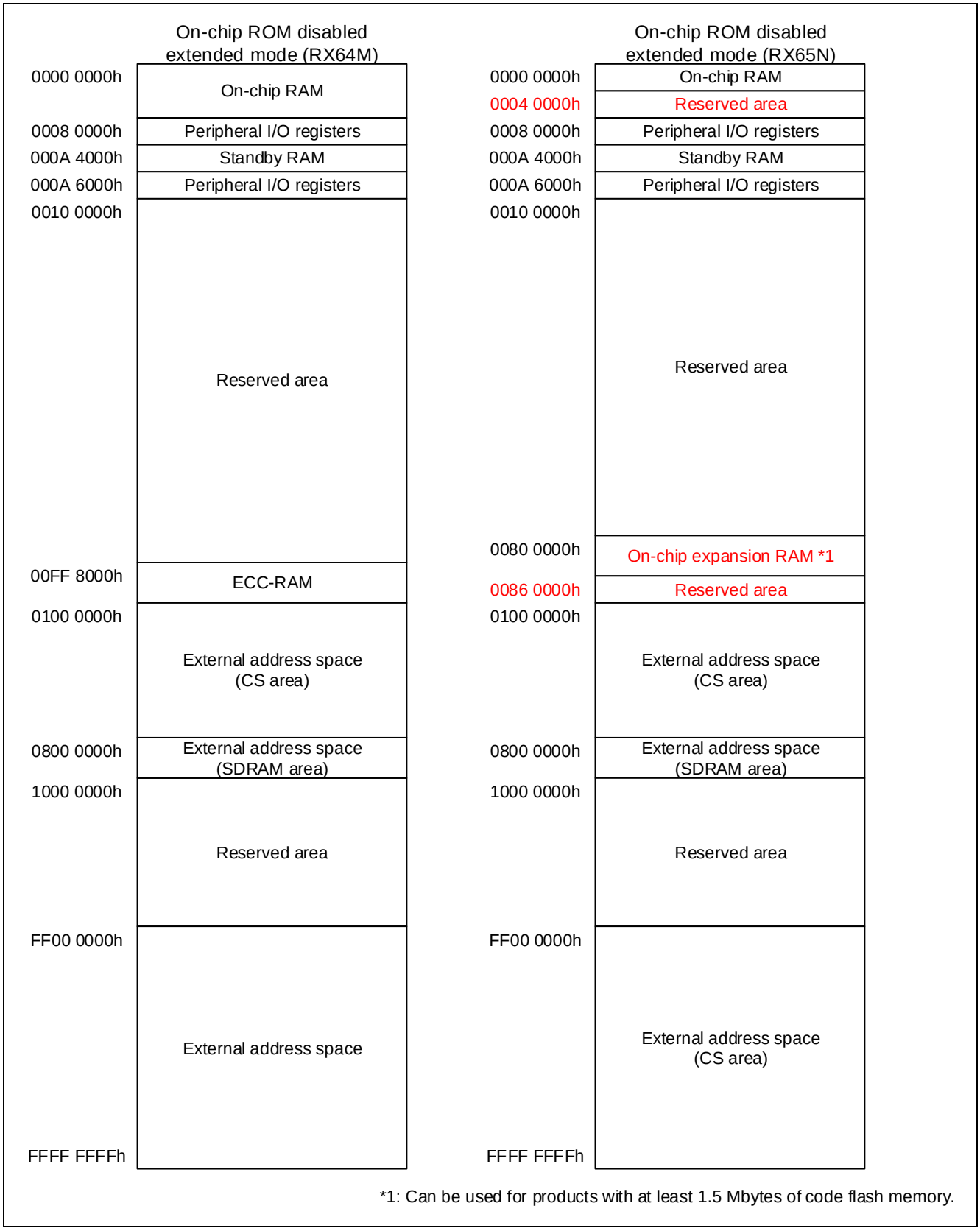

Figure 2.3 Memory Map in Each Operating Mode (On-chip ROM disabled extended mode)

2.3 Option-Setting Memory

Table 2.3 shows a comparative listing of the option-setting memory registers, and Figure 2.4 shows a comparative of the option-setting memory.

Table 2.3 Comparative Listing of Option-Setting Memory Registers

Register	Bit	RX64M	RX65N
SPCC	IDE	ID code protection enable bit	—
	SEPR	Block erasure command protect bit	—
	WRPR	Programming command protect bit	—
	RDPR	Read command protect bit	—
MDE	BANKMD[2:0]	—	Bank Mode Select *1
TMEF	TMEFDB[2:0]	—	Dual-Bank TM Enable *1
BANKSEL	—	—	Bank Select Register *1
FAW	—	—	Flash access window setting register
ROMCODE	—	—	ROM code protection register

*1: Can be used for products with at least 1.5 Mbytes of code flash memory.

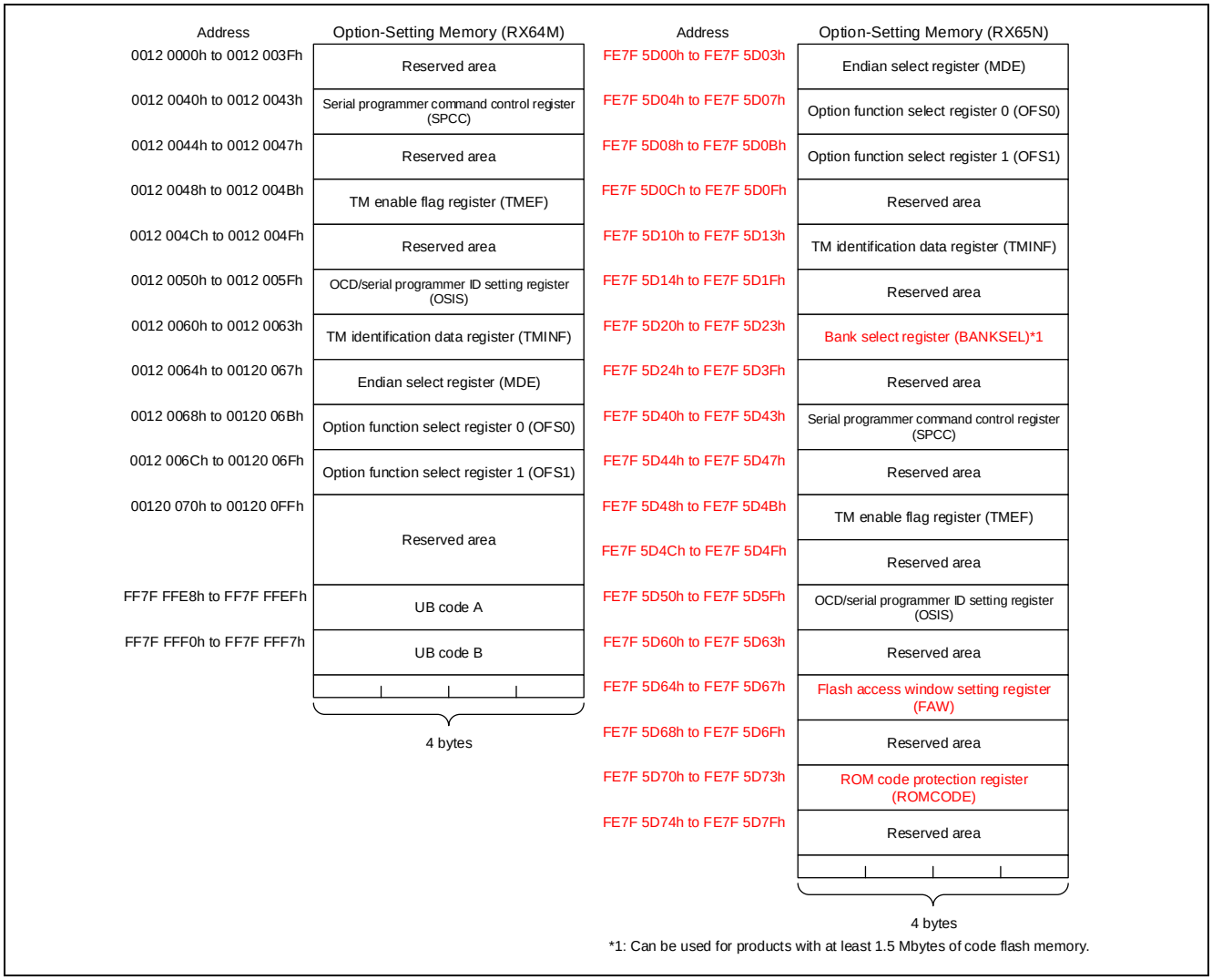

Figure 2.4 Comparative of Option-Setting Memory

2.4 Clock Generation Circuit

Table 2.4 shows a comparative overview of the clock generation circuit specifications, and Table 2.5Table shows a comparative listing of the clock generation circuit registers.

Table 2.4 Comparative Overview of Clock Generation Circuit Specifications

Item	RX64M	RX65N
Uses	• Generates the system clock (ICLK) supplied to the CPU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) supplied to the ETHERC, EDMAC, EPTPC, USBA, RSPI, SCIF, MTU3, GPT, and AES. (Note 1) • Generates the peripheral module clock (PCLKB) supplied to the peripheral modules. • Generates the peripheral module (analog conversion) clocks (PCLKC: unit 0, PCLKD: unit 1) to be supplied to the S12AD. • Generates the FlashIF clock (FCLK) supplied to the FlashIF. • Generates the external bus clock (BCLK) supplied to the external bus. • Generates the SDRAM clock (SDCLK) supplied to the SDRAM. • Generates the USB clock (UCLK) supplied to the PHY in the USBb and USBA. • Generates the USBA clock (USBMCLK) supplied to the PHY in the USBA. • Generates the CAC clock (CACCLK) supplied to the CAC. • Generates the CAN clock (CANMCLK) supplied to the CAN. • Generates the RTC sub clock (RTCSCLK) supplied to the RTC. • Generates the RTC main clock (RTCMCLK) supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) supplied to the IWDT. • Generates the JTAG clock (JTAGTCK) supplied to the JTAG.	• Generates the system clock (ICLK) supplied to the CPU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) supplied to the ETHERC, EDMAC, RSPI, SCIi, MTU3, AES *1, GLCDC *2, and DRW2D *2. (Note 2) • Generates the peripheral module clock (PCLKB) supplied to the peripheral modules. • Generates the peripheral module (analog conversion) clocks (PCLKC: unit 0, PCLKD: unit 1) to be supplied to the S12AD. • Generates the FlashIF clock (FCLK) supplied to the FlashIF. • Generates the external bus clock (BCLK) supplied to the external bus. • Generates the SDRAM clock (SDCLK) supplied to the SDRAM. • Generates the USB clock (UCLK) supplied to the USBb. • Generates the CAC clock (CACCLK) supplied to the CAC. • Generates the CAN clock (CANMCLK) supplied to the CAN. • Generates the RTC sub clock (RTCSCLK) supplied to the RTC. • Generates the RTC main clock (RTCMCLK) supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) supplied to the IWDT. • Generates the JTAG clock (JTAGTCK) supplied to the JTAG.

Item	RX64M	RX65N
Operating frequencies	• ICLK: 120 MHz (max.) • PCLKA: 120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKC: 60 MHz (max.) • PCLKD: 60 MHz (max.) • FCLK: 4 MHz to 60 MHz (for programming and erasing the code flash and data flash) 60 MHz (max.) (for reading from the data flash) • BCLK: 120 MHz (max.) • BCLK pin output: 60 MHz (max.) • SDCLK pin output: 60 MHz (max.) • UCLK: 48 MHz (max.) • USBMCLK: 20 MHz, 24 MHz • CACCLK: Same frequency as each oscillator • CANMCLK: 24 MHz (max.) • RTCSCLK: 32.768 kHz • RTCMCLK: 8 MHz to 16 MHz • IWDTCLK: 120 kHz • JTAGTCK: 10 MHz (max.)	• ICLK: 120 MHz (max.) (Note 3) • PCLKA: 120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKC: 60 MHz (max.) • PCLKD: 60 MHz (max.) • FCLK: 4 MHz to 60 MHz (for programming and erasing the code flash memory and data flash memory*2) 60 MHz (max) (for reading from the data flash memory *2) • BCLK: 120 MHz (max.) • BCLK pin output: 60 MHz (max.) • SDCLK pin output: 60 MHz (max.) • UCLK: 48 MHz (max.) • CACCLK: Same frequency as each oscillator • CANMCLK: 24 MHz (max.) • RTCSCLK: 32.768 kHz • RTCMCLK: 8 MHz to 16 MHz • IWDTCLK: 120 kHz • JTAGTCK: 10 MHz (max.)
Main clock oscillator	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When oscillation stop of the main clock is detected, the system clock source is switched to LOCO, MTU3, and GPT output can be forcedly driven to high-impedance.	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When oscillation stop of the main clock is detected, the system clock source is switched to LOCO, and MTU3 output can be forcedly driven to high-impedance.
Sub-clock oscillator	• Resonator frequency: 32.768 kHz Connectable resonator or additional circuit: crystal resonator • Connection pins: XCIN, XCOUT	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pins: XCIN, XCOUT
PLL frequency synthesizer	• Input clock source: Main clock, HOCO • Input pulse frequency division ratio: Selectable from 1, 2, and 3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication ratio: Selectable within range from 10 to 30 • PLL frequency synthesizer output clock frequency: 120 MHz to 240 MHz	• Input clock source: Main clock, HOCO • Input pulse frequency division ratio: Selectable from 1, 2, and 3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication ratio: Selectable within range from 10 to 30 • PLL frequency synthesizer output clock frequency: 120 MHz to 240 MHz
High-speed on-chip oscillator (HOCO)	• Oscillation frequency: Selectable from 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control	• Oscillation frequency: Selectable from 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control
Low-speed on-chip	Oscillation frequency: 240 kHz	Oscillation frequency: 240 kHz

Item	RX64M	RX65N
oscillator (LOCO)		
IWDT-dedicated on-chip oscillator	Oscillation frequency: 120 kHz	Oscillation frequency: 120 kHz
External clock input (TCK) for JTAG	Input clock frequency: 10 MHz (max.)	Input clock frequency: 10 MHz (max.)
Control of output on BCLK pin	• BCLK clock output or high output is selectable • BCLK or BCLK/2 is selectable as the output clock	• BCLK clock output or high output is selectable • BCLK or BCLK/2 is selectable as the output clock
Control of output on SDCLK pin	SDCLK clock output or high output is selectable	SDCLK clock output or high output is selectable
Event link function (output)	Main clock oscillator oscillation stop detection	Main clock oscillator oscillation stop detection
Event link function (input)	Switching of clock source to low-speed on-chip oscillator	Switching of clock source to low-speed on-chip oscillator

*1: Can be used for products with code flash memory less than 1 megabyte.

*2: Can be used for products with at least 1.5 Mbytes of code flash memory.

Note 1: Restrictions in relation to the clock when ETHERC is in use are as follows.

12.5 MHz ≤ PCLKA ≤ 120 MHz

Note 2: Restrictions in relation to the clock when ETHERC is in use are as follows.

12.5 MHz ≤ PCLKA ≤ 120 MHz, PCLKA frequency = ICLK frequency

Note 3: When the frequency of ICLK is set to faster than 50 MHz, the value of the ROMWT register needs to be modified.

Table 2.5 Comparative Listing of Clock Generation Circuit Registers

Register	Bit	RX64M	RX65N
ROMWT	—	—	ROM wait cycle setting register

2.5 Low Power Consumption Functions

Table 2.6 shows a comparative overview of the low power consumption functions, Table 2.7 to Table 2.10 shows a Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode, and Table 2.11 shows a comparative listing of the low power consumption functions registers.

Table 2.6 Comparative Overview of Low Power Consumption Functions

Item	RX64M	RX65N
Reduction of power consumption by clock switching	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKA, PCLKB, PCLKC, and PCLKD), external bus clock (BCLK), and Flash interface clock (FCLK).	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKA, PCLKB, PCLKC, and PCLKD), external bus clock (BCLK), and Flash interface clock (FCLK).
BCLK output control function	BCLK output or high-level output can be selected.	BCLK output or high-level output can be selected.
SDCLK output control function	SDCLK output or high-level output can be selected.	SDCLK output or high-level output can be selected.
Module stop function	Each peripheral module can be stopped independently.	Each peripheral module can be stopped independently.
Function for transition to low power consumption mode	It is possible to transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped.	It is possible to transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped.
Low power consumption modes	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode
Operating power reduction function	• Power consumption can be reduced in normal operation, sleep mode, and all-module clock stop mode by selecting an appropriate operating power consumption control mode according to the operating frequency and operating voltage. • Operating power control modes: 3 — High-speed operating mode — Low-speed operating mode 1 — Low-speed operating mode 2	• Power consumption can be reduced in normal operation, sleep mode, and all-module clock stop mode by selecting an appropriate operating power consumption control mode according to the operating frequency and operating voltage. • Operating power control modes: 3 — High-speed operating mode — Low-speed operating mode 1 — Low-speed operating mode 2 There is no difference in the power consumption when the same conditions (frequency and voltage) are specified in low-speed operating mode 1 and low-speed operating mode 2.

Table 2.7 Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode (Sleep Mode)

Entering and Exiting Low Power Consumption Modes and Operating States	RX64M	RX65N
	Sleep Mode	Sleep Mode
Transition condition	Control register + instruction	Control register + instruction
Method of release other than reset	Interrupt	Interrupt
State after release	Program execution state (interrupt processing)	Program execution state (interrupt processing)
Main clock oscillator	Operating possible	Operating possible
Sub-clock oscillator	Operating possible	Operating possible
High-speed on-chip oscillator	Operating possible	Operating possible
Low-speed on-chip oscillator	Operating possible	Operating possible
IWDT-dedicated on-chip oscillator	Operating possible	Operating possible
PLL	Operating possible	Operating possible
CPU	Stopped (Retained)	Stopped (Retained)
RAM (ECC RAM included)	Operating possible (Retained)	—
RAM and expansion RAM	—	Operating possible (Retained)
Standby RAM	Operating possible (Retained)	Operating possible (Retained)
Flash memory	Operating	Operating
USBFS host/function module (USBb)	Operating possible	Operating possible
USBFS host/function module (USBA)	Operating possible	—
Watchdog timer (WDTA)	Stopped (Retained)	Stopped (Retained)
Independent watchdog timer (IWDT)	Operating possible	Operating possible
Realtime clock (RTC)	Operating possible	Operating possible
8-bit timer (unit 0, unit 1) (TMR)	Operating possible	Operating possible
Voltage detection circuit (LVDA)	Operating possible	Operating possible
Power-on reset circuit	Operating	Operating
Peripheral modules	Operating possible	Operating possible
I/O ports	Operating	Operating

Table 2.8 Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode (All-Module Clock Stop Mode)

Entering and Exiting Low Power Consumption Modes and Operating States	RX64M	RX65N
	All-Module Clock Stop Mode	All-Module Clock Stop Mode
Transition condition	Control register + instruction	Control register + instruction
Method of release other than reset	Interrupt	Interrupt
State after release	Program execution state (interrupt processing)	Program execution state (interrupt processing)
Main clock oscillator	Operating possible	Operating possible
Sub-clock oscillator	Operating possible	Operating possible
High-speed on-chip oscillator	Operating possible	Operating possible
Low-speed on-chip oscillator	Operating possible	Operating possible
IWDT-dedicated on-chip oscillator	Operating possible	Operating possible
PLL	Operating possible	Operating possible
CPU	Stopped (Retained)	Stopped (Retained)
RAM (ECC RAM included)	Stopped (Retained)	—
RAM and expansion RAM	—	Stopped (Retained)
Standby RAM	Stopped (Retained)	Stopped (Retained)
Flash memory	Stopped (Retained)	Stopped (Retained)
USBFS host/function module (USBb)	Stopped	Stopped
USBFS host/function module (USBA)	Stopped	—
Watchdog timer (WDTA)	Stopped (Retained)	Stopped (Retained)
Independent watchdog timer (IWDT)	Operating possible	Operating possible
Realtime clock (RTC)	Operating possible	Operating possible
8-bit timer (unit 0, unit 1) (TMR)	Operating possible	Operating possible
Voltage detection circuit (LVDA)	Operating possible	Operating possible
Power-on reset circuit	Operating	Operating
Peripheral modules	Stopped (Retained)	Stopped (Retained)
I/O ports	Retained	Retained

Table 2.9 Comparative Listing of Comparative Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode (Software Standby Mode)

Entering and Exiting Low Power Consumption Modes and Operating States	RX64M	RX65N
	Software Standby Mode	Software Standby Mode
Transition condition	Control register + instruction	Control register + instruction
Method of release other than reset	Interrupt	Interrupt
State after release	Program execution state (interrupt processing)	Program execution state (interrupt processing)
Main clock oscillator	Operating possible	Operating possible
Sub-clock oscillator	Operating possible	Operating possible
High-speed on-chip oscillator	Stopped	Stopped
Low-speed on-chip oscillator	Stopped	Stopped
IWDT-dedicated on-chip oscillator	Operating possible	Operating possible
PLL	Stopped	Stopped
CPU	Stopped (Retained)	Stopped (Retained)
RAM (ECC RAM included)	Stopped (Retained)	—
RAM and expansion RAM	—	Stopped (Retained)
Standby RAM	Stopped (Retained)	Stopped (Retained)
Flash memory	Stopped (Retained)	Stopped (Retained)
USBFS host/function module (USBb)	Stopped	Stopped
USBFS host/function module (USBA)	Stopped	—
Watchdog timer (WDTA)	Stopped (Retained)	Stopped (Retained)
Independent watchdog timer (IWDT)	Operating possible	Operating possible
Realtime clock (RTC)	Operating possible	Operating possible
8-bit timer (unit 0, unit 1) (TMR)	Stopped (Retained)	Stopped (Retained)
Voltage detection circuit (LVDA)	Operating possible	Operating possible
Power-on reset circuit	Operating	Operating
Peripheral modules	Stopped (Retained)	Stopped (Retained)
I/O ports	Retained	Retained

Table 2.10 Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode (Deep Software Standby Mode)

Entering and Exiting Low Power Consumption Modes and Operating States	RX64M	RX65N
	Deep Software Standby Mode	Deep Software Standby Mode
Transition condition	Control register + instruction	Control register + instruction
Method of release other than reset	Interrupt	Interrupt
State after release	Program execution state (reset processing)	Program execution state (reset processing)
Main clock oscillator	Operating possible	Operating possible
Sub-clock oscillator	Operating possible	Operating possible
High-speed on-chip oscillator	Stopped	Stopped
Low-speed on-chip oscillator	Stopped	Stopped
IWDT-dedicated on-chip oscillator	Stopped (Undefined)	Stopped (Undefined)
PLL	Stopped	Stopped
CPU	Stopped (Undefined)	Stopped (Undefined)
RAM (ECC RAM included)	Stopped (Undefined)	—
RAM and expansion RAM	—	Stopped (Undefined)
Standby RAM	Stopped (Retained/Undefined)	Stopped (Retained/Undefined)
Flash memory	Stopped (Retained)	Stopped (Retained)
USBFS host/function module (USBb)	Stopped (Retained/Undefined)	Stopped (Retained/Undefined)
USBFS host/function module (USBA)	Stopped (Retained/Undefined)	—
Watchdog timer (WDTA)	Stopped (Undefined)	Stopped (Undefined)
Independent watchdog timer (IWDT)	Stopped (Undefined)	Stopped (Undefined)
Realtime clock (RTC)	Operating possible	Operating possible
8-bit timer (unit 0, unit 1) (TMR)	Stopped (Undefined)	Stopped (Undefined)
Voltage detection circuit (LVDA)	Operating possible	Operating possible
Power-on reset circuit	Operating	Operating
Peripheral modules	Stopped (Undefined)	Stopped (Undefined)
I/O ports	Retained	Retained

Table 2.11 Comparative Listing of Low Power Consumption Functions Registers

Register	Bit	RX64M	RX65N
MSTPCRA	MSTPA7	General PWM timer bit	—
MSTPCRB	MSTPB2	CAN module 2 module stop bit	—
	MSTPB12	Universal serial bus 2.0 FS interface module stop bit	—
	MSTPB14	Ethernet controller and ethernet controller DMA controller (channel 1) modules stop bit	—
	MSTPB16	—	Serial peripheral interface 1 module stop bit
	MSTPB20	—	I^2C Bus Interface 1 Module Stop *1
MSTPCRC	MSTPC2	—	Expansion RAM Module Stop *1
	MSTPC6	ECCRAM module stop bit	—
	MSTPC22	—	Serial peripheral interface 2 module stop bit
	MSTPC24	FIFO on-chip serial communications interface 11 module stop bit	Serial communications interface 11 module stop bit
	MSTPC25	FIFO on-chip serial communications interface 10 module stop bit	Serial communications interface 10 module stop bit
	MSTPC26	FIFO on-chip serial communications interface 9 module stop bit	Serial communications interface 9 module stop bit
	MSTPC27	FIFO on-chip serial communications interface 8 module stop bit	Serial communications interface 8 module stop bit
	MSTPC28	—	2D drawing engine Module Stop *1
	MSTPC29	—	Graphic-LCD controller Module Stop *1
MSTPCRD	MSTPD13	—	SD slave interface module stop bit
	MSTPD14	Serial sound interface 1 module stop bit	—
	MSTPD15	Serial sound interface 0 module stop bit	
	MSTPD23	Sampling rate converter module stop bit	—
	MSTPD27	—	Trusted Secure IP Module Stop *1

*1: Can be used for products with at least 1.5 Mbytes of code flash memory.

2.6 Interrupt Controller

Table 2.12 shows a comparative overview of the interrupt controller specifications, and Table 2.13 shows a comparative listing of the interrupt controller registers.

Table 2.12 Comparative Overview of Interrupt Controller Specifications

Item		RX64M (ICUA)	RX65N (ICUB)
Interrupt	Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection (detection method is fixed for each interrupt source) • Interrupt grouping: Multiple interrupt sources can be grouped together and treated as a single interrupt source. — Group BE0 interrupt: Peripheral module interrupt source using PCLKB as operation clock (edge detection) — Group BL0 and BL1 interrupts: Peripheral module interrupt sources using PCLKB as operation clock (level detection) — Group AL0 and AL1 interrupts: Peripheral module interrupt sources using PCLKA as operation clock (level detection) • Selectable interrupt B: For each interrupt vector number from 128 to 207, one peripheral module interrupt source using PCLKB as operation clock may be assigned. • Selectable interrupt A: For each interrupt vector number from 208 to 255, one peripheral module interrupt source using PCLKA as operation clock may be assigned.	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection (detection method is fixed for each interrupt source) • Interrupt grouping: Multiple interrupt sources can be grouped together and treated as a single interrupt source. — Group BE0 interrupt: Peripheral module interrupt source using PCLKB as operation clock (edge detection) — Group BL0, BL1, and BL2 interrupts: Peripheral module interrupt sources using PCLKB as operation clock (level detection) — Group AL0 and AL1 interrupts: Peripheral module interrupt sources using PCLKA as operation clock (level detection) • Selectable interrupt B: For each interrupt vector number from 128 to 207, one peripheral module interrupt source using PCLKB as operation clock may be assigned. • Selectable interrupt A: For each interrupt vector number from 208 to 255, one peripheral module interrupt source using PCLKA as operation clock may be assigned.

Item		RX64M (ICUA)	RX65N (ICUB)
Interrupt	External pin interrupts	• Interrupts from signals input to IRQi pins (i = 0 to 15) • Interrupt detection: Low level, falling edge, rising edge, and rising and falling edges. One of these detection methods can be set for each source. • Digital filter may be used to suppress noise.	• Interrupts from signals input to IRQi pins (i = 0 to 15) • Interrupt detection: Low level, falling edge, rising edge, and rising and falling edges. One of these detection methods can be set for each source. • Digital filter may be used to suppress noise.
	Software interrupt	• Interrupts can be generated by writing to a register. • Interrupt sources: 2	• Interrupts can be generated by writing to a register. • Interrupt sources: 2
	Interrupt priority level	Priority level can be set with interrupt source priority register r (IPRr) (r = 000 to 255)	Priority level can be set with interrupt source priority register r (IPRr) (r = 000 to 255)
	Fast interrupt function	CPU interrupt response time can be reduced. This function can be used for only one interrupt source.	CPU interrupt response time can be reduced. This function can be used for only one interrupt source.
	DTC and DMAC control	Interrupt sources can be used to start the DTC and DMAC.	Interrupt sources can be used to start the DTC and DMAC.
	EXDMAC control	• Interrupt selected by software configurable interrupt B source select register 144 or software configurable interrupt A source select register 208 can be used to start EXDMAC0. • Interrupt selected by software configurable interrupt B source select register 145 or software configurable interrupt A source select register 209 can be used to start EXDMAC1.	• Interrupt selected by software configurable interrupt B source select register 144 or software configurable interrupt A source select register 208 can be used to start EXDMAC0. • Interrupt selected by software configurable interrupt B source select register 145 or software configurable interrupt A source select register 209 can be used to start EXDMAC1.
Non-maskable interrupts	NMI pin interrupt	Interrupts from signals input to NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter may be used to suppress noise.	Interrupts from signals input to NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter may be used to suppress noise.
	Oscillation stop detection interrupt	This interrupt occurs when the main clock oscillator stop is detected.	This interrupt occurs when the main clock oscillator stop is detected.
	WDT underflow/refresh error interrupt	This interrupt occurs when the watchdog timer (WDT) underflows or a refresh error occurs.	This interrupt occurs when the watchdog timer (WDT) underflows or a refresh error occurs.
	IWDT underflow/refresh error interrupt	This interrupt occurs when the independent watchdog timer (IWDT) underflows or a refresh error occurs.	This interrupt occurs when the independent watchdog timer (IWDT) underflows or a refresh error occurs.
	Voltage monitoring 1 interrupt	Interrupt triggered by voltage detection circuit 1 (LVD1)	Interrupt triggered by voltage detection circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	Interrupt triggered by voltage detection circuit 2 (LVD2)	Interrupt triggered by voltage detection circuit 2 (LVD2)

Item		RX64M (ICUA)	RX65N (ICUB)
Non-maskable interrupts	RAM error interrupt	This interrupt occurs when a parity check error is detected in the RAM or an ECC error is detected in the ECCRAM.	This interrupt occurs when a parity check error is detected in the RAM (including the expanded RAM *1).
Return from low power consumption modes	Sleep mode	Return is initiated by any interrupt source.	Return is initiated by any interrupt source.
	All-module clock stop mode	Return is initiated by NMI pin interrupts, external pin interrupts, and peripheral function interrupts (voltage monitor 1, voltage monitor 2, oscillation stop detection, USB resume, RTC alarm, RTC period, USBA resume, IWDT, selectable interrupts 146 to 157).	Return is initiated by NMI pin interrupts, external pin interrupts, and peripheral function interrupts (voltage monitor 1, voltage monitor 2, oscillation stop detection, USB resume, RTC alarm, RTC period, IWDT, selectable interrupts 146 to 157).
	Software standby mode	Return is initiated by NMI pin interrupts, external pin interrupts, and peripheral function interrupts (voltage monitor 1, voltage monitor 2, USB resume, RTC alarm, RTC period, USBA resume, IWDT).	Return is initiated by NMI pin interrupts, external pin interrupts, and peripheral function interrupts (voltage monitor 1, voltage monitor 2, USB resume, RTC alarm, RTC period, IWDT).
	Deep software standby mode	Return is initiated by NMI pin interrupts, some external pin interrupts, and peripheral function interrupts (voltage monitor 1, voltage monitor 2, USB resume, RTC alarm, RTC period, USBA resume).	Return is initiated by NMI pin interrupts, some external pin interrupts, and peripheral function interrupts (voltage monitor 1, voltage monitor 2, USB resume, RTC alarm, RTC period).

*1: Can be used for products with at least 1.5 Mbytes of code flash memory.

Table 2.13 Comparative Listing of Interrupt Controller Registers

Register	Bit	RX64M (ICUA)	RX65N (ICUB)
NMISR	ECCRAMST	RAM ECC error interrupt status flag	—
	RAMST	—	RAM error interrupt status flag
NMIER	ECCRAMEN	RAM ECC error interrupt enable bit	—
	RAMEN	—	RAM error interrupt enable bit
GRPBL2	—		Group BL2 interrupt request register
GENBL2	—		Group BL2 interrupt request enable register
PIBRk	—	Software Configurable Interrupt B Request Register k (k = 0h to Ah)	Software Configurable Interrupt B Request Register k (k = 0h to Bh)
PIARk	—	Software configurable interrupt A request register k (k = 0h to Bh)	Software configurable interrupt A request register k (k = 0h to 5h, Bh)

2.7 Bus

Table 2.14 shows a comparative overview of the bus specifications, and Table 2.15 shows a comparative listing of the bus registers.

Table 2.14 Comparative Overview of Bus Specifications

Item		RX64M	RX65N
CPU bus	Instruction bus	• Connected to the CPU (for instructions). • Connected to the on-chip memory (RAM and code flash memory). • Operates in synchronization with the system clock (ICLK).	• Connected to the CPU (for instructions). • Connected to the on-chip memory (RAM, expansion RAM*1, code flash memory). • Operates in synchronization with the system clock (ICLK).
	Operand bus	• Connected to the CPU (for operand). • Connected to the on-chip memory (RAM and code flash memory). • Operates in synchronization with the system clock (ICLK).	• Connected to the CPU (for operand). • Connected to the on-chip memory (RAM, expansion RAM*1, code flash memory). • Operates in synchronization with the system clock (ICLK).
Memory buses	Memory bus 1	Connected to the RAM.	Connected to the RAM.
	Memory bus 2	Connected to the code flash memory.	Connected to the code flash memory.
	Memory bus 3	Connected to the ECCRAM.	Connected to expansion RAM*1
Internal main buses	Internal main bus 1	• Connected to the CPU. • Operates in synchronization with the system clock (ICLK).	• Connected to the CPU. • Operates in synchronization with the system clock (ICLK).
	Internal main bus 2	• Connected to the DTC, DMAC, and EDMAC. • Connected to the on-chip memory (RAM and code flash memory). • Operates in synchronization with the system clock (ICLK).	• Connected to the DTC, DMAC, EDMAC, and extended bus master. • Connected to the on-chip memory (RAM, expansion RAM*1, code flash memory). • Operates in synchronization with the system clock (ICLK).
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, DMAC, EXDMAC, interrupt controller, and bus error monitoring section). • Operates in synchronization with the system clock (ICLK). (EXDMAC operates in synchronization with BCLK.)	• Connected to peripheral modules (DTC, DMAC, EXDMAC, interrupt controller, and bus error monitoring section). • Operates in synchronization with the system clock (ICLK). (EXDMAC operates in synchronization with BCLK.)
	Internal peripheral bus 2	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, 4, and 5). • Operates in synchronization with the peripheral module clock (PCLKB).	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, 4, and 5). • Operates in synchronization with the peripheral module clock (PCLKB).

Item		RX64M	RX65N
Internal peripheral buses	Internal peripheral bus 3	• Connected to peripheral modules (USBb, PDC, and standby RAM). • Operates in synchronization with the peripheral module clock (PCLKB).	• Connected to peripheral modules (USBb, PDC, and standby RAM). • Operates in synchronization with the peripheral module clock (PCLKB).
	Internal peripheral bus 4	• Connected to peripheral modules (EDMAC, ETHERC,EPTPC, MTU3, GPT,SCIF, RSPI, USBA, and AES). • Operates in synchronization with the peripheral module clock (PCLKA).	• Connected to peripheral modules (EDMAC,ETHERC,MTU3,SCIi, RSPI, and AES *2). • Operates in synchronization with the peripheral module clock (PCLKA).
	Internal peripheral bus 5	Reserved area	• Connected to peripheral modules (GLCDC, DRW2D) *1 • Operates in synchronization with the peripheral-module clock (PCLKA) *1
	Internal peripheral bus 6	• Connected to code flash (in P/E) and data flash memory. • Operates in synchronization with the FlashIF clock (FCLK).	• Connected to code flash (in P/E) and data flash memory *1. • Operates in synchronization with the FlashIF clock (FCLK).
External bus	CS area	• Connected to external devices. • Operates in synchronization with the external bus clock (BCLK).	• Connected to external devices. • Operates in synchronization with the external bus clock (BCLK).
	SDRAM area	• Connected to SDRAM. • Operates in synchronization with the SDRAM clock (SDCLK).	• Connected to SDRAM. • Operates in synchronization with the SDRAM clock (SDCLK).

*1: Can be used for products with at least 1.5 Mbytes of code flash memory.

*2: Can be used for products with code flash memory less than 1 megabyte.

Table 2.15 Comparative Listing of Bus Registers

Register	Bit	RX64M	RX65N
CSnCR (n = 0 to 7)	BSIZE[1:0]	External bus width select bits b5 b4 0 0: A 16-bit bus width is selected. 0 1: A 32-bit bus width is selected. 1 0: An 8-bit bus width is selected. 1 1: Setting prohibited.	External bus width select bits b5 b4 0 0: A 16-bit bus width is selected. 0 1: Setting prohibited. / A 32-bit bus width is selected*1. 1 0: An 8-bit bus width is selected. 1 1: Setting prohibited.
SDCCR	BSIZE[1:0]	SDRAM bus width select bits b5 b4 0 0: A 16-bit bus width is selected. 0 1: A 32-bit bus width is selected. 1 0: An 8-bit bus width is selected. 1 1: Setting prohibited.	SDRAM bus width select bits b5 b4 0 0: A 16-bit bus width is selected. 0 1: Setting prohibited. / A 32-bit bus width is selected*1. 1 0: An 8-bit bus width is selected. 1 1: Setting prohibited.
BERSR1	MST[2:0]	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC/DMAC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: EDMAC 1 1 1: EXDMAC	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC/DMAC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: EDMAC/SDSI 1 1 1: EXDMAC
BUSPRI	BPRA[1:0]	Memory bus 1 and 3 priority (RAM/ECCRAM) control bits	Internal Peripheral Bus 1 and 3 (RAM / expansion RAM *1) Priority Control
	BPHB[1:0]	Internal peripheral bus 4 and 5 priority control bit	Internal peripheral bus 4 and 5 priority control bit *1

*1: Can be used for products with at least 1.5 Mbytes of code flash memory.

2.8 Data Transfer Controller

Table 2.16 shows a comparative overview of the data transfer controller specifications, and Table 2.17 shows a comparative listing of the data transfer controller registers.

Table 2.16 Comparative Overview of Data Transfer Controller

Item	RX64M (DTCa)	RX65N (DTCb)
Transfer modes	• Normal transfer mode A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address is returned to the transfer start address after a number of data transfers corresponding to the repeat size. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, 1,024 bytes. • Block transfer mode — A single activation leads to the transfer of a single block. — Maximum block size setting: 256 × 32 bits = 1,024 bytes	• Normal transfer mode A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address is returned to the transfer start address after a number of data transfers corresponding to the repeat size. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, 1,024 bytes. • Block transfer mode — A single activation leads to the transfer of a single block. — Maximum block size setting: 256 × 32 bits = 1,024 bytes
Transfer channels	• Channel transfer corresponding to the interrupt source is possible (transferred by DTC activation request from the ICU). • Data of multiple channels can be transferred on a single activation source (chain transfer). • Either “executed when the counter is 0” or “always executed” can be selected for chain transfer.	• Channel transfer corresponding to the interrupt source is possible (transferred by DTC activation request from the ICU). • Data of multiple channels can be transferred on a single activation source (chain transfer). • Either “executed when the counter is 0” or “always executed” can be selected for chain transfer.
Transfer space	• 16 Mbytes in short-address mode (areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh, excepting reserved areas) • 4 Gbytes in full-address mode (area from 0000 0000h to FFFF FFFFh, excepting reserved areas)	• 16 Mbytes in short-address mode (areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh, excepting reserved areas) • 4 Gbytes in full-address mode (area from 0000 0000h to FFFF FFFFh, excepting reserved areas)
Data transfer units	• Single data: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data	• Single data: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data
CPU interrupt requests	• An interrupt request can be generated to the CPU on a DTC activation interrupt. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after data transfer of a specified volume.	• An interrupt request can be generated to the CPU on a DTC activation interrupt. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after data transfer of a specified volume.

Item	RX64M (DTCa)	RX65N (DTCb)
Event link activation	Event link request generated after one data transfer (or after one block transfer in case of block transfer operation).	Event link request generated after one data transfer (or after one block transfer in case of block transfer operation).
Read skip	Reading of the transfer information can be skipped when the same transfer is repeated.	Reading of the transfer information can be skipped when the same transfer is repeated.
Write-back skip	When “fixed” is selected for the transfer source address or transfer destination address, write-back of non-updated transfer data can be omitted.	When “fixed” is selected for the transfer source address or transfer destination address, write-back of non-updated transfer data can be omitted.
Write-back disable	—	It is possible to disable write-back of transfer information.
Sequence transfer	—	A series of complicated transfers can be registered as a sequence. Any sequence can be selected by the transfer data and executed. • Only one trigger source can be set at a time. • Up to 256 sequences for a single trigger source • The data that is initially transferred in response to a transfer request determines a sequence • The whole sequence can be executed on a single request, or be suspended in the middle of the sequence and resumed on the next transfer request (division of sequence).
Displacement addition	—	Displacement can be added to the transfer source address (selectable in each set of transfer information).
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Table 2.17 Comparative Listing of Data Transfer Controller Registers

Register	Bit	RX64M (DTCa)	RX65N (DTCb)
MRA	WBDIS	—	Write-back disable bit
MRB	SQEND	—	Sequence transfer end bit
	INDX	—	Index table reference bit
MRC	—	—	DTC mode register C
DTCIBR	—	—	DTC index table base register
DTCOR	—	—	DTC operation register
DTCSQE	—	—	DTC sequence transfer enable register
DTCDISP	—	—	DTC address displacement register

2.9 Event Link Controller

Table 2.18 shows a comparative overview of the event link controller specifications, Table 2.19 shows a comparative listing of the event link controller registers.

Table 2.18 Comparative Overview of Event Link Controller Specifications

Item	RX64M (ELC)	RX65N (ELC)
Event link function	• 119 event signals can be directly connected to modules. • It is possible to specify that timer modules operate when an event is input. • Event link operation is possible for port B and port E. — Single-port*1: Event link operation can be enabled for a specified single bit in a port. — Port group*1: An event link can be enabled for a group of specified bits within 8-pin I/O ports.	• 82 event signals can be directly connected to modules. • It is possible to specify that timer modules operate when an event is input. • Event link operation is possible for port B and port E. — Single-port*1: Event link operation can be enabled for a specified single bit in a port. — Port group*1: An event link can be enabled for a group of specified bits within 8-pin I/O ports.
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Note 1. The single port or port group specified as the input generates an event when a change in the connected signal value occurs.

Table 2.19 Comparative Listing of Event Link Controller Registers

Register	Bit	RX64M (ELC)	RX65N (ELC)
ELSRn	—	Event link setting register n (n = 0, 3, 4, 7, 10 to 13, 15, 16, 18 to 28, 33, 35 to 38, 41 to 45)	Event link setting register n (n = 0, 3, 4, 7, 10 to 13, 15, 16, 18 to 28, 33, 35 to 38, 45)
ELOPI	—	Event link option setting register I	—
ELOPJ	—	Event link option setting register J	—

2.10 I/O Ports

Table 2.20 to Table 2.22 shows a Comparative Listing of Specifications of I/O Ports, and Table 2.23 shows a comparative listing of the I/O port register.

Table 2.20 Comparative Listing of Specifications of I/O Ports (177 or 176 Pins)

Port	RX64M	RX65N
PORT0	P00 to P03, P05, P07	P00 to P03, P05, P07
PORT1	P10 to P17	P10 to P17
PORT2	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P53	P50 to P57
PORT6	P60 to P67	P60 to P67
PORT7	P70 to P77	P70 to P77
PORT8	P80 to P83, P86, P87	P80 to P87
PORT9	P90 to P97	P90 to P97
PORTA	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7
PORTF	PF0 to PF5	PF0 to PF5
PORTG	PG0 to PG7	PG0 to PG7
PORTJ	PJ3, PJ5	PJ0 to PJ3, PJ5

Table 2.21 Comparative Listing of Specifications of I/O Ports (145 or 144 Pins)

Port	RX64M	RX65N
PORT0	P00 to P03, P05, P07	P00 to P03, P05, P07
PORT1	P12 to P17	P12 to P17
PORT2	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P56	P50 to P56
PORT6	P60 to P67	P60 to P67
PORT7	P70 to P77	P70 to P77
PORT8	P80 to P83, P86, P87	P80 to P83, P86, P87
PORT9	P90 to P93	P90 to P93
PORTA	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7
PORTF	PF5	PF5
PORTG	Not provided	Not provided
PORTJ	PJ3, PJ5	PJ3, PJ5

Table 2.22 Comparative Listing of Specifications of I/O Ports (100 Pins)

Port	RX64M	RX65N
PORT0	P05, P07	P05, P07
PORT1	P12 to P17	P12 to P17
PORT2	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P55	P50 to P55
PORT6	Not provided	Not provided
PORT7	Not provided	Not provided
PORT8	Not provided	Not provided
PORT9	Not provided	Not provided
PORTA	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7
PORTF	Not provided	Not provided
PORTG	Not provided	Not provided
PORTJ	PJ3	PJ3

Table 2.23 Comparative Listing of I/O Port Register

Register	Bit	RX64M	RX65N
DSCR2	—	—	Drive capacity control register 2

2.11 Multi-Function Pin Controller

Table 2.24 shows a comparative listing of functions assigned to each multiplexed pin, and Table 2.25 shows a comparative listing of the multi-function pin controller port registers.

Blue characters exist only in the RX65N, and orange characters exist only in the RX64M.

Table 2.24 Comparative Listing of Functions Assigned to Each Multiplexed Pin

Pin Functions	Allocation Port	RX64M			RX65N		
		177 pin 176 pin	145 pin 144 pin	100 pin	177 pin 176 pin	145 pin 144 pin	100 pin
NMI (input)	P35	√	√	√	√	√	√
EDREQ0 (input)	P22	√	√	√	√	√	√
	P55	×	√	√	√	√	√
	P80	√	√	×	√	√	×
EDACK0 (output)	P23	√	√	√	√	√	√
	P54	×	√	√	√	√	√
	P81	√	√	×	√	√	×
EDREQ1 (input)	P24	√	√	√	√	√	√
	P33	√	√	√	√	√	√
	P82	√	√	×	√	√	×
EDACK1 (output)	P25	√	√	√	√	√	√
	P56	×	√	×	√	√	×
	P83	√	√	×	√	√	×
	PJ3	√	√	√	√	√	√
IRQ0-DS (input)	P30	√	√	√	√	√	√
IRQ0 (input)	P10	√	×	×	√	×	×
	PD0	√	√	√	√	√	√
IRQ1-DS (input)	P31	√	√	√	√	√	√
IRQ1 (input)	P11	√	×	×	√	×	×
	PD1	√	√	√	√	√	√
IRQ2-DS (input)	P32	√	√	√	√	√	√
IRQ2 (input)	P12	√	√	√	√	√	√
	PD2	√	√	√	√	√	√
IRQ3-DS (input)	P33	√	√	√	√	√	√
IRQ3 (input)	P13	√	√	√	√	√	√
	PD3	√	√	√	√	√	√
IRQ4-DS (input)	PB1	√	√	√	√	√	√
IRQ4 (input)	P14	√	√	√	√	√	√
	P34	√	√	√	√	√	√
	PD4	√	√	√	√	√	√
	PF5	√	√	×	√	√	×
IRQ5-DS (input)	PA4	√	√	√	√	√	√
IRQ5 (input)	P15	√	√	√	√	√	√
	PD5	√	√	√	√	√	√
	PE5	√	√	√	√	√	√
IRQ6-DS (input)	PA3	√	√	√	√	√	√

Pin Functions	Allocation Port	RX64M			RX65N		
		177 pin 176 pin	145 pin 144 pin	100 pin	177 pin 176 pin	145 pin 144 pin	100 pin
IRQ6 (input)	P16	√	√	√	√	√	√
	PD6	√	√	√	√	√	√
	PE6	√	√	√	√	√	√
IRQ7-DS (input)	PE2	√	√	√	√	√	√
IRQ7 (input)	P17	√	√	√	√	√	√
	PD7	√	√	√	√	√	√
	PE7	√	√	√	√	√	√
IRQ8-DS (input)	P40	√	√	√	√	√	√
IRQ8 (input)	P00	√	√	×	√	√	×
	P20	√	√	√	√	√	√
IRQ9-DS (input)	P41	√	√	√	√	√	√
IRQ9 (input)	P01	√	√	×	√	√	×
	P21	√	√	√	√	√	√
IRQ10-DS (input)	P42	√	√	√	√	√	√
IRQ10 (input)	P02	√	√	×	√	√	×
	P55	×	√	√	√	√	√
IRQ11-DS (input)	P43	√	√	√	√	√	√
IRQ11 (input)	P03	√	√	×	√	√	×
	PA1	√	√	√	√	√	√
IRQ12-DS (input)	P44	√	√	√	√	√	√
IRQ12 (input)	PB0	√	√	√	√	√	√
	PC1	√	√	√	√	√	√
IRQ13-DS (input)	P45	√	√	√	√	√	√
IRQ13 (input)	P05	√	√	√	√	√	√
	PC6	√	√	√	√	√	√
IRQ14-DS (input)	P46	√	√	√	√	√	√
IRQ14 (input)	PC0	√	√	√	√	√	√
	PC7	√	√	√	√	√	√
IRQ15-DS (input)	P47	√	√	√	√	√	√
IRQ15 (input)	P07	√	√	√	√	√	√
	P67	√	√	×	√	√	×
MTIOC0A (input/output)	P34	√	√	√	√	√	√
	PB3	√	√	√	√	√	√
MTIOC0B (input/output)	P13	√	√	√	√	√	√
	P15	√	√	√	√	√	√
	PA1	√	√	√	√	√	√
MTIOC0C (input/output)	P32	√	√	√	√	√	√
	PB1	√	√	√	√	√	√
MTIOC0D (input/output)	P33	√	√	√	√	√	√
	PA3	√	√	√	√	√	√
MTIOC1A (input/output)	P20	√	√	√	√	√	√
	PE4	√	√	√	√	√	√
MTIOC1B (input/output)	P21	√	√	√	√	√	√
	PB5	√	√	√	√	√	√

Pin Functions	Allocation Port	RX64M			RX65N		
		177 pin 176 pin	145 pin 144 pin	100 pin	177 pin 176 pin	145 pin 144 pin	100 pin
MTIOC2A (input/output)	P26	√	√	√	√	√	√
	PB5	√	√	√	√	√	√
MTIOC2B (input/output)	P27	√	√	√	√	√	√
	PE5	√	√	√	√	√	√
MTIOC3A (input/output)	P14	√	√	√	√	√	√
	P17	√	√	√	√	√	√
	PC1	√	√	√	√	√	√
	PC7	√	√	√	√	√	√
MTIOC3B (input/output)	P17	√	√	√	√	√	√
	P22	√	√	√	√	√	√
	P80	√	√	×	√	√	×
	PB7	√	√	√	√	√	√
	PC5	√	√	√	√	√	√
	PE1	√	√	√	√	√	√
MTIOC3C (input/output)	P16	√	√	√	√	√	√
	P56	×	√	×	√	√	×
	PC0	√	√	√	√	√	√
	PC6	√	√	√	√	√	√
	PJ3	√	√	√	√	√	√
MTIOC3D (input/output)	P16	√	√	√	√	√	√
	P23	√	√	√	√	√	√
	P81	√	√	×	√	√	×
	PB6	√	√	√	√	√	√
	PC4	√	√	√	√	√	√
	PE0	√	√	√	√	√	√
MTIOC4A (input/output)	P21	√	√	√	√	√	√
	P24	√	√	√	√	√	√
	P82	√	√	×	√	√	×
	PA0	√	√	√	√	√	√
	PB3	√	√	√	√	√	√
	PE2	√	√	√	√	√	√
MTIOC4B (input/output)	P17	√	√	√	√	√	√
	P30	√	√	√	√	√	√
	P54	×	√	√	√	√	√
	PC2	√	√	√	√	√	√
	PD1	√	√	√	√	√	√
	PE3	√	√	√	√	√	√
MTIOC4C (input/output)	P25	√	√	√	√	√	√
	P83	√	√	×	√	√	×
	P87	√	√	×	√	√	×
	PB1	√	√	√	√	√	√
	PE1	√	√	√	√	√	√
	PE5	√	√	√	√	√	√

Pin Functions	Allocation Port	RX64M			RX65N		
		177 pin 176 pin	145 pin 144 pin	100 pin	177 pin 176 pin	145 pin 144 pin	100 pin
MTIOC4D (input/output)	P31	√	√	√	√	√	√
	P55	×	√	√	√	√	√
	P86	√	√	×	√	√	×
	PC3	√	√	√	√	√	√
	PD2	√	√	√	√	√	√
	PE4	√	√	√	√	√	√
MTIC5U (input)	P12	√	×	×	√	×	×
	PA4	√	√	√	√	√	√
	PD7	√	√	√	√	√	√
MTIC5V (input)	P11	√	×	×	√	×	×
	PA6	√	√	√	√	√	√
	PD6	√	√	√	√	√	√
MTIC5W (input)	P10	√	×	×	√	×	×
	PB0	√	√	√	√	√	√
	PD5	√	√	√	√	√	√
MTIOC6A (input/output)	PE7	√	√	√	√	√	√
	PJ1	—	—	—	√	×	×
MTIOC6B (input/output)	PA5	√	√	√	√	√	√
	PJ0	—	—	—	√	×	×
MTIOC6C (input/output)	PE6	√	√	√	√	√	√
	P85	—	—	—	√	×	×
MTIOC6D (input/output)	PA0	√	√	√	√	√	√
	P84	—	—	—	√	×	×
MTIOC7A (input/output)	PA2	√	√	√	√	√	√
MTIOC7B (input/output)	PA1	√	√	√	√	√	√
MTIOC7C (input/output)	P67	√	√	×	√	√	×
MTIOC7D (input/output)	P66	√	√	×	√	√	×
MTIOC8A (input/output)	PD6	√	√	√	√	√	√
MTIOC8B (input/output)	PD4	√	√	√	√	√	√
MTIOC8C (input/output)	PD5	√	√	√	√	√	√
MTIOC8D (input/output)	PD3	√	√	√	√	√	√
MTCLKA (input)	P14	√	√	√	√	√	√
	P24	√	√	√	√	√	√
	PA4	√	√	√	√	√	√
	PC6	√	√	√	√	√	√
MTCLKB (input)	P15	√	√	√	√	√	√
	P25	√	√	√	√	√	√
	PA6	√	√	√	√	√	√
	PC7	√	√	√	√	√	√
MTCLKC (input)	P22	√	√	√	√	√	√
	PA1	√	√	√	√	√	√
	PC4	√	√	√	√	√	√

Pin Functions	Allocation Port	RX64M			RX65N		
		177 pin 176 pin	145 pin 144 pin	100 pin	177 pin 176 pin	145 pin 144 pin	100 pin
MTCLKD (input)	P23	√	√	√	√	√	√
	PA3	√	√	√	√	√	√
	PC5	√	√	√	√	√	√
POE0# (input)	P32	√	√	√	√	√	√
	P93	√	√	×	√	√	×
	PC4	√	√	√	√	√	√
	PD1	√	√	√	√	√	√
	PD7	√	√	√	√	√	√
POE4# (input)	P33	√	√	√	√	√	√
	P92	√	√	×	√	√	×
	PB5	√	√	√	√	√	√
	PD0	√	√	√	√	√	√
	PD6	√	√	√	√	√	√
POE8# (input)	P17	√	√	√	√	√	√
	P30	√	√	√	√	√	√
	PD3	√	√	√	√	√	√
	PE3	√	√	√	√	√	√
	PJ5	√	√	×	√	√	×
POE10# (input)	P32	√	√	√	√	√	√
	P34	√	√	√	√	√	√
	PA6	√	√	√	√	√	√
	PD5	√	√	√	√	√	√
POE11# (input)	P33	√	√	√	√	√	√
	PB3	√	√	√	√	√	√
	PD4	√	√	√	√	√	√
GTIOC0A (input/output)	P23	√	√	√	—	—	—
	P83	√	√	×	—	—	—
	PA5	√	√	√	—	—	—
	PD3	√	√	√	—	—	—
	PE5	√	√	√	—	—	—
GTIOC0B (input/output)	P17	√	√	√	—	—	—
	P81	√	√	×	—	—	—
	PA0	√	√	√	—	—	—
	PD2	√	√	√	—	—	—
	PE2	√	√	√	—	—	—
GTIOC1A (input/output)	P22	√	√	√	—	—	—
	PC5	√	√	√	—	—	—
	PA2	√	√	√	—	—	—
	PE4	√	√	√	—	—	—
	PD1	√	√	√	—	—	—

Pin Functions	Allocation Port	RX64M			RX65N		
		177 pin 176 pin	145 pin 144 pin	100 pin	177 pin 176 pin	145 pin 144 pin	100 pin
GTIOC1B (input/output)	P67	√	√	×	—	—	—
	P87	√	√	×	—	—	—
	PC3	√	√	√	—	—	—
	PD0	√	√	√	—	—	—
	PE1	√	√	√	—	—	—
GTIOC2A (input/output)	P21	√	√	√	—	—	—
	P82	√	√	×	—	—	—
	PA1	√	√	√	—	—	—
	PE3	√	√	√	—	—	—
GTIOC2B (input/output)	P66	√	√	×	—	—	—
	P86	√	√	×	—	—	—
	PC2	√	√	√	—	—	—
	PE0	√	√	√	—	—	—
GTIOC3A (input/output)	PC7	√	√	√	—	—	—
	PE7	√	√	√	—	—	—
GTIOC3B (input/output)	PC6	√	√	√	—	—	—
	PE6	√	√	√	—	—	—
GTETRG (input)	P15	√	√	√	—	—	—
	PC4	√	√	√	—	—	—
	PA6	√	√	√	—	—	—
TIOCA0 (input/output)	P86	√	√	×	√	√	×
	PA0	√	√	√	√	√	√
TIOCB0 (input/output)	P17	√	√	√	√	√	√
	PA1	√	√	√	√	√	√
TIOCC0 (input/output)	P32	√	√	√	√	√	√
	P85	—	—	—	√	×	×
TIOCD0 (input/output)	P33	√	√	√	√	√	√
	PA3	√	√	√	√	√	√
TIOCA1 (input/output)	P56	×	√	×	√	√	×
	PA4	√	√	√	√	√	√
TIOCB1 (input/output)	P16	√	√	√	√	√	√
	PA5	√	√	√	√	√	√
TIOCA2 (input/output)	P87	√	√	×	√	√	×
	PA6	√	√	√	√	√	√
TIOCB2 (input/output)	P15	√	√	√	√	√	√
	PA7	√	√	√	√	√	√
TIOCA3 (input/output)	P21	√	√	√	√	√	√
	PB0	√	√	√	√	√	√
TIOCB3 (input/output)	P20	√	√	√	√	√	√
	PB1	√	√	√	√	√	√
TIOCC3 (input/output)	P22	√	√	√	√	√	√
	PB2	√	√	√	√	√	√
TIOCD3 (input/output)	P23	√	√	√	√	√	√
	PB3	√	√	√	√	√	√

Pin Functions	Allocation Port	RX64M			RX65N		
		177 pin 176 pin	145 pin 144 pin	100 pin	177 pin 176 pin	145 pin 144 pin	100 pin
TIOCA4 (input/output)	P25	√	√	√	√	√	√
	PB4	√	√	√	√	√	√
TIOCB4 (input/output)	P24	√	√	√	√	√	√
	PB5	√	√	√	√	√	√
TIOCA5 (input/output)	P13	√	√	√	√	√	√
	PB6	√	√	√	√	√	√
TIOCB5 (input/output)	P14	√	√	√	√	√	√
	PB7	√	√	√	√	√	√
TCLKA (input)	P14	√	√	√	√	√	√
	PC2	√	√	√	√	√	√
TCLKB (input)	P15	√	√	√	√	√	√
	PA3	√	√	√	√	√	√
	PC3	√	√	√	√	√	√
TCLKC (input)	P16	√	√	√	√	√	√
	PB2	√	√	√	√	√	√
	PC0	√	√	√	√	√	√
TCLKD (input)	P17	√	√	√	√	√	√
	PB3	√	√	√	√	√	√
	PC1	√	√	√	√	√	√
PO0 (output)	P20	√	√	√	√	√	√
PO1 (output)	P21	√	√	√	√	√	√
PO2 (output)	P22	√	√	√	√	√	√
PO3 (output)	P23	√	√	√	√	√	√
PO4 (output)	P24	√	√	√	√	√	√
PO5 (output)	P25	√	√	√	√	√	√
PO6 (output)	P26	√	√	√	√	√	√
PO7 (output)	P27	√	√	√	√	√	√
PO8 (output)	P30	√	√	√	√	√	√
PO9 (output)	P31	√	√	√	√	√	√
PO10 (output)	P32	√	√	√	√	√	√
PO11 (output)	P33	√	√	√	√	√	√
PO12 (output)	P34	√	√	√	√	√	√
PO13 (output)	P13	√	√	√	√	√	√
	P15	√	√	√	√	√	√
PO14 (output)	P16	√	√	√	√	√	√
PO15 (output)	P14	√	√	√	√	√	√
	P17	√	√	√	√	√	√
PO16 (output)	P73	√	√	×	√	√	×
	PA0	√	√	√	√	√	√
PO17 (output)	PA1	√	√	√	√	√	√
	PC0	√	√	√	√	√	√
PO18 (output)	PA2	√	√	√	√	√	√
	PC1	√	√	√	√	√	√
	PE1	√	√	√	√	√	√

Pin Functions	Allocation Port	RX64M			RX65N		
		177 pin 176 pin	145 pin 144 pin	100 pin	177 pin 176 pin	145 pin 144 pin	100 pin
PO19 (output)	P74	√	√	×	√	√	×
	PA3	√	√	√	√	√	√
PO20 (output)	P75	√	√	×	√	√	×
	PA4	√	√	√	√	√	√
PO21 (output)	PA5	√	√	√	√	√	√
	PC2	√	√	√	√	√	√
PO22 (output)	P76	√	√	×	√	√	×
	PA6	√	√	√	√	√	√
PO23 (output)	P77	√	√	×	√	√	×
	PA7	√	√	√	√	√	√
	PE2	√	√	√	√	√	√
PO24 (output)	PB0	√	√	√	√	√	√
	PC3	√	√	√	√	√	√
PO25 (output)	PB1	√	√	√	√	√	√
	PC4	√	√	√	√	√	√
PO26 (output)	P80	√	√	×	√	√	×
	PB2	√	√	√	√	√	√
	PE3	√	√	√	√	√	√
PO27 (output)	P81	√	√	×	√	√	×
	PB3	√	√	√	√	√	√
PO28 (output)	P82	√	√	×	√	√	×
	PB4	√	√	√	√	√	√
	PE4	√	√	√	√	√	√
PO29 (output)	PB5	√	√	√	√	√	√
	PC5	√	√	√	√	√	√
PO30 (output)	PB6	√	√	√	√	√	√
	PC6	√	√	√	√	√	√
PO31 (output)	PB7	√	√	√	√	√	√
	PC7	√	√	√	√	√	√
TMO0 (output)	P22	√	√	√	√	√	√
	PB3	√	√	√	√	√	√
TMCI0 (input)	P01	√	√	×	√	√	×
	P21	√	√	√	√	√	√
	PB1	√	√	√	√	√	√
TMRI0 (input)	P00	√	√	×	√	√	×
	P20	√	√	√	√	√	√
	PA4	√	√	√	√	√	√
TMO1 (output)	P17	√	√	√	√	√	√
	P26	√	√	√	√	√	√
TMCI1 (input)	P02	√	√	×	√	√	×
	P12	√	√	√	√	√	√
	P54	×	√	√	√	√	√
	PC4	√	√	√	√	√	√

Pin Functions	Allocation Port	RX64M			RX65N		
		177 pin 176 pin	145 pin 144 pin	100 pin	177 pin 176 pin	145 pin 144 pin	100 pin
TMRI1 (input)	P24	√	√	√	√	√	√
	PB5	√	√	√	√	√	√
TMO2 (output)	P16	√	√	√	√	√	√
	PC7	√	√	√	√	√	√
TMCI2 (input)	P15	√	√	√	√	√	√
	P31	√	√	√	√	√	√
	PC6	√	√	√	√	√	√
TMRI2 (input)	P14	√	√	√	√	√	√
	PC5	√	√	√	√	√	√
TMO3 (output)	P13	√	√	√	√	√	√
	P32	√	√	√	√	√	√
	P55	×	√	√	√	√	√
TMCI3 (input)	P11	√	×	×	√	×	×
	P27	√	√	√	√	√	√
	P34	√	√	√	√	√	√
	PA6	√	√	√	√	√	√
TMRI3 (input)	P10	√	×	×	√	×	×
	P30	√	√	√	√	√	√
	P33	√	√	√	√	√	√
TOC0 (output)	PC7	√	√	√	√	√	√
TIC0 (input)	PC6	√	√	√	√	√	√
TOC1 (output)	PE7	√	√	√	√	√	√
TIC1 (input)	PE6	√	√	√	√	√	√
TOC2 (output)	PD3	√	√	√	√	√	√
TIC2 (input)	PD2	√	√	√	√	√	√
TOC3 (output)	PE3	√	√	√	√	√	√
TIC3 (input)	PE2	√	√	√	√	√	√
REF50CK0 (input)	P76	√	√	×	√	√	×
	PB2	√	√	√	√	√	√
	PE5	√	√	√	√	√	√
RMII0_CRS_DV (input)	P83	√	√	×	√	√	×
	PB7	√	√	√	√	√	√
RMII0_TXD0 (output)	P81	√	√	×	√	√	×
	PB5	√	√	√	√	√	√
RMII0_TXD1 (output)	P82	√	√	×	√	√	×
	PB6	√	√	√	√	√	√
RMII0_RXD0 (input)	P75	√	√	×	√	√	×
	PB1	√	√	√	√	√	√
RMII0_RXD1 (input)	P74	√	√	×	√	√	×
	PB0	√	√	√	√	√	√
RMII0_TXD_EN (output)	P80	√	√	×	√	√	×
	PA0	√	√	√	√	√	√
	PB4	√	√	√	√	√	√

Pin Functions	Allocation Port	RX64M			RX65N		
		177 pin 176 pin	145 pin 144 pin	100 pin	177 pin 176 pin	145 pin 144 pin	100 pin
RMII0_RX_ER (input)	P77	√	√	×	√	√	×
	PB3	√	√	√	√	√	√
ET0_CRS (input)	P83	√	√	×	√	√	×
	PB7	√	√	√	√	√	√
ET0_RX_DV (input)	PC2	√	√	√	√	√	√
ET0_EXOUT (output)	P55	×	√	√	√	√	√
	PA6	√	√	√	√	√	√
	PJ3	√	√	√	√	√	√
ET0_LINKSTA (input)	P34	√	√	√	√	√	√
	P54	×	√	√	√	√	√
	PA5	√	√	√	√	√	√
ET0_ETXD0 (output)	P81	√	√	×	√	√	×
	PB5	√	√	√	√	√	√
ET0_ETXD1 (output)	P82	√	√	×	√	√	×
	PB6	√	√	√	√	√	√
ET0_ETXD2 (output)	PC5	√	√	√	√	√	√
ET0_ETXD3 (output)	PC6	√	√	√	√	√	√
ET0_ERXD0 (input)	P75	√	√	×	√	√	×
	PB1	√	√	√	√	√	√
ET0_ERXD1 (input)	P74	√	√	×	√	√	×
	PB0	√	√	√	√	√	√
ET0_ERXD2 (input)	PC1	√	√	√	√	√	√
	PE4	√	√	√	√	√	√
ET0_ERXD3 (input)	PC0	√	√	√	√	√	√
	PE3	√	√	√	√	√	√
ET0_TX_EN (output)	P80	√	√	×	√	√	×
	PA0	√	√	√	√	√	√
	PB4	√	√	√	√	√	√
ET0_TX_ER (output)	PC3	√	√	√	√	√	√
ET0_RX_ER (input)	P77	√	√	×	√	√	×
	PB3	√	√	√	√	√	√
ET0_TX_CLK (input)	PC4	√	√	√	√	√	√
ET0_RX_CLK (input)	P76	√	√	×	√	√	×
	PB2	√	√	√	√	√	√
	PE5	√	√	√	√	√	√
ET0_COL (input)	PC7	√	√	√	√	√	√
ET0_WOL (output)	P73	√	√	×	√	√	×
	PA1	√	√	√	√	√	√
	PA7	√	√	√	√	√	√
ET0_MDC (output)	P72	√	√	×	√	√	×
	PA4	√	√	√	√	√	√
ET0_MDIO (input/output)	P71	√	√	×	√	√	×
	PA3	√	√	√	√	√	√

Pin Functions	Allocation Port	RX64M			RX65N		
		177 pin 176 pin	145 pin 144 pin	100 pin	177 pin 176 pin	145 pin 144 pin	100 pin
REF50CK1 (input)	PG0	√	×	×	—	—	—
RMII1_CRS_DV (input)	P92	√	×	×	—	—	—
RMII1_TXD0 (output)	PG3	√	×	×	—	—	—
RMII1_TXD1 (output)	PG4	√	×	×	—	—	—
RMII1_RXD0 (input)	P94	√	×	×	—	—	—
RMII1_RXD1 (input)	P95	√	×	×	—	—	—
RMII1_TXD_EN (output)	P60	√	×	×	—	—	—
RMII1_RX_ER (input)	PG1	√	×	×	—	—	—
ET1_CRS (input)	P92	√	×	×	—	—	—
ET1_RX_DV (input)	P90	√	×	×	—	—	—
ET1_EXOUT (output)	P26	√	×	×	—	—	—
ET1_LINKSTA (input)	P93	√	×	×	—	—	—
ET1_ETXD0 (output)	PG3	√	×	×	—	—	—
ET1_ETXD1 (output)	PG4	√	×	×	—	—	—
ET1_ETXD2 (output)	PG5	√	×	×	—	—	—
ET1_ETXD3 (output)	PG6	√	×	×	—	—	—
ET1_ERXD0 (input)	P94	√	×	×	—	—	—
ET1_ERXD1 (input)	P95	√	×	×	—	—	—
ET1_ERXD2 (input)	P96	√	×	×	—	—	—
ET1_ERXD3 (input)	P97	√	×	×	—	—	—
ET1_TX_EN (output)	P60	√	×	×	—	—	—
ET1_TX_ER (output)	PG7	√	×	×	—	—	—
ET1_RX_ER (input)	PG1	√	×	×	—	—	—
ET1_TX_CLK (input)	PG2	√	×	×	—	—	—
ET1_RX_CLK (input)	PG0	√	×	×	—	—	—
ET1_COL (input)	P91	√	×	×	—	—	—
ET1_WOL (output)	P27	√	×	×	—	—	—
ET1_MDC (output)	P31	√	×	×	—	—	—
ET1_MDIO (input/output)	P30	√	×	×	—	—	—
RXD0 (input)/ SMISO0 (input/output)/ SSCL0 (input/output)	P21	√	√	√	√	√	√
	P33	√	√	√	√	√	√
TXD0 (output)/ SMOSI0 (input/output)/ SSDA0 (input/output)	P20	√	√	√	√	√	√
	P32	√	√	√	√	√	√
SCK0 (input/output)	P22	√	√	√	√	√	√
	P34	√	√	√	√	√	√
CTS0# (input)/ RTS0# (output)/ SS0# (input)	P23	√	√	√	√	√	√
	PJ3	√	√	√	√	√	√

Pin Functions	Allocation Port	RX64M			RX65N		
		177 pin 176 pin	145 pin 144 pin	100 pin	177 pin 176 pin	145 pin 144 pin	100 pin
RXD1 (input)/ SMISO1 (input/output)/ SSCL1 (input/output)	P15	√	√	√	√	√	√
	P30	√	√	√	√	√	√
	PF2	√	×	×	√	×	×
TXD1 (output)/ SMOSI1 (input/output)/ SSDA1 (input/output)	P16	√	√	√	√	√	√
	P26	√	√	√	√	√	√
	PF0	√	×	×	√	×	×
SCK1 (input/output)	P17	√	√	√	√	√	√
	P27	√	√	√	√	√	√
	PF1	√	×	×	√	×	×
CTS1# (input)/ RTS1# (output)/ SS1# (input)	P14	√	√	√	√	√	√
	P31	√	√	√	√	√	√
RXD2 (input)/ SMISO2 (input/output)/ SSCL2 (input/output)	P12	√	√	√	√	√	√
	P52	√	√	√	√	√	√
TXD2 (output)/ SMOSI2 (input/output)/ SSDA2 (input/output)	P13	√	√	√	√	√	√
	P50	√	√	√	√	√	√
SCK2 (input/output)	P11	√	×	×	√	×	×
	P51	√	√	√	√	√	√
CTS2# (input)/ RTS2# (output)/ SS2# (input)	P54	×	√	√	√	√	√
	PJ5	√	√	×	√	√	×
RXD3 (input)/ SMISO3 (input/output)/ SSCL3 (input/output)	P16	√	√	√	√	√	√
	P25	√	√	√	√	√	√
TXD3 (output)/ SMOSI3 (input/output)/ SSDA3 (input/output)	P17	√	√	√	√	√	√
	P23	√	√	√	√	√	√
SCK3 (input/output)	P15	√	√	√	√	√	√
	P24	√	√	√	√	√	√
CTS3# (input)/ RTS3# (output)/ SS3# (input)	P26	√	√	√	√	√	√
RXD4 (input)/ SMISO4 (input/output)/ SSCL4 (input/output)	PB0	√	√	×	√	√	×
TXD4 (output)/ SMOSI4 (input/output)/ SSDA4 (input/output)	PB1	√	√	×	√	√	×
SCK4 (input/output)	PB3	√	√	×	√	√	×
CTS4# (input)/ RTS4# (output)/ SS4# (input)	PB2	√	√	×	√	√	×

Pin Functions	Allocation Port	RX64M			RX65N		
		177 pin 176 pin	145 pin 144 pin	100 pin	177 pin 176 pin	145 pin 144 pin	100 pin
RXD5 (input)/ SMISO5 (input/output)/ SSCL5 (input/output)	PA2	√	√	√	√	√	√
	PA3	√	√	√	√	√	√
	PC2	√	√	√	√	√	√
TXD5 (output)/ SMOSI5 (input/output)/ SSDA5 (input/output)	PA4	√	√	√	√	√	√
	PC3	√	√	√	√	√	√
SCK5 (input/output)	PA1	√	√	√	√	√	√
	PC1	√	√	√	√	√	√
	PC4	√	√	√	√	√	√
CTS5# (input)/ RTS5# (output)/ SS5# (input)	PA6	√	√	√	√	√	√
	PC0	√	√	√	√	√	√
RXD6 (input)/ SMISO6 (input/output)/ SSCL6 (input/output)	P01	√	√	×	√	√	×
	P33	√	√	√	√	√	√
	PB0	√	√	√	√	√	√
TXD6 (output)/ SMOSI6 (input/output)/ SSDA6 (input/output)	P00	√	√	×	√	√	×
	P32	√	√	√	√	√	√
	PB1	√	√	√	√	√	√
SCK6 (input/output)	P02	√	√	×	√	√	×
	P34	√	√	√	√	√	√
	PB3	√	√	√	√	√	√
CTS6# (input)/ RTS6# (output)/ SS6# (input)	PB2	√	√	√	√	√	√
	PJ3	√	√	√	√	√	√
RXD7 (input)/ SMISO7 (input/output)/ SSCL7 (input/output)	P57	—	—	—	√	×	×
	P92	√	√	×	√	√	×
TXD7 (output)/ SMOSI7 (input/output)/ SSDA7 (input/output)	P55	—	—	—	√	√	×
	P90	√	√	×	√	√	×
SCK7 (input/output)	P56	—	—	—	√	√	×
	P91	√	√	×	√	√	×
CTS7# (input)/ RTS7# (output)/ SS7# (input)	P93	√	√	×	√	√	×
RXD8 (input) / SMISO8 (input/output)/ SSCL8 (input/output)	PC6	√	√	√	√	√	√
	PJ1	—	—	—	√	×	×
TXD8 (output) / SMOSI8 (input/output)/ SSDA8 (input/output)	PC7	√	√	√	√	√	√
	PJ2	—	—	—	√	×	×

Pin Functions	Allocation Port	RX64M			RX65N		
		177 pin 176 pin	145 pin 144 pin	100 pin	177 pin 176 pin	145 pin 144 pin	100 pin
SCK8 (input/output)/	PC5	√	√	√	√	√	√
RTS8# (output)	PJ0	—	—	—	√	×	×
CTS8# (input) / RTS8# (output)/ SS8# (input)	PC4	√	√	√	√	√	√
RXD9 (input) / SMISO9 (input/output)/ SSCL9 (input/output)	PB6	√	√	√	√	√	√
TXD9 (output) / SMOSI9 (input/output)/ SSDA9 (input/output)	PB7	√	√	√	√	√	√
SCK9 (input/output)/ RTS9# (output)	PB5	√	√	√	√	√	√
CTS9# (input) / RTS9# (output)/ SS9# (input)	PB4	√	√	√	√	√	√
RXD10 (input) /	P81	√	√	×	√	√	×
SMISO10 (input/output)/	P86	√	√	×	√	√	×
SSCL10 (input/output)	PC6	—	—	—	√	√	√
TXD10 (output)/	P82	√	√	×	√	√	×
SMOSI10 (input/output)/	P87	√	√	×	√	√	×
SSDA10 (input/output)	PC7	—	—	—	√	√	√
SCK10 (input/output)	P80	√	√	×	√	√	×
	P83	√	√	×	√	√	×
	PC5	—	—	—	√	√	√
RTS10# (output)	P80	√	√	×	√	√	×
CTS10# (input)/ SS10#(input)	P83	√	√	×	√	√	×
CTS10# (input)/ RTS10# (output)/ SS10# (input)	PC4	—	—	—	√	√	√
RXD11 (input) /	P76	√	√	×	√	√	×
SMISO11 (input/output)/ SSCL11 (input/output)	PB6	—	—	—	√	√	√
TXD11 (output)/	P77	√	√	×	√	√	×
SMOSI11 (input/output)/ SSDA11 (input/output)	PB7	—	—	—	√	√	√
SCK11 (input/output)/	P75	√	√	×	√	√	×
RTS11# (output)	PB5	—	—	—	√	√	√
CTS11# (input)/ SS11#(input)	P74	√	√	×	√	√	×
CTS11# (input)/ RTS11# (output)/ SS11#(input)	PB4	—	—	—	√	√	√

Pin Functions	Allocation Port	RX64M			RX65N		
		177 pin 176 pin	145 pin 144 pin	100 pin	177 pin 176 pin	145 pin 144 pin	100 pin
RXD12 (input)/ SMISO12 (input/output)/ SSCL12 (input/output)/ RXDX12 (input)	PE2	√	√	√	√	√	√
TXD12 (output)/ SMOSI12 (input/output)/ SSDA12 (input/output)/ TXDX12 (output)/ SIOX12 (input/output)	PE1	√	√	√	√	√	√
SCK12 (input/output)	PE0	√	√	√	√	√	√
CTS12# (input)/ RTS12# (output)/ SS12# (input)	PE3	√	√	√	√	√	√
SCL0[FM+] (input/output)	P12	√	√	√	√	√	√
SDA0[FM+] (input/output)	P13	√	√	√	√	√	√
SCL1 (input/output)	P21	—	—	—	√	√	×
SDA1 (input/output)	P20	—	—	—	√	√	×
SCL2-DS (input/output)	P16	√	√	√	√	√	√
SDA2-DS (input/output)	P17	√	√	√	√	√	√
USB0_VBUS (input)	P16	√	√	√	√	√	√
USB0_EXICEN (output)	P21	√	√	√	√	√	√
USB0_VBUSEN (output)	P16	√	√	√	√	√	√
	P24	√	√	√	√	√	√
	P32	√	√	√	√	√	√
USB0_OVRCURA (input)	P14	√	√	√	√	√	√
USB0_OVRCURB (input)	P16	√	√	√	√	√	√
	P22	√	√	√	√	√	√
USB0_ID (input)	P20	√	√	√	√	√	√
USBA_VBUS (input)	P11	√	×	×	—	—	—
USBA_EXICEN (output)	P21	√	×	×	—	—	—
USBA_VBUSEN (output)	P11	√	×	×	—	—	—
	P15	√	×	×	—	—	—
USBA_OVRCURA (input)	P10	√	×	×	—	—	—
USBA_OVRCURB (input)	P22	√	×	×	—	—	—
USBA_ID (input)	P20	√	×	×	—	—	—
CRX0 (input)	P33	√	√	√	√	√	√
	PD2	√	√	√	√	√	√
CTX0 (output)	P32	√	√	√	√	√	√
	PD1	√	√	√	√	√	√
CRX1-DS (input)	P15	√	√	√	√	√	√
CRX1 (input)	P55	×	√	√	×	√	√
CTX1 (output)	P14	√	√	√	√	√	√
	P54	×	√	√	×	√	√
CRX2 (input)	P67	√	√	×	—	—	—
CTX2 (output)	P66	√	√	×	—	—	—

Pin Functions	Allocation Port	RX64M			RX65N		
		177 pin 176 pin	145 pin 144 pin	100 pin	177 pin 176 pin	145 pin 144 pin	100 pin
RSPCKA (input/output)	PA5	√	√	√	√	√	√
	PC5	√	√	√	√	√	√
MOSIA (input/output)	PA6	√	√	√	√	√	√
	PC6	√	√	√	√	√	√
MISOA (input/output)	PA7	√	√	√	√	√	√
	PC7	√	√	√	√	√	√
SSLA0 (input/output)	PA4	√	√	√	√	√	√
	PC4	√	√	√	√	√	√
SSLA1 (output)	PA0	√	√	√	√	√	√
	PC0	√	√	√	√	√	√
SSLA2 (output)	PA1	√	√	√	√	√	√
	PC1	√	√	√	√	√	√
SSLA3 (output)	PA2	√	√	√	√	√	√
	PC2	√	√	√	√	√	√
RSPCKB (input/output)	P27	—	—	—	√	√	√
	PE5	—	—	—	√	√	√
MOSIB (input/output)	P26	—	—	—	√	√	√
	PE6	—	—	—	√	√	√
MISOB (input/output)	P30	—	—	—	√	√	√
	PE7	—	—	—	√	√	√
SSLB0 (input/output)	P31	—	—	—	√	√	√
	PE4	—	—	—	√	√	√
SSLB1 (output)	P50	—	—	—	√	√	√
	PE0	—	—	—	√	√	√
SSLB2 (output)	P51	—	—	—	√	√	√
	PE1	—	—	—	√	√	√
SSLB3 (output)	P52	—	—	—	√	√	√
	PE2	—	—	—	√	√	√
RSPCKC (input/output)	P56	—	—	—	√	×	×
	PD3	—	—	—	√	√	√
MOSIC (input/output)	P54	—	—	—	√	×	×
	PD1	—	—	—	√	√	√
MISOC (input/output)	P55	—	—	—	√	×	×
	PD2	—	—	—	√	√	√
SSLC0 (input/output)	P57	—	—	—	√	×	×
	PD4	—	—	—	√	√	√
SSLC1 (output)	PD5	—	—	—	√	√	√
	PJ0	—	—	—	√	×	×
SSLC2 (output)	PD6	—	—	—	√	√	√
	PJ1	—	—	—	√	×	×
SSLC3 (output)	PD7	—	—	—	√	√	√
	PJ2	—	—	—	√	×	×

Pin Functions	Allocation Port	RX64M			RX65N		
		177 pin 176 pin	145 pin 144 pin	100 pin	177 pin 176 pin	145 pin 144 pin	100 pin
RTCOUT (output)	P16	√	√	√	√	√	√
	P32	√	√	√	√	√	√
RTCIC0 (input)	P30	√	√	√	√	√	√
RTCIC1 (input)	P31	√	√	√	√	√	√
RTCIC2 (input)	P32	√	√	√	√	√	√
AN000 (input)	P40	√	√	√	√	√	√
AN001 (input)	P41	√	√	√	√	√	√
AN002 (input)	P42	√	√	√	√	√	√
AN003 (input)	P43	√	√	√	√	√	√
AN004 (input)	P44	√	√	√	√	√	√
AN005 (input)	P45	√	√	√	√	√	√
AN006 (input)	P46	√	√	√	√	√	√
AN007 (input)	P47	√	√	√	√	√	√
ADTRG0# (input)	P07	√	√	√	√	√	√
	P16	√	√	√	√	√	√
	P25	√	√	√	√	√	√
AN100 (input)	PE2	√	√	√	√	√	√
AN101 (input)	PE3	√	√	√	√	√	√
AN102 (input)	PE4	√	√	√	√	√	√
AN103 (input)	PE5	√	√	√	√	√	√
AN104 (input)	PE6	√	√	√	√	√	√
AN105 (input)	PE7	√	√	√	√	√	√
AN106 (input)	PD6	√	√	√	√	√	√
AN107 (input)	PD7	√	√	√	√	√	√
AN108 (input)	PD0	√	√	√	√	√	√
AN109 (input)	PD1	√	√	√	√	√	√
AN110 (input)	PD2	√	√	√	√	√	√
AN111 (input)	PD3	√	√	√	√	√	√
AN112 (input)	PD4	√	√	√	√	√	√
AN113 (input)	PD5	√	√	√	√	√	√
AN114 (input)	P90	√	√	×	√	√	×
AN115 (input)	P91	√	√	×	√	√	×
AN116 (input)	P92	√	√	×	√	√	×
AN117 (input)	P93	√	√	×	√	√	×
AN118 (input)	P00	√	√	×	√	√	×
AN119 (input)	P01	√	√	×	√	√	×
AN120 (input)	P02	√	√	×	√	√	×
ANEX0 (output)	PE0	√	√	√	√	√	√
ANEX1 (input)	PE1	√	√	√	√	√	√
ADTRG1# (input)	P13	√	√	√	√	√	√
	P17	√	√	√	√	√	√
DA0 (output)	P03	√	√	×	√	√	×
DA1 (output)	P05	√	√	√	√	√	√

Pin Functions	Allocation Port	RX64M			RX65N		
		177 pin 176 pin	145 pin 144 pin	100 pin	177 pin 176 pin	145 pin 144 pin	100 pin
PIXCLK (input)	P24	√	√	×	√	√	×
VSYNC (input)	P32	√	√	×	√	√	×
HSYNC (input)	P25	√	√	×	√	√	×
PIXD0 (input)	P15	√	√	×	√	√	×
PIXD1 (input)	P86	√	√	×	√	√	×
PIXD2 (input)	P87	√	√	×	√	√	×
PIXD3 (input)	P17	√	√	×	√	√	×
PIXD4 (input)	P20	√	√	×	√	√	×
PIXD5 (input)	P21	√	√	×	√	√	×
PIXD6 (input)	P22	√	√	×	√	√	×
PIXD7 (input)	P23	√	√	×	√	√	×
PCKO (output)	P33	√	√	×	√	√	×
SSISCK0 (input/output)	P23	√	√	√	—	—	—
SSIWS0 (input/output)	P21	√	√	√	—	—	—
SSIRXD0 (output)	P20	√	√	√	—	—	—
SSITXD0 (output)	P17	√	√	√	—	—	—
SSISCK1 (input/output)	P24	√	√	√	—	—	—
SSIWS1 (input/output)	P15	√	√	√	—	—	—
SSIDATA1 (input/output)	P25	√	√	√	—	—	—
AUDIO_CLK (input)	P22	√	√	√	—	—	—
MMC_RES# (output)	P75	√	√	×	√	√	×
	PE7	√	√	√	√	√	√
MMC_CLK (output)	P77	√	√	×	√	√	×
	PD5	√	√	√	√	√	√
MMC_CD (input)	PC2	√	√	×	√	√	×
	PE6	√	√	√	√	√	√
MMC_CMD (input/output)	P76	√	√	×	√	√	×
	PD4	√	√	√	√	√	√
MMC_D0 (input/output)	PC3	√	√	×	√	√	×
	PD6	√	√	√	√	√	√
MMC_D1 (input/output)	PC4	√	√	×	√	√	×
	PD7	√	√	√	√	√	√
MMC_D2 (input/output)	P80	√	√	×	√	√	×
	PD2	√	√	√	√	√	√
MMC_D3 (input/output)	P81	√	√	×	√	√	×
	PD3	√	√	√	√	√	√
MMC_D4 (input/output)	P82	√	√	×	√	√	×
	PE0	√	√	√	√	√	√
MMC_D5 (input/output)	PC5	√	√	×	√	√	×
	PE1	√	√	√	√	√	√
MMC_D6 (input/output)	PC6	√	√	×	√	√	×
	PE2	√	√	√	√	√	√
MMC_D7 (input/output)	PC7	√	√	×	√	√	×
	PE3	√	√	√	√	√	√

Pin Functions	Allocation Port	RX64M			RX65N		
		177 pin 176 pin	145 pin 144 pin	100 pin	177 pin 176 pin	145 pin 144 pin	100 pin
SDHI_CLK (output)	P21	—	—	—	√	√	×
	P77	√	√	×	√	√	×
	PD5	√	√	√	√	√	√
SDHI_CMD (input/output)	P20	—	—	—	√	√	×
	P76	√	√	×	√	√	×
	PD4	√	√	√	√	√	√
SDHI_CD (input)	P25	—	—	—	√	√	×
	P81	√	√	×	√	√	×
	PE6	√	√	√	√	√	√
SDHI_WP (input)	P24	—	—	—	√	√	×
	P80	√	√	×	√	√	×
	PE7	√	√	√	√	√	√
SDHI_D0 (input/output)	P22	—	—	—	√	√	×
	PC3	√	√	×	√	√	×
	PD6	√	√	√	√	√	√
SDHI_D1 (input/output)	P23	—	—	—	√	√	×
	PC4	√	√	×	√	√	×
	PD7	√	√	√	√	√	√
SDHI_D2 (input/output)	P75	√	√	×	√	√	×
	P87	—	—	—	√	√	×
	PD2	√	√	√	√	√	√
SDHI_D3 (input/output)	P17	—	—	—	√	√	×
	PC2	√	√	×	√	√	×
	PD3	√	√	√	√	√	√
SDSI_CLK (input)	P77	—	—	—	√	√	×
	PB5	—	—	—	√	√	√
SDSI_CMD (input/output)	P76	—	—	—	√	√	×
	PB4	—	—	—	√	√	√
SDSI_D0 (input/output)	PC3	—	—	—	√	√	×
	PB6	—	—	—	√	√	√
SDSI_D1 (input/output)	PC4	—	—	—	√	√	×
	PB7	—	—	—	√	√	√
SDSI_D2 (input/output)	P75	—	—	—	√	√	×
	PB2	—	—	—	√	√	√
SDSI_D3 (input/output)	PC2	—	—	—	√	√	×
	PB3	—	—	—	√	√	√
CACREF (input)	PC7	√	√	√	√	√	√
	PA0	√	√	√	√	√	√
QSPCLK (input/output)	P77	√	√	×	√	√	×
	PD5	√	√	√	√	√	√
QSSL (input/output)	P76	√	√	×	√	√	×
	PD4	√	√	√	√	√	√
QMO/QIO0 (input/output)	PC3	√	√	×	√	√	×
	PD6	√	√	√	√	√	√

Pin Functions	Allocation Port	RX64M			RX65N		
		177 pin 176 pin	145 pin 144 pin	100 pin	177 pin 176 pin	145 pin 144 pin	100 pin
QMI/QIO1 (input/output)	PC4	√	√	×	√	√	×
	PD7	√	√	√	√	√	√
QIO2 (input/output)	P80	√	√	×	√	√	×
	PD2	√	√	√	√	√	√
QIO3 (input/output)	P81	√	√	×	√	√	×
	PD3	√	√	√	√	√	√
LCD_EXTCLK (input)*1	P73	—	—	—	√	×	×
	PD0	—	—	—	√	√	√
LCD_CLK (output)*1	P14	—	—	—	√	×	×
	PB5	—	—	—	√	√	√
LCD_TCON0 (output)*1	P13	—	—	—	√	×	×
	PB4	—	—	—	√	√	√
LCD_TCON1 (output)*1	P12	—	—	—	√	×	×
	PB3	—	—	—	√	√	√
LCD_TCON2 (output)*1	PB2	—	—	—	√	√	√
	PJ2	—	—	—	√	×	×
LCD_TCON3 (output)*1	PB1	—	—	—	√	√	√
	PJ1	—	—	—	√	×	×
LCD_DATA0 (output)*1	PB0	—	—	—	√	√	√
	PJ0	—	—	—	√	×	×
LCD_DATA1 (output)*1	P85	—	—	—	√	×	×
	PA7	—	—	—	√	√	√
LCD_DATA2 (output)*1	P84	—	—	—	√	×	×
	PA6	—	—	—	√	√	√
LCD_DATA3 (output)*1	P57	—	—	—	√	×	×
	PA5	—	—	—	√	√	√
LCD_DATA4 (output)*1	P56	—	—	—	√	×	×
	PA4	—	—	—	√	√	√
LCD_DATA5 (output)*1	P55	—	—	—	√	×	×
	PA3	—	—	—	√	√	√
LCD_DATA6 (output)*1	P54	—	—	—	√	×	×
	PA2	—	—	—	√	√	√
LCD_DATA7 (output)*1	P11	—	—	—	√	×	×
	PA1	—	—	—	√	√	√
LCD_DATA8 (output)*1	P83	—	—	—	√	×	×
	PA0	—	—	—	√	√	√
LCD_DATA9 (output)*1	PC7	—	—	—	√	×	×
	PE7	—	—	—	√	√	√
LCD_DATA10 (output)*1	PC6	—	—	—	√	×	×
	PE6	—	—	—	√	√	√
LCD_DATA11 (output)*1	PC5	—	—	—	√	×	×
	PE5	—	—	—	√	√	√
LCD_DATA12 (output)*1	P82	—	—	—	√	×	×
	PE4	—	—	—	√	√	√

Pin Functions	Allocation Port	RX64M			RX65N		
		177 pin 176 pin	145 pin 144 pin	100 pin	177 pin 176 pin	145 pin 144 pin	100 pin
LCD_DATA13 (output)*1	P81	—	—	—	√	×	×
	PE3	—	—	—	√	√	√
LCD_DATA14 (output)*1	P80	—	—	—	√	×	×
	PE2	—	—	—	√	√	√
LCD_DATA15 (output)*1	PC4	—	—	—	√	×	×
	PE1	—	—	—	√	√	√
LCD_DATA16 (output)*1	PC3	—	—	—	√	×	×
	PE0	—	—	—	√	√	√
LCD_DATA17 (output)*1	P77	—	—	—	√	×	×
	PD7	—	—	—	√	√	√
LCD_DATA18 (output)*1	P76	—	—	—	√	×	×
	PD6	—	—	—	√	√	√
LCD_DATA19 (output)*1	PC2	—	—	—	√	×	×
	PD5	—	—	—	√	√	√
LCD_DATA20 (output)*1	P75	—	—	—	√	×	×
	PD4	—	—	—	√	√	√
LCD_DATA21 (output)*1	P74	—	—	—	√	×	×
	PD3	—	—	—	√	√	√
LCD_DATA22 (output)*1	PC1	—	—	—	√	×	×
	PD2	—	—	—	√	√	√
LCD_DATA23 (output)*1	P72	—	—	—	√	×	×
	PD1	—	—	—	√	√	√

*1: Can be used for products with at least 1.5 Mbytes of code flash memory.

Table 2.25 Comparative Listing of Multi-Function Pin Controller Registers

Register	Bit	RX64M	RX65N
PmnPFS	—	Refer to the user's manual for descriptions of the pin function control registers.	
PFCSS0	CS0S	CS0# Output Pin Select 0: Set P60 as CS0# output pin 1: Set PC7 as CS0# output pin Note. P60 is not present in 100-pin products. Thus, even if this bit is set to "0b", PC7 is set as CS0# output pin.	CS0# Output Pin Select 0: Set P60 as CS0# output pin 1: Set PC7 as CS0# output pin Note. P60 is not present in 100-pin products. When CS0# output is used, set this bit to 1.
	CS1S[1:0]	CS1# Output Pin Select b3 b2 0 0: Set P61 as CS1# output pin 0 1: Set P71 as CS1# output pin 1 X: Set PC6 as CS1# output pin Note. P61 and P71 are not present in 100-pin products. Thus, even if these bits are set to other than "1xb", PC6 is set as CS1# output pin.	CS1# Output Pin Select b3 b2 0 0: Set P61 as CS1# output pin 0 1: Set P71 as CS1# output pin 1 X: Set PC6 as CS1# output pin Note. P61 and P71 are not present in 100-pin products. When CS1# output is used, set these bits to 1xb.
	CS2S[1:0]	CS2# Output Pin Select b5 b4 0 0: Set P62 as CS2# output pin 0 1: Set P72 as CS2# output pin 1 X: Set PC5 as CS2# output pin Note. P62 and P72 are not present in 100-pin products. Thus, even if these bits are set to other than "1xb", PC5 is set as CS2# output pin.	CS2# Output Pin Select b5 b4 0 0: Set P62 as CS2# output pin 0 1: Set P72 as CS2# output pin 1 X: Set PC5 as CS2# output pin Note. P62 and P72 are not present in 100-pin products. When CS2# output is used, set these bits to 1xb.
	CS3S[1:0]	CS3# Output Pin Select b7 b6 0 0: Set P63 as CS3# output pin 0 1: Set P73 as CS3# output pin 1 X: Set PC4 as CS3# output pin Note. P63 and P73 are not present in 100-pin products. Thus, even if these bits are set to other than "1xb", PC4 is set as CS3# output pin.	CS3# Output Pin Select b7 b6 0 0: Set P63 as CS3# output pin 0 1: Set P73 as CS3# output pin 1 X: Set PC4 as CS3# output pin Note. P63 and P73 are not present in 100-pin products. When CS3# output is used, set these bits to 1xb.

Register	Bit	RX64M	RX65N
PFCSS1	CS4S[1:0]	CS4# Output Pin Select b1 b0 0 0: Set P64 as CS4# output pin 0 1: Set P74 as CS4# output pin 1 X: Set P24 as CS4# output pin Note. P64 and P74 are not present in 100-pin products. Thus, even if these bits are set to other than “1xb”, P24 is set as CS4# output pin.	CS4# Output Pin Select b1 b0 0 0: Set P64 as CS4# output pin 0 1: Set P74 as CS4# output pin 1 X: Set P24 as CS4# output pin Note. P64 and P74 are not present in 100-pin products. When CS4# output is used, set these bits to 1xb.
	CS5S[1:0]	CS5# Output Pin Select b3 b2 0 0: Set P65 as CS5# output pin 0 1: Set P75 as CS5# output pin 1 X: Set P25 as CS5# output pin Note. P65 and P75 are not present in 100-pin products. Thus, even if these bits are set to other than “1xb”, P25 is set as CS5# output pin.	CS5# Output Pin Select b3 b2 0 0: Set P65 as CS5# output pin 0 1: Set P75 as CS5# output pin 1 X: Set P25 as CS5# output pin Note. P65 and P75 are not present in 100-pin products. When CS5# output is used, set these bits to 1xb.
	CS6S[1:0]	CS6# Output Pin Select b5 b4 0 0: Set P66 as CS6# output pin 0 1: Set P76 as CS6# output pin 1 X: Set P26 as CS6# output pin Note. P66 and P76 are not present in 100-pin products. Thus, even if these bits are set to other than “1xb”, P26 is set as CS6# output pin.	CS6# Output Pin Select b5 b4 0 0: Set P66 as CS6# output pin 0 1: Set P76 as CS6# output pin 1 X: Set P26 as CS6# output pin Note. P66 and P76 are not present in 100-pin products. When CS6# output is used, set these bits to 1xb.
	CS7S[1:0]	CS7# Output Pin Select b7 b6 0 0: Set P67 as CS7# output pin 0 1: Set P77 as CS7# output pin 1 X: Set P27 as CS7# output pin Note. P67 and P77 are not present in 100-pin products. Thus, even if these bits are set to other than “1xb”, P27 is set as CS7# output pin.	CS7# Output Pin Select b7 b6 0 0: Set P67 as CS7# output pin 0 1: Set P77 as CS7# output pin 1 X: Set P27 as CS7# output pin Note. P67 and P77 are not present in 100-pin products. When CS7# output is used, set these bits to 1xb.
PFBCR0	DH32E	D16 to D31 output enable bit	D16 to D31 Output Enable *1
	WR32BC32E	WR3#/BC3# output enable bit WR2#/BC2# output enable bit	WR3#/BC3# and WR2#/BC2# Output Enable *1
PFBCR1	ALES	ALE select bit	ALE select bit *1
PFBCR2	—	—	External Bus Control Register 2 *1
PFBCR3	—	—	External Bus Control Register 3 *1
PFENET	PHYMODE1	Ethernet channel 1 mode setting bit	—

*1: Can be used for products with at least 1.5 Mbytes of code flash memory.

2.12 Port Output Enable

Table 2.26 shows a comparative overview of port output enable specifications, and Table 2.27 shows a comparative listing of the port output enable registers.

Table 2.26 Comparative Overview of Port Output Enable

Item	RX64M (POE3)	RX65N (POE3a)
Target pins for switching to high-impedance state	• MTU output pins MTU0 pins (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) MTU3 pins (MTIOC3B, MTIOC3D) MTU4 pins (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) MTU6 pins (MTIOC6B, MTIOC6D) MTU7 pins (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D) • GPT output pins GPT0 pins (GTIOC0A, GTIOC0B) GPT1 pins (GTIOC1A, GTIOC1B) GPT2 pins (GTIOC2A, GTIOC2B) GPT3 pins (GTIOC3A, GTIOC3B)	• MTU output pins MTU0 pins (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) MTU3 pins (MTIOC3B, MTIOC3D) MTU4 pins (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) MTU6 pins (MTIOC6B, MTIOC6D) MTU7 pins (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D)
Generating conditions of request for switching to high-impedance state	• Change to input pin When input is received on POE0# POE4#, POE8#, POE10#, or POE11# • Shorting of output pins When a match (short circuit) occurs between the output signal levels (active level) over one or more cycles on the following combination of pins: MTIOC3B and MTIOC3D MTIOC4A and MTIOC4C MTIOC4B and MTIOC4D MTIOC6B and MTIOC6D MTIOC7A and MTIOC7C MTIOC7B and MTIOC7D GTIOC0A and GTIOC0B GTIOC1A and GTIOC1B GTIOC2A and GTIOC2B • When a register setting is made • When clock generation circuit oscillation stop is detected	• Change to input pin When input is received on POE0#, POE4#, POE8#, POE10#, or POE11# • Shorting of output pins When a match (short circuit) occurs between the output signal levels (active level) over one or more cycles on the following combination of pins: MTIOC3B and MTIOC3D MTIOC4A and MTIOC4C MTIOC4B and MTIOC4D MTIOC6B and MTIOC6D MTIOC7A and MTIOC7C MTIOC7B and MTIOC7D • When a register setting is made • When main clock generation circuit oscillation stop is detected

Item	RX64M (POE3)	RX65N (POE3a)
Functions	• Each of the POE0#, POE4#, POE8#, POE10#, and POE11# input pins can be set for falling edge, PCLK/8 × 16, PCLK/16 × 16, or PCLK/128 × 16 low-level sampling. • Pins for the MTU complementary PWM output, MTU0, GPT output, and GPT3 pins can be placed in the high-impedance state by the POE0#, POE4#, POE8#, POE10#, and POE11# falling-edge or low-level sampling. • The MTU's complementary PWM output pins and the MTU0 pins, GPT output pins, and GPT3 pins can be placed in the high-impedance state when clock generation circuit oscillation-stop is detected. • The MTU's complementary PWM output pins or the GPT pins can be placed in the high-impedance state when the output levels of the MTU's complementary PWM output pins or GPT output pins (GPT0, GPT1, or GPT2) are compared and simultaneous active-level output continues for one cycle or more. • Pins for the MTU complementary PWM output and MTU0, GPT output, and GPT3 pins can be placed in the high-impedance state by modifying the settings in the POE registers. • Interrupts can be generated by input level sampling or output level comparison results.	• Each of the POE0#, POE4#, POE8#, POE10#, and POE11# input pins can be set for falling edge, PCLK/8 × 16, PCLK/16 × 16, or PCLK/128 × 16 low-level sampling. • Pins for the MTU complementary PWM output and MTU0 pins can be placed in the high-impedance state by the POE0#, POE4#, POE8#, POE10#, and POE11# falling-edge or low-level sampling. • Pins for complementary PWM output from the MTU and MTU0 pins can be placed in the high-impedance state when oscillation by the clock generation circuit stops. • Pins for the MTU complementary PWM output can be placed in the high-impedance state when output levels of the MTU complementary PWM output pins are compared and simultaneous active-level output continues for one cycle or more. • Pins for the MTU complementary PWM output and MTU0 pins can be placed in the high-impedance state by modifying the settings in the POE registers. • Interrupts can be generated by input level sampling or output level comparison results.

Table 2.27 Comparative Listing of Port Output Enable Registers

Register	Bit	RX64M (POE3)	RX65N (POE3a)
ALR1	OLSG0A	MTIOC3B/GTIOC0A active level setting bit	MTIOC3B active level setting bit
	OLSG0B	MTIOC3D/GTIOC0B active level setting bit	MTIOC3D active level setting bit
	OLSG1A	MTIOC4A/GTIOC1A active level setting bit	MTIOC4A active level setting bit
	OLSG1B	MTIOC4C/GTIOC1B active level setting bit	MTIOC4C active level setting bit
	OLSG2A	MTIOC4B/GTIOC2A active level setting bit	MTIOC4B active level setting bit
	OLSG2B	MTIOC4D/GTIOC2B active level setting bit	MTIOC4D active level setting bit
SPOER	MTUCH34HIZ	MTU3 and MTU4 or GPT0 to GPT2 output high-impedance enable bit	MTU3 and MTU4 output high-impedance enable bit
	GPT01HIZ	GPT0 and GPT1 output high-impedance enable bit	—
	GPT23HIZ	GPT2 and GPT3 output high-impedance enable bit	—
POECR3	—	Port output enable control register 3	—
POECR6	—	Port output enable control register 6	—
G0SELR	—	GPT0 pin select register	—
G1SELR	—	GPT1 pin select register	—
G2SELR	—	GPT2 pin select register	—
G3SELR	—	GPT3 pin select register	—
MGSELR	—	MTU/GPT pin function select register	—

2.13 Ethernet Controller

Table 2.28 shows a comparative overview of Ethernet controller specifications.

Table 2.28 Comparative Overview of Ethernet Controller

Item	RX64M (ETHERC)	RX65N (ETHERC)
Channels	2 channels	1 channel
Protocol	Flow control compliant with IEEE 802.3x	Flow control compliant with IEEE 802.3x
Data transmission and reception	Frames compliant with the Ethernet/IEEE 802.3 standard can be transmitted and received.	Frames compliant with the Ethernet/IEEE 802.3 standard can be transmitted and received.
Bit rate	Supports 10 Mbps and 100 Mbps.	Supports 10 Mbps and 100 Mbps.
Communication modes	Supports full-duplex and half-duplex modes.	Supports full-duplex and half-duplex modes.
Interfaces	Media Independent Interface (MII) and Reduced Media Independent Interface (RMII), compliant with the IEEE 802.3u standard	Media Independent Interface (MII) and Reduced Media Independent Interface (RMII), compliant with the IEEE 802.3u standard
Functions	Magic Packet™*1 detection and Wake-On-LAN (WOL) signal output	Magic Packet™*1 detection and Wake-On-LAN (WOL) signal output

Note 1. Magic Packet is a trademark of Advanced Micro Devices, Inc.

2.14 DMA Controller for the Ethernet Controller

Table 2.29 shows a comparative listing of the DMA controller for the ethernet controller registers.

Table 2.29 Comparative Listing of DMA Controller for the Ethernet Controller Registers

Register	Bit	RX64M (EDMACa)	RX65N (EDMACa)
EESIPR	ADEIP	Address error interrupt request enable bit	—
PTPEDMAC.EESR	—	PTP/EDMAC status register	—
PTPEDMAC.EESIPR	—	PTP/EDMAC status interrupt enable register	—
FDR	RDF[4:0]	Receive FIFO depth b4 b0 0 1 1 1 1: 4,096 bytes Do not set to values other than the above.	Receive FIFO depth b4 b0 0 0 1 1 1: 1,968 bytes Do not set to values other than the above.
FCFTR	RFDO[2:0]	Receive FIFO data PAUSE output threshold bits b2 b0 0 0 0: When 224 (256 – 32) bytes of data is stored in the receive FIFO 0 0 1: When 480 (512 – 32) bytes of data is stored in the receive FIFO : 1 1 0: When 1,760 (1,792 – 32) bytes of data is stored in the receive FIFO 1 1 1: When 2,016 (2,048 – 32) bytes of data is stored in the receive FIFO	Receive FIFO data PAUSE output threshold bits b2 b0 0 0 0: When 224 (256 – 32) bytes of data is stored in the receive FIFO 0 0 1: When 480 (512 – 32) bytes of data is stored in the receive FIFO : 1 1 0: When 1,760 (1,792 – 32) bytes of data is stored in the receive FIFO 1 1 1: When 1,952 (2,048 – 96) bytes of data is stored in the receive FIFO

2.15 USB 2.0 FS Host/Function Module

Table 2.30 shows a comparative listing of the USB 2.0 FS host/function module registers.

Table 2.30 Comparative Listing of USB 2.0 FS Host/Function Module Registers

Register	Bit	RX64M (USBb)	RX65N (USBb)
PHYSLEW	SLEWR00	Driver cross point adjustment 00 bit 0: Host controller is selected. 1: Function controller is selected.	Driver cross point adjustment 00 bit Set this bit to 1.
	SLEWR01	Driver cross point adjustment 01 bit 0: Function controller is selected. 1: Host controller is selected.	Driver cross point adjustment 01 bit Set this bit to 0.
	SLEWF00	Driver cross point adjustment 00 bit Set this bit to 1.	Driver cross point adjustment 00 bit Set this bit to 1.
	SLEWF01	Driver cross point adjustment 01 bit 0: Function controller is selected. 1: Host controller is selected.	Driver cross point adjustment 01 bit Set this bit to 0.

2.16 Serial Communication Interface

The RX64M Group has 9 independent serial communications interface (SCI) channels (SCIg: 8 channels, SCIh: 1 channel) and 4 independent serial communications interface with FIFO (SCIFA).

The RX65N Group and RX651 Group have 13 independent serial communications interface (SCI) channels (SCIg: 10 channels, SCIi: 2 channels, SCIh: 1 channel).

Table 2.31 shows a comparative overview of the SCIg specifications, Table 2.32 shows a comparative overview of the SCIi specifications, Table 2.33 shows a comparative overview of the SCIh specifications, Table 2.34 shows a comparative overview of the SCI channel specifications, and Table 2.35 shows a comparative listing of the serial communications interface registers.

Table 2.31 Comparative Overview of SCIg Specifications

Item		RX64M (SCIg)	RX65N (SCIg)
Number of channels		8 channels	10 channels
Serial communication modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication		• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		Selectable between LSB-first or MSB-first transfer.*1	Selectable between LSB-first or MSB-first transfer.*1
Interrupt sources		Transmit end, transmit data empty, receive data full, receive error, completion of generation of start condition, restart condition, or stop condition (simple I²C mode)	Transmit end, transmit data empty, receive data full, receive error, completion of generation of start condition, restart condition, or stop condition (simple I²C mode)
Low power consumption function		The module stop state can be specified for each channel.	The module stop state can be specified for each channel.
Asynchronous mode	Data length	7, 8, or 9 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	The CTSn# and RTSn# pins can be used to control transmission and reception.	The CTSn# and RTSn# pins can be used to control transmission and reception.
	Start bit detection	Selectable between low level and falling edge.	Selectable between low level and falling edge.
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.

Item		RX64M (SCIg)	RX65N (SCIg)
Asynchronous mode	Clock source	An internal or external clock can be selected. Transfer rate clock input from the TMR can be used (SCI5 and SCI6).	An internal or external clock can be selected. Transfer rate clock input from the TMR can be used (SCI5 and SCI6).
	Double-speed mode	Baud rate generator double-speed mode is selectable.	Baud rate generator double-speed mode is selectable.
	Multi-processor communication function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate on-chip digital noise filters.	The signal paths from input on the RXDn pins incorporate on-chip digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	The CTSn and RTSn pins can be used to control transmission and reception.	The CTSn# and RTSn# pins can be used to control transmission and reception.
Smart card interface mode	Error processing	An error signal can be transmitted automatically when a parity error is detected during reception.	An error signal can be transmitted automatically when a parity error is detected during reception.
		Data can be retransmitted automatically when an error signal is received during transmission.	Data can be retransmitted automatically when an error signal is received during transmission.
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^2C mode	Communication format	I^2C bus format	I^2C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer rate	Fast mode is supported.	Fast mode is supported.
	Noise canceler	The signal paths from input on the SSCLn and SSDAn pins incorporate on-chip digital noise filters, and the noise cancellation bandwidth is adjustable.	The signal paths from input on the SSCLn and SSDAn pins incorporate on-chip digital noise filters, and the noise cancellation bandwidth is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Error detection	Overrun error	Overrun error
	SS input pin function	Applying a high-level signal to the SSn# pin causes the output pins to enter the high-impedance state.	Applying a high-level signal to the SSn# pin causes the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.
Bit rate modulation function		On-chip baud rate generator output correction can reduce errors.	On-chip baud rate generator output correction can reduce errors.
Event link function (SCI5 only)		Error (receive error, error signal detection) event output	Error (receive error, error signal detection) event output
		Receive data full event output	Receive data full event output
		Transmit data empty event output	Transmit data empty event output
		Transmit end event output	Transmit end event output

Note 1. Only MSB-first is available in simple I^2C mode.

Table 2.32 Comparative Overview of SCIi Specifications

Item		RX64M (SCIFA)	RX65N (SCIi)
Number of channels		4 channels	2 channels
Serial communication modes		Asynchronous and clock synchronous	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		—	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication		• Transmitter: Continuous data transmission possible using 16-stage FIFO buffering • Receiver: Continuous data reception possible using 16-stage FIFO buffering	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		LSB first or MSB first	Selectable between LSB-first or MSB-first transfer.∗1
Interrupt sources		TEIF : Transmit end TXIF : Transmit FIFO data empty RXIF : Receive FIFO data full DRIF : Receive data ready (only valid in asynchronous communication mode) ERIF : Receive error BRIF : Break detect or overrun error	Transmit end, transmit data empty, receive data full, receive error, receive data ready, and data match, completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)
Low power consumption function		—	The module stop state can be specified for each channel.
Asynchronous mode	Data length	7 or 8 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or none	Even parity, odd parity, or no parity
	Receive error detection	A parity error, overrun error, or framing error can be detected as a receive error.	Parity, overrun, and framing errors
	Hardware flow control	Controls data transmission and reception using the CTS# and RTS# pins.	The CTSn# and RTSn# pins can be used to control transmission and reception.
	Transmit/receive FIFO	Transmitter: Continuous data transmission possible using 16-stage FIFO buffering Receiver: Continuous data reception possible using 16-stage FIFO buffering	Usable as a FIFO with 16 transmit stages and 16 receive stages.
	Data match detection	—	Compares receive data and comparison data, and generates interrupt when they are matched
	Start bit detection	—	Selectable between low level and falling edge.

Item		RX64M (SCIFA)	RX65N (SCIi)
	Break detection	Break signal detection by hardware	When a framing error occurs, a break can be detected by reading the internal register
	Clock source	Internal clock or external clock selectable	An internal or external clock can be selected.
	Double-speed mode	—	Baud rate generator double-speed mode is selectable.
	Multi-processor communication function	—	Serial communication among multiple processors
	Noise cancellation	Incorporates a digital noise filter in the RXD pin input path.	The signal paths from input on the RXDn pins incorporate on-chip digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	An overrun error can be detected as a receive error.	Overrun error
	Hardware flow control	—	The CTSn# and RTSn# pins can be used to control transmission and reception.
	Transmit/receive FIFO	Transmitter: Continuous data transmission possible using 16-stage FIFO buffering Receiver: Continuous data reception possible using 16-stage FIFO buffering	Usable as a FIFO with 16 transmit stages and 16 receive stages.
Smart card interface mode	Error processing	—	An error signal can be transmitted automatically when a parity error is detected during reception.
		—	Data can be retransmitted automatically when an error signal is received during transmission.
	Data type	—	Both direct convention and inverse convention are supported.
Simple I^2C mode	Communication format	—	I^2C bus format
	Operating mode	—	Master (single-master operation only)
	Transfer rate	—	Fast mode is supported.
	Noise canceler	—	The signal paths from input on the SSCLn and SSDAn pins incorporate on-chip digital noise filters, and the noise cancellation bandwidth is adjustable.
Simple SPI mode	Data length	—	8 bits
	Error detection	—	Overrun error
	SS input pin function	—	Applying a high-level signal to the SSn# pin causes the output pins to enter the high-impedance state.
	Clock settings	—	Four kinds of settings for clock phase and clock polarity are selectable.

Item	RX64M (SCIFA)	RX65N (SCIi)
Bit rate modulation function	Errors can be reduced using the on-chip baud rate generator's output correction	On-chip baud rate generator output correction can reduce errors.

Table 2.33 Comparative Overview of SCIh Specifications

Item		RX64M (SCIh)	RX65N (SCIh)
Number of channels		1 channels	1 channels
Serial communication modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I2C-bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I2C-bus • Simple SPI bus
Transfer speed		Bit rate specifiable with the on-chip baud rate generator.	Bit rate specifiable with the on-chip baud rate generator.
Full-duplex communications		Transmitter: Continuous transmission possible using double-buffer structure. Receiver: Continuous reception possible using double-buffer structure.	Transmitter: Continuous transmission possible using double-buffer structure. Receiver: Continuous reception possible using double-buffer structure.
Data transfer		Selectable as LSB first or MSB first transfer *1	Selectable as LSB first or MSB first transfer *1
Interrupt sources		Transmit end, transmit data empty, receive data full, and receive error Completion of generation of a start condition, restart condition, or stop condition (for simple I2C mode)	Transmit end, transmit data empty, receive data full, and receive error Completion of generation of a start condition, restart condition, or stop condition (for simple I2C mode)
Low power consumption function		Module stop state can be set.	Module stop state can be set.
Asynchronous mode	Data length	7, 8, or 9 bits	7, 8, or 9 bits
	Transmission stop bit	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Start-bit detection	Low level or falling edge is selectable.	Low level or falling edge is selectable.
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.
	Clock source	An internal or external clock can be selected. Transfer rate clock input from the TMR can be used. (SCI12)	An internal or external clock can be selected. Transfer rate clock input from the TMR can be used. (SCI12)

Item		RX64M (SCIh)	RX65N (SCIh)
Asynchronous mode	Double-speed mode	Baud rate generator double-speed mode is selectable.	Baud rate generator double-speed mode is selectable.
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
Smart card interface mode	Error processing	An error signal can be automatically transmitted when detecting a parity error during reception	An error signal can be automatically transmitted when detecting a parity error during reception
		Data can be automatically retransmitted when receiving an error signal during transmission	Data can be automatically retransmitted when receiving an error signal during transmission
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^2C mode	Transfer format	I^2C-bus format	I^2C-bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer rate	Fast mode is supported	Fast mode is supported
	Noise cancellation	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.
Simple SPI bus	Data length	8 bits	8 bits
	Detection of errors	Overrun error	Overrun error
	SS input pin function	Applying the high level to the SSn# pin can cause the output pins to enter the highimpedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the highimpedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.
Extended serial mode	Start Frame transmission	• Output of a low level as the Break Field over a specified width and generation of interrupts on completion • Detection of bus collisions and the generation of interrupts on detection	• Output of a low level as the Break Field over a specified width and generation of interrupts on completion • Detection of bus collisions and the generation of interrupts on detection

Item		RX64M (SCIh)	RX65N (SCIh)
Extended serial mode	Start Frame reception	• Detection of the Break Field low width and generation of an interrupt on detection • Comparison of Control Fields 0 and 1 and generation of an interrupt when the two match • Two kinds of data for comparison (primary and secondary) can be set in Control Field 1. • A priority interrupt bit can be set in Control Field 1. • Handling of Start Frames that do not include a Break Field • Handling of Start Frames that do not include a Control Field • Function for measuring bit rates	• Detection of the Break Field low width and generation of an interrupt on detection • Comparison of Control Fields 0 and 1 and generation of an interrupt when the two match • Two kinds of data for comparison (primary and secondary) can be set in Control Field 1. • A priority interrupt bit can be set in Control Field 1. • Handling of Start Frames that do not include a Break Field • Handling of Start Frames that do not include a Control Field • Function for measuring bit rates
	I/O control function	• Selectable polarity for TXDX12 and RXDX12 signals • Selection of a digital filter for the RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Selectable timing for the sampling of data received through RXDX12 • Signals received on RXDX12 can be passed though to SCIg when the extended serial mode control section is off.	• Selectable polarity for TXDX12 and RXDX12 signals • Selection of a digital filter for the RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Selectable timing for the sampling of data received through RXDX12 • Signals received on RXDX12 can be passed though to SCIg when the extended serial mode control section is off.
	Timer function	Usable as a reloading timer	Usable as a reloading timer
Bit rate modulation function		Correction of outputs from the on-chip baud rate generator can reduce errors.	Correction of outputs from the on-chip baud rate generator can reduce errors.

Note 1. In simple I^2C mode, only MSB first is available.

Table 2.34 Comparative Overview of SCI Channel Specifications

Item	RX64M (SCIg, SCIh)	RX65N (SCIg, SCIi, SCIh)
Synchronous mode	SCI0 to SCI7, SCI12	SCI0 to SCI7, SCI8 to SCI11, SCI12
Clock synchronous mode	SCI0 to SCI7, SCI12	SCI0 to SCI7, SCI8 to SCI11, SCI12
Smart card interface mode	SCI0 to SCI7, SCI12	SCI0 to SCI7, SCI8 to SCI11, SCI12
Simple I^2C mode	SCI0 to SCI7, SCI12	SCI0 to SCI7, SCI8 to SCI11, SCI12
Simple SPI mode	SCI0 to SCI7, SCI12	SCI0 to SCI7, SCI8 to SCI11, SCI12
Extended serial mode	SCI12	SCI12
TMR clock input	SCI5, SCI6, SCI12	SCI5, SCI6, SCI12
Event link function	SCI5	SCI5
FIFO mode	SCIFA8, SCIFA9, SCIFA10, SCIFA11	SCI10, SCI11

Table 2.35 Comparative Listing of Serial Communication Interface Registers

Register	Bit	RX64M (SCIg, SCIh)	RX65N (SCIg, SCIi, SCIh)
FRDR	—	—	Receive FIFO data register
FTDR	—	—	Transmit FIFO data register
SSRFIFO	—	—	Serial status register*1
FCR	—	—	FIFO control register
FDR	—	—	FIFO data count register
LSR	—	—	Line status register
CDR	—	—	Comparison data register
DCCR	—	—	Data comparison control register
SPTR	—	—	Serial port register

Note 1. Non-smart card interface mode and FIFO mode (SCMR.SMIF = 0 and FCR.FM = 1)

2.17 CAN Module

Table 2.36 shows a comparative overview of the CAN module specifications.

Table 2.36 Comparative Overview of CAN Module Interface

Item	RX64M (CAN)	RX65N (CAN)
Number of channels	3 channels	2 channels
Protocol	ISO 11898-1 compliant (standard and extended frames)	ISO 11898-1 compliant (standard and extended frames)
Bit rate	Programmable bit rate below 1 Mbps (fCAN ≥ 8 MHz) fCAN: CAN clock source	Programmable bit rate below 1 Mbps (fCAN ≥ 8 MHz) fCAN: CAN clock source
Message box	32 mailboxes: Two selectable mailbox modes • Normal mailbox mode: 32 mailboxes can be configured for either transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for either transmission or reception. Of the other mailboxes, four FIFO stages can be configured for transmission and four FIFO stages for reception.	32 mailboxes: Two selectable mailbox modes • Normal mailbox mode: 32 mailboxes can be configured for either transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for either transmission or reception. Of the other mailboxes, four FIFO stages can be configured for transmission and four FIFO stages for reception.
Reception	• Data frames and remote frames can be received. • Selectable receiving ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot reception function • Selectable between overwrite mode (messages overwritten) and overrun mode (messages discarded) • Reception-complete interrupt can be individually enabled or disabled for each mailbox.	• Data frames and remote frames can be received. • Selectable receiving ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot reception function • Selectable between overwrite mode (messages overwritten) and overrun mode (messages discarded) • Reception-complete interrupt can be individually enabled or disabled for each mailbox.
Acceptance filter	• Eight acceptance masks (one mask for every four mailboxes) • The mask can be individually enabled or disabled for each mailbox.	• Eight acceptance masks (one mask for every four mailboxes) • The mask can be individually enabled or disabled for each mailbox.
Transmission	• Data frames and remote frames can be transmitted. • Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot transmission function • Selectable between ID priority mode and mailbox number priority mode • Transmission requests can be aborted. (Completion of abort can be confirmed with a flag.)	• Data frames and remote frames can be transmitted. • Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot transmission function • Selectable between ID priority mode and mailbox number priority mode • Transmission requests can be aborted. (Completion of abort can be confirmed with a flag.)

Item	RX64M (CAN)	RX65N (CAN)
Transmission	• Transmission-complete interrupt can be individually enabled or disabled for each mailbox.	• Transmission-complete interrupt can be individually enabled or disabled for each mailbox.
Mode transition for bus-off recovery	The mode transition for recovery from the bus-off state can be selected. • ISO 11898-1 compliant • Automatic transition to CAN halt mode at bus-off start • Automatic transition to CAN halt mode at bus-off end • Transition to CAN halt mode by a program • Transition to error-active state by a program	The mode transition for recovery from the bus-off state can be selected. • ISO 11898-1 compliant • Automatic transition to CAN halt mode at bus-off start • Automatic transition to CAN halt mode at bus-off end • Transition to CAN halt mode by a program • Transition to error-active state by a program
Error status monitoring	• CAN bus errors (stack error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored. • Transition to error states can be detected (error-warning, error-passive, bus-off start, and bus-off recovery). • The error counters can be read.	• CAN bus errors (stack error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored. • Transition to error states can be detected (error-warning, error-passive, bus-off start, and bus-off recovery). • The error counters can be read.
Time stamp function	• Time stamp function using a 16-bit counter • The reference clock can be selected from 1-, 2-, 4- and 8-bit time periods.	• Time stamp function using a 16-bit counter • The reference clock can be selected from 1-, 2-, 4- and 8-bit time periods.
Interrupt function	Five interrupt sources (reception complete, transmission complete, receive FIFO, transmit FIFO, and error interrupt)	Five interrupt sources (reception complete, transmission complete, receive FIFO, transmit FIFO, and error interrupt)
CAN sleep mode	Current consumption can be reduced by stopping the CAN clock.	Current consumption can be reduced by stopping the CAN clock.
Software support units	Three software support units: • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support	Three software support units: • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support
CAN clock source	Peripheral module clock (PCLKB), CANMCLK	Peripheral module clock (PCLKB), CANMCLK
Test mode	Three test modes for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback)	Three test modes for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback)
Low power consumption function	Module stop state can be set.	Module stop state can be set.

2.18 Serial Peripheral Interface

Table 2.37 shows a comparative overview of the serial peripheral interface specifications, and Table 2.38 shows a comparative listing of the serial peripheral interface registers.

Table 2.37 Comparative Overview of Serial Peripheral Interface

Item	RX64M (RSPIa)	RX65N (RSPIc)
Number of channels	1 channel	3 channels
RSPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communication through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK is supported. • Switching of the phase of RSPCK is supported.	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communication through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK is supported. • Switching of the phase of RSPCK is supported.
Data format	• Selectable between MSB-first and LSB-first. • Transfer bit length is selectable among 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (with each frame consisting of up to 32 bits).	• Selectable between MSB-first and LSB-first. • Transfer bit length is selectable among 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (with each frame consisting of up to 32 bits). • Ability to swap transmit data and receive data in byte units
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from 2 to 4,096). • In slave mode, the minimum PCLK clock divided by 8 can be input as RSPCK (the maximum frequency of RSPCK is PCLK divided by 8). Width at high level: 4 cycles of PCLK; width at low level: 4 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from 2 to 4,096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is PCLK divided by 4). Width at high level: 2 cycles of PCLK; width at low level: 2 cycles of PCLK
Buffer configuration	• The transmit and receive buffers have a double buffer configuration. • The transmit and receive buffers are each 128 bits in size.	• The transmit and receive buffers have a double buffer configuration. • The transmit and receive buffers are each 128 bits in size.
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection

Item	RX64M (RSPIa)	RX65N (RSPIc)
SSL control function	• Four SSL signals (SSLn0 to SSLn3) for each channel • In single-master mode, SSLn0 to SSLn3 signals are output. • In multi-master mode: SSLn0 signal is input, and SSLn1 to SSLn3 signals are either output or unused. • In slave mode: SSLn0 signal is input, and SSLn1 to SSLn3 signals are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • SSL polarity-change function	• Four SSL pins (SSLn0 to SSLn3) for each channel • In single-master mode, SSLn0 to SSLn3 pins are output. • In multi-master mode: SSLn0 pin is input, and SSLn1 to SSLn3 pins are either output or unused. • In slave mode: SSLn0 pin is input, and SSLn1 to SSLn3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • SSL polarity-change function
Control in master transfer	• Transfers of up to eight commands can be performed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, LSB/MSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • The MOSI signal value when SSL is negated can be specified. • RSPCK auto-stop function	• Transfers of up to eight commands can be performed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, LSB/MSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • The MOSI signal value when SSL is negated can be specified. • RSPCK auto-stop function
Interrupt sources	• Receive buffer full interrupt • Transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, parity error) • RSPI idle interrupt (RSPI idle)	• Receive buffer full interrupt • Transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, underrun, parity error) • RSPI idle interrupt (RSPI idle)
Event link function (output)	The following events can be output to the event link controller: • Receive buffer run event signal • Transmit buffer empty event signal • Mode fault, overrun, or parity error event signal • RSPI idle event signal • Transmit end event signal	The following events can be output to the event link controller: • Receive buffer run event signal • Transmit buffer empty event signal • Mode fault, overrun, underrun, or parity error event signal • RSPI idle event signal • Transmit end event signal

Item	RX64M (RSPIa)	RX65N (RSPIc)
Other functions	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode function	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode function
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Table 2.38 Comparative Listing of Serial Peripheral Interface Registers

Register	Bit	RX64M (RSPIa)	RX65N (RSPIc)
SPSR	MODF	Mode fault error flag 0: No mode fault error occurred 1: A mode fault error occurred	Mode fault error flag 0: No mode fault error occurred, no underrun error occurred. 1: A mode fault error occurred, an underrun error occurred.
	UDRF	—	Underrun error flag
SPDR	—	RSPI data register Possible access sizes: • Longword access (SPDCR.SPLW = 1) • Word access (SPDCR.SPLW = 0)	RSPI data register Possible access sizes: • Longword access (SPDCR.SPLW = 1, SPBYTE = 0) • Word access (SPDCR.SPLW = 0, SPBYTE = 0) • Byte access (SPDCR.SPBYT = 1)
SPDCR	SPBYT	—	RSPI byte access specification bit
SPDCR2	—	—	RSPI data control register 2

2.19 CRC Calculator

Table 2.39 shows a comparative overview of the CRC calculator specifications, and Table 2.40 shows a comparative listing of the CRC calculator registers.

Table 2.39 Comparative Overview of CRC Calculator

Item	RX64M (CRC)	RX65N (CRCA)
Data size	8 or 16 bits	8 or 32 bits
Data for CRC calculation	• 8- or 16-bit data size: CRC code generated for 8n bits of data (n = natural number)	• 8-bit data size: CRC code generated for 8n bits of data (n = natural number) • 32-bit data size: CRC code generated for 32n bits of data (n = natural number)
CRC processor unit	• Operation executed on eight bits in parallel	• Operation executed on eight bits in parallel • Operation executed on 32 bits in parallel
CRC generating polynomial	One of three generating polynomials selectable: • 8-bit CRC $X^8 + X^2 + X + 1$ • 16-bit CRC $X^{16} + X^{15} + X^2 + 1$ $X^{16} + X^{12} + X^5 + 1$	One of five generating polynomials selectable: • 8-bit CRC $X^8 + X^2 + X + 1$ • 16-bit CRC $X^{16} + X^{15} + X^2 + 1$ $X^{16} + X^{12} + X^5 + 1$ • 32-bit CRC $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$
CRC calculation switching	The order of the bits produced by CRC calculation can be switched for LSB first or MSB first communication	The order of the bits produced by CRC calculation can be switched for LSB first or MSB first communication
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Table 2.40 Comparative Listing of CRC Calculator Registers

Register	Bit	RX64M (CRC)	RX65N (CRCA)
CRCCR	GPS	CRC generating polynomial switching bits (b1 and b0)	CRC generating polynomial switching bits (b2 to b0)
	LMS	CRC calculation switching bit (b2)	CRC calculation switching bit (b6)
CRCDIR	—	• When generating 16-bit or 8-bit CRCs CRC data input register (b7 to b0)	• When generating 32-bit CRCs CRC data input register (b31 to b0) • When generating 16-bit or 8-bit CRCs CRC data input register (b7 to b0)
CRCDOR	—	• When generating 16-bit CRCs CRC data output register (b15 to b0) The bottom byte (b7 to b0) is used when generating 8-bit CRCs.	• When generating 32-bit CRCs CRC data output register (b31 to b0) • When generating 16-bit CRCs CRC data output register (b15 to b0) • When generating 8-bit CRCs CRC data output register (b7 to b0)

2.20 SD Host Interface (SDHI)

Table 2.41 shows a comparative overview of the SD Host interface specifications, and Table 2.42 shows a comparative listing of the SD Host interface registers.

Table 2.41 Comparative Overview of SD Host Interface

Item	RX64M (SDHI)	RX65N (SDHI)
Interface	• Compatible with SD memory cards and SDIO cards. • Transfer bus width selectable between wide bus mode (4-bit) and default bus mode (1-bit). • Able to access SD, SDHC, and SDXC memory cards.	• Compatible with SD memory cards and SDIO cards. • Transfer bus width selectable between wide bus mode (4-bit) and default bus mode (1-bit). • Able to access SD, SDHC, and SDXC memory cards.
Transfer modes	Support for high-speed mode and default speed mode	Support for high-speed mode and default speed mode
SDHI clock	SDHI clock generated by dividing peripheral module clock B (PCLKB) by n, where n = 2, 4, 8, 16, 32, 64, 128, 256, or 512.	SDHI clock generated by dividing peripheral module clock B (PCLKB) by n, where n = 1, 2, 4, 8, 16, 32, 64, 128, 256, or 512.
Error check functions	• CRC7 (command, response) • CRC16 (transfer data)	• CRC7 (command, response) • CRC16 (transfer data)
Interrupt sources	4 sources • Card access interrupt (CACI) • SDIO access interrupt (SDACI) • Card detection interrupt (CDETI) • SD buffer access interrupt (SBFAI)	4 sources • Card access interrupt (CACI) • SDIO access interrupt (SDACI) • Card detection interrupt (CDETI) • SD buffer access interrupt (SBFAI)
DMA transfer request	• DMAC and DTC can be activated by the SD buffer access (SBFAI) interrupt. • The SD buffer is read and write accessible by the DMAC and DTC.	• DMAC and DTC can be activated by the SD buffer access (SBFAI) interrupt. • The SD buffer is read and write accessible by the DMAC and DTC.
Other functions	• Card detection function • Write protection function	• Card detection function • Write protection function

Table 2.42 Comparative Listing of SD Host Interface Registers

Register	Bit	RX64M (SDHI)	RX65N (SDHI)
SDCLKCR	CLKSEL[7:0]	SDHI clock frequency select bits b7 b0 0 0 0 0 0 0 0 0: 1/2 PCLKB frequency 0 0 0 0 0 0 0 1: 1/4 PCLKB frequency 0 0 0 0 0 0 1 0: 1/8 PCLKB frequency 0 0 0 0 0 1 0 0: 1/16 PCLKB frequency 0 0 0 0 1 0 0 0: 1/32 PCLKB frequency 0 0 0 1 0 0 0 0: 1/64 PCLKB frequency 0 0 1 0 0 0 0 0: 1/128 PCLKB frequency 0 1 0 0 0 0 0 0: 1/256 PCLKB frequency 1 0 0 0 0 0 0 0: 1/512 PCLKB frequency Do not set to values other than the above.	SDHI clock frequency select bits b7 b0 0 0 0 0 0 0 0 0: 1/2 PCLKB frequency 0 0 0 0 0 0 0 1: 1/4 PCLKB frequency 0 0 0 0 0 0 1 0: 1/8 PCLKB frequency 0 0 0 0 0 1 0 0: 1/16 PCLKB frequency 0 0 0 0 1 0 0 0: 1/32 PCLKB frequency 0 0 0 1 0 0 0 0: 1/64 PCLKB frequency 0 0 1 0 0 0 0 0: 1/128 PCLKB frequency 0 1 0 0 0 0 0 0: 1/256 PCLKB frequency 1 0 0 0 0 0 0 0: 1/512 PCLKB frequency 1 1 1 1 1 1 1 1: PCLKB Do not set to values other than the above.
SDVER	CLKRAT	Operating clock condition bit (value 0 after a reset)	Operating clock condition bit (value 1 after a reset)

2.21 AES

Regarding the public release of this section, an exchange of non-disclosure agreement is necessary.

For details, contact your Renesas sales agency.

2.22 RNG

Regarding the public release of this section, an exchange of non-disclosure agreement is necessary.

For details, contact your Renesas sales agency.

2.23 12-Bit A/D Converter

Table 2.43 shows a comparative overview of the 12-bit A/D converter specifications, and Table 2.44 shows a comparative listing of the 12-bit A/D converter registers.

Table 2.43 Comparative Overview of 12-Bit A/D Converter

Item	RX64M (S12ADC)	RX65N (S12ADFa)
Number of units	1 unit	2 units
Input channels	Unit 0: 8 channels Unit 1: 21 channels + one extended channel	Unit 0: 8 channels Unit 1: 21 channels + one extended channel
Extended analog function	Temperature sensor output, internal reference voltage	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	• (0.48 µs) per channel (12-bit conversion mode) • (0.45 µs) per channel (10-bit conversion mode) • (0.42 µs) per channel (8-bit conversion mode) (Operating with A/D conversion clock ADCLK = 60 MHz)	• (0.48 µs) per channel (12-bit conversion mode) • (0.45 µs) per channel (10-bit conversion mode) • (0.42 µs) per channel (8-bit conversion mode) (Operating with A/D conversion clock ADCLK = 60 MHz)
A/D conversion clock (ADCLK)	Peripheral module clock PCLKB and A/D conversion clock ADCLK can be set so that the frequency ratio is one of the following: PCLKB: ADCLK division ratio = 1:1, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit (CPG).	Peripheral module clock PCLKB and A/D conversion clock ADCLK can be set so that the frequency ratio is one of the following: PCLKB: ADCLK division ratio = 1:1, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit (CPG).
Data register	• For analog input: 29 data registers (unit 0: 8 data registers, unit 1: 21 data registers), one data register for each unit for A/D conversion data multiplexing in double trigger mode, two data registers for each unit for A/D conversion data multiplexing in double trigger mode extended operation • For temperature sensor: One data register (unit 1 only) • For internal reference voltage: One data register (unit 1 only) • 1 register per unit for self-diagnostics • The results of A/D conversion are stored in 12-bit A/D data registers. • 8-, 10-, and 12-bit accuracy output for the results of A/D conversion	• For analog input: 29 data registers (unit 0: 8 data registers, unit 1: 21 data registers), one data register for each unit for A/D conversion data multiplexing in double trigger mode, two data registers for each unit for A/D conversion data multiplexing in double trigger mode extended operation • For temperature sensor: One data register (unit 1 only) • For internal reference voltage: One data register (unit 1 only) • 1 register per unit for self-diagnostics • The results of A/D conversion are stored in 12-bit A/D data registers. • 8-, 10-, and 12-bit accuracy output for the results of A/D conversion

Item	RX64M (S12ADC)	RX65N (S12ADFa)
Data register	• The value obtained by adding up A/D-converted results is stored as a value (number of conversion accuracy bits + 2 bits) in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.	• The value obtained by adding up A/D-converted results is stored as a value (number of conversion accuracy bits + 2 bits/4 bits) in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.
Operating modes	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 8 (unit 0) or up to 12 (unit 1) user-selected channels. — A/D conversion is performed only once on the temperature sensor output (unit 1 only). — A/D conversion is performed only once on the internal reference voltage (unit 1 only). — A/D conversion is performed only once on the extended analog input (unit 1 only). • Continuous scan mode: — A/D conversion is performed repeatedly on the analog inputs of up to 8 (unit 0) or up to 21 (unit 1) user-selected channels, the temperature sensor output (unit 1 only), or the internal reference voltage (unit 1 only). — A/D conversion is performed repeatedly on the extended analog input (unit 1 only).	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 8 (unit 0) or up to 12 (unit 1) user-selected channels. — A/D conversion is performed only once on the temperature sensor output (unit 1 only). — A/D conversion is performed only once on the internal reference voltage (unit 1 only). — A/D conversion is performed only once on the extended analog input (unit 1 only). • Continuous scan mode: — A/D conversion is performed repeatedly on the analog inputs of up to 8 (unit 0) or up to 21 (unit 1) user-selected channels, the temperature sensor output (unit 1 only), or the internal reference voltage (unit 1 only). — A/D conversion is performed repeatedly on the extended analog input (unit 1 only).

Item	RX64M (S12ADC)	RX65N (S12ADFa)
Operating modes	• Group scan mode: — Either two (A and B) groups may be selected. — The analog inputs of user-selected channels, the temperature sensor output (unit 1 only), or the internal reference voltage (unit 1 only) are divided up among group A and group B, and A/D conversion is performed only once on the analog inputs selected as a group unit. — The scanning start conditions (synchronous triggers) can be selected independently for group A and group B allowing conversion to start at a different time for each group. • Group scan mode (with group A priority control selected): — If a group A trigger is input during A/D conversion on group B, the A/D conversion on group B is stopped and A/D conversion is performed on group A. — Restart (rescan) of A/D conversion on group B after completion of A/D conversion on group A can be enabled.	• Group scan mode: — Either two (A and B) or three (A, B, and C) groups can be selected. (When the number of groups selected is two, only the combination of group A and group B is selectable.) — The analog inputs of user-selected channels, the temperature sensor output (unit 1 only), or the internal reference voltage (unit 1 only) are divided up among group A and group B, or among groups A, B, and C, and A/D conversion is performed only once on the analog inputs selected as a group unit. — The scanning start conditions (synchronous triggers) can be selected independently for group A, group B, and group C, allowing conversion to start at a different time for each group. • Group scan mode (with group priority control selected): — If a trigger for a higher-priority group occurs when A/D conversion on a lower-priority group is in progress, scanning of the lower-priority group is stopped and scanning of the higher-priority group starts. Regarding the priority sequence, a setting is available to specify whether or not scanning of the lower-priority group restarts (rescan) after scanning finishes of group A (high priority), group B (middle priority), and group C (low priority). For rescanning, a setting is available to specify whether to start from the first of the selected channels or from the next unscanned channel after the last channel on which A/D conversion completed.

Item	RX64M (S12ADC)	RX65N (S12ADFa)
A/D conversion start conditions	• Software trigger • Synchronous trigger Conversion start is triggered by the MTU, TMR, TPU, ELC, and GPT. • Asynchronous trigger A/D conversion can be started by the external trigger ADTRG0# pin (unit 0) or ADTRG1# pin (unit 1).	• Software trigger • Synchronous trigger Conversion start is triggered by the MTU, TMR, TPU, and ELC. • Asynchronous trigger A/D conversion can be started by the external trigger ADTRG0# pin (unit 0) or ADTRG1# pin (unit 1).
Functions	• Sample-and-hold function • Channel-dedicated sample-and-hold function (3 channels: unit 0 only) • Variable sampling state count • Self-diagnostic function for 12-bit A/D converter • Selectable A/D-converted value adding mode or averaging mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Function for switching among 12-, 10-, and 8-bit conversion • A/D data register auto-clear function • Extended analog input function • Digital comparison function (comparison of values in the comparison register and the data register, and comparison of values in the data registers)	• Sample-and-hold function • Channel-dedicated sample-and-hold function (3 channels: unit 0 only) • Variable sampling state count • Self-diagnostic function for 12-bit A/D converter • Selectable A/D-converted value adding mode or averaging mode • Analog input disconnection detection assist function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Function for switching among 12-, 10-, and 8-bit conversion • A/D data register auto-clear function • Extended analog input function • Compare function (window A, window B)

Item	RX64M (S12ADC)	RX65N (S12ADFa)
Interrupt sources	• In modes other than double trigger mode and group scan mode, an A/D scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of a single scan. • In double trigger mode, an A/D scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of a double scan. • In group scan mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of a group A scan. On completion of a group B scan a dedicated group B scan end interrupt request (GBADI or GBADI1) can be generated. • When double trigger mode is selected in group scan mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of two scans of group A. On completion of two scans of group B a dedicated group B or group C scan end interrupt request (GBADI or GBADI1) can be generated. • A compare interrupt (S12CMPAI or S12CMPAI1) can be generated when the digital compare function comparison conditions are met. • The DMAC or DTC can be activated by the S12ADI/S12ADI1 or BADI/GBADI1 interrupt.	• In modes other than double trigger mode and group scan mode, an A/D scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of a single scan. • In double trigger mode, an A/D scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of a double scan. • In group scan mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of a group A scan. On completion of a group B scan a dedicated group B scan end interrupt request (GBADI or GBADI1) can be generated, and on completion of a group C scan a dedicated group C scan end interrupt request (GCADI or GCADI1) can be generated. • When double trigger mode is selected in group scan mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of two scans of group A. On completion of two scans of group B or C a dedicated group B or group C scan end interrupt request (GBADI/GCADI or GBADI1/GCADI1) can be generated. • A compare interrupt (S12CMPAI, S12CMPAI1, S12CMPBI, or S12CMPBI1) can be generated when the digital compare function comparison conditions are met. • The DMAC or DTC can be activated by the S12ADI/S12ADI1, BADI/GBADI1, or GCADI/GCADI1 interrupt.
Event link function	• In group scan mode an ELC event is generated on completion of scans of groups other than group B. • Scanning can be started by a trigger from the ELC.	• An ELC event can be generated at end of all scans. • Scanning can be started by a trigger from the ELC.
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Table 2.44 Comparative Listing of 12-Bit A/D Converter Registers

Register	Bit	RX64M (S12ADC)	RX65N (S12ADFa)
S12AD.ADANSA0	ANSA0[15:0] (RX64M) ANSA007–ANSA000 (RX65N)	A/D conversion channel select bits	A/D conversion channel select bits
S12AD1.ADANSA0	ANSA0[15:0] (RX64M) ANSA015–ANSA000 (RX65N)	A/D conversion channel select bits	A/D conversion channel select bits
ADANSA1	ANSA1[4:0] (RX64M) ANSA104–ANSA100 (RX65N)	A/D conversion channel select bits	A/D conversion channel select bits
S12AD.ADANSB0	ANSB0[15:0] (RX64M) ANSB007–ANSB000 (RX65N)	A/D conversion channel select bits	A/D conversion channel select bits
S12AD1.ADANSB0	ANSB0[15:0] (RX64M) ANSB015–ANSB000 (RX65N)	A/D conversion channel select bits	A/D conversion channel select bits
ADANSB1	ANSB1[4:0] (RX64M) ANSB104–ANSB100 (RX65N)	A/D conversion channel select bits	A/D conversion channel select bits
ADANSC0	—	—	A/D channel select register C0
ADANSC1	—	—	A/D channel select register C1
S12AD.ADADS0	ADS0[15:0] (RX64M) ADS007–ADS000 (RX65N)	A/D-converted value addition/average channel select bits	A/D-converted value addition/average channel select bits
S12AD1.ADADS0	ADS0[15:0](RX64M) ADS015–ADS000 (RX65N)	A/D-converted value addition/average channel select bits	A/D-converted value addition/average channel select bits
ADADS1	ADS1[4:0] (RX64M) ADS104–ADS100 (RX65N)	A/D-converted value addition/average channel select bits	A/D-converted value addition/average channel select bits
ADADC	ADC	Addition count select bit (b1, b0) b1 b0 0 0: 1-time conversion 0 1: 2-time conversion 1 0: 3-time conversion 1 1: 4-time conversion Do not set to values other than the above.	Addition count select bit (b2, b1, b0) b2 b0 0 0 0: 1-time conversion 0 0 1: 2-time conversion 0 1 0: 3-time conversion 0 1 1: 4-time conversion 1 0 1: 16-time conversion Do not set to values other than the above.
ADGCEXCR	—	—	A/D group C extended input control register
ADGCTRGR	—	—	A/D group C trigger select register

Register	Bit	RX64M (S12ADC)	RX65N (S12ADFa)
ADGSPCR	PGS	Group A priority control setting bit	Group priority control setting bit
	GBRSCN	Group B restart setting bit	Low-priority group restart setting bit
	LGRRS	—	Restart channel select bit
	GBRP	Group B single scan continuous start bit	Single scan continuous start bit
ADCMPCR	CMPAB[1:0]	—	Window A/B complex conditions setting bits
	WCMPE	Window function bit (b6)	Window function setting bit (b14)
	CMPIE	Compare interrupt enable bit	—
	CMPBE	—	Comparison window B enable bit
	CMPAE	—	Comparison window A enable bit
	CMPBIE	—	Comparison window B interrupt enable bit
	CMPAIE	—	Comparison window A interrupt enable bit
S12AD.ADCMPANSR0	CMPS0[15:0] (RX64M) CMPCHA007–CMPCHA000 (RX65N)	Compare channel select bits	Comparison window A channel select bits
S12AD1.ADCMPANSR0	CMPS0[15:0] (RX64M) CMPCHA015–CMPCHA000 (RX65N)	Compare channel select bits	Comparison window A channel select bits
ADCMPANSR1	CMPS1[4:0] (RX64M) CMPCHA104–CMPCHA000 (RX65N)	Compare channel select bits	Comparison window A channel select bits
S12AD.ADCMPLR0	CMPL0[15:0] (RX64M) CMPLCHA007–CMPLCHA000 (RX65N)	Compare level select bits	Comparison window A comparison condition select bits
S12AD1.ADCMPLR0	CMPL0[15:0] (RX64M) CMPLCHA015–CMPLCHA000 (RX65N)	Compare level select bits	Comparison window A comparison condition select bits
ADCMPLR1	CMPL1[4:0] (RX64M) CMPLCHA104–CMPLCHA000 (RX65N)	Compare level select bits	Comparison window A comparison condition select bits
ADCMPDR0	—	A/D compare data register 0	A/D comparison function window A lower level setting register
ADCMPDR1	—	A/D compare data register 1	A/D comparison function window A upper level setting register
S12AD.ADCMPSR0	CMPF0[15:0] (RX64M) CMPSTCHA007–CMPSTCHA 000 (RX65N)	Compare flag	Comparison window A flag
S12AD1.ADCMPSR0	CMPF0[15:0] (RX64M) CMPSTCHA015–CMPSTCHA 000 (RX65N)	Compare flag	Comparison window A flag

Register	Bit	RX64M (S12ADC)	RX65N (S12ADFa)
ADCMPSR1	CMPF1[4:0] (RX64M) CMPSTCHA104–CMPSTCHA000 (RX65N)	Compare flag	Comparison window A flag
ADWINMON	—	—	A/D comparison function window A/B status monitoring register
ADCMPBNSR	—	—	A/D comparison function window B channel select register
ADWINLLB	—	—	A/D comparison function window B lower level setting register
ADWINULB	—	—	A/D comparison function window B upper level setting register
ADCMPBSR	—	—	A/D comparison function window B channel status register
ADSAM	—	—	A/D conversion time setting register
ADSAMPR	—	—	A/D conversion time setting protection release register

2.24 12-Bit D/A Converter

Table 2.45 shows a comparative listing of the 12-Bit D/A Converter registers.

Table 2.45 Comparative Listing of 12-Bit D/A Converter Registers

Register	Bit	RX64M	RX65N
DAASWCR	—	—	D/A Output Amplifier Stabilization Wait Control Register

2.25 RAM

Table 2.46 shows a comparative overview of the RAM specifications, and Table 2.47 shows a comparative listing of the RAM registers.

Table 2.46 Comparative Overview of RAM

	RX64M		RX65N
Item	No ECC Error Correction	ECC Error Correction (ECCRAM)	No ECC Error Correction
RAM capacity	512 Kbytes (RAM0: 512 Kbytes)	32 Kbytes	256 Kbytes (RAM0: 256 Kbytes) 384 Kbytes *1 (Expansion RAM)
RAM address	RAM0: 0000 0000h to 0007 FFFFh	ECCRAM0: 00FF 8000h to 00FF FFFFh	RAM0: 0000 0000h to 0003 FFFFh Expansion RAM: 0080 0000h to 0085 FFFFh *1
Access	• The RAM can be enabled or disabled. • Single-cycle access is possible for both reading and writing.	• The ECCRAM can be enabled or disabled. • Without ECC error correction: Access is done in two cycles for both reading and writing. • With ECC error correction (when no error has occurred): Access is done in two cycles for both reading and writing. • With ECC error correction (when an error has occurred): Access is done in three cycles for both reading and writing.	• The RAM can be enabled or disabled. • Single-cycle access is possible for both reading and writing.
Data retention function	Data is not retained in deep software standby mode.	Data is not retained in deep software standby mode.	Data is not retained in deep software standby mode.
Low power consumption function	Module stop state can be set.	Module stop state can be set.	Module stop state can be set.
Error checking function	• Detection of 1-bit errors • Generation of non-maskable interrupt or interrupt when an error occurs	• ECC error correction function Correction of 1-bit errors and detection of 2-bit errors • Generation of non-maskable interrupt or interrupt when an error occurs	• Detection of 1-bit errors • Generation of non-maskable interrupt or interrupt when an error occurs

*1: Can be used for products with at least 1.5 Mbytes of code flash memory.

Table 2.47 Comparative Listing of RAM Registers

Register	Bit	RX64M	RX65N
ECCRAMMODE	—	ECCRAM operating mode control register	—
ECCRAM2STS	—	ECCRAM 2-bit error status register	—
ECCRAM1STSEN	—	ECCRAM 1-bit error information update enable register	—
ECCRAM1STS	—	ECCRAM 1-bit error status register	—
ECCRAMPRCR	—	ECCRAM protection register	—
ECCRAM2ECAD	—	ECCRAM 2-bit error address capture register	—
ECCRAM1ECAD	—	ECCRAM 1-bit error address capture register	—
ECCRAMPRCR2	—	ECCRAM protection register 2	—
ECCRAMTST	—	ECCRAM test control register	—
EXRAMMODE	—	—	Expansion RAM Operating Mode Control Register *1
EXRAMSTS	—	—	Expansion RAM Error Status Register *1
EXRAMECAD	—	—	Expansion RAM Error Address Capture Register *1
EXRAMPRCR	—	—	Expansion RAM Protection Register *1

*1: Can be used for products with at least 1.5 Mbytes of code flash memory.

2.26 Flash Memory (Code Flash)

Table 2.48 shows a comparative overview of the flash memory (code flash) specifications, and Table 2.49 shows a comparative listing of the flash memory registers.

Table 2.48 Comparative Overview of Flash Memory (Code Flash) Specifications

Item	RX64M	RX65N
Memory space	• User area: Maximum 4 Mbytes • User boot area: 32 Kbytes	• User area: Maximum 2 Mbyte*1
Cache	Not provided	• Capacity: Max. 256 bytes • Mapping method: 8-way set associative • Replacement method: LRU algorithm • Line size: 16 bytes
Read cycle	High-speed read operation using 1 cycle of ICLK is supported.	• When cache hit occurs: 1 cycle • When cache miss occurs: 1 cycle if ICLK ≤ 50 MHz, 2 cycles if 50 MHz < ICLK ≤ 100 MHz, 3 cycles if ICLK > 100 MHz
Value after erase	FFh	FFh
Programming/ erasing method	• Programming and erasing the code flash memory/data flash memory is handled by the FACI commands specified in the FACI command issuing area (007E 0000h). • Programming through transfer by a dedicated flash-memory programmer via a serial interface (serial programming) • Programming of flash memory by a user program (self-programming)	• Programming and erasing the code flash memory is handled by the FACI commands specified in the FACI command issuing area (007E 0000h) • Programming/erasure through transfer by a dedicated flash-memory programmer via a serial interface (serial programming) • Programming/erasure of flash memory by a user program (self-programming)
Security function	Prevents unauthorized modification or reading of data.	Prevents unauthorized modification or reading of data.
Protection function	Prevents unintentional programming of the flash memory.	Prevents unintentional programming of the flash memory.
Dual bank function *1	—	The dual-bank structure makes a safe update possible in cases where programming is suspended. • Linear mode: the code flash memory is used as one area • Dual mode: the code flash memory is divided into two areas
Trusted Memory (TM) function	Prevents unauthorized reading of blocks 8 and 9 in the code flash memory.	Prevents unauthorized reading of blocks 8 and 9 in the code flash memory. Dual mode: blocks 8, 9 ,46, and 47 *1
Background operation (BGO) function	• Read access to the code flash memory is possible while the code flash memory is being programmed. • Read access to the code flash memory is possible while the data flash memory is being programmed.	• The code flash memory can be read while the code flash memory is being programmed or erased. *1 • The data flash memory can be read while the code flash memory is being programmed or erased. *1 • The code flash memory can be read while the data flash memory is being programmed or erased. *1

Item	RX64M	RX65N
Units of programming and erasure	• Programming the user area and user boot area: 256 bytes • Erasing the user area: One block	• Programming the user area: 128 bytes • Erasing the user area: One block
Other functions	Interrupts can be accepted during self-programming.	Interrupts can be accepted during self-programming.
	In the initial settings of this MCU, an expansion area of the option-setting memory can be set.	In the initial settings of this MCU, an expansion area of the option-setting memory can be set.
On-board programming	• Programming/erasure in boot mode (for the SCI interface) — The asynchronous serial interface (SCI1) is used. — The transfer rate is adjusted automatically. — The user boot area can also be programmed or erased.	• Programming/erasure in boot mode (for the SCI interface) — The asynchronous serial interface (SCI1) is used. — The transfer rate is adjusted automatically.
	• Programming/erasure in boot mode (for the USB interface) — USBb is used. — Dedicated hardware is not required, so direct connection to a PC is possible.	• Programming/erasure in boot mode (for the USB interface) — USBb is used. — Dedicated hardware is not required, so direct connection to a PC is possible.
	• Programming/erasure in user boot mode — Able to create original boot programs of the user's making.	• Programming/erasure in boot mode (for the FINE interface) — FINE is used.
	• Programming/erasure by a routine for code flash memory/data flash memory programming within the user program. — This allows code flash memory/data flash memory programming/erasure without resetting the system..	• Programming and erasure by self-programming. — This allows code flash memory programming/erasure without resetting the system.
Programming and erasure by dedicated parallel programmer	A flash programmer can be used to program or erase the user area and user boot area.	Programming and erasure of the code flash memory and option-setting memory by using a parallel programmer is possible.
Unique ID	A 12-byte ID code provided for each MCU	A 16-byte ID code provided for each MCU

*1: Can be used for products with at least 1.5 Mbytes of code flash memory.

Table 2.49 Comparative Listing of Flash Memory Registers

Register	Bit	RX64M	RX65N
FWEPROR	FLWE[1:0]	Flash programming and erasure bits b1 b0 0 0: Programming/erasure, programming/erasure of lock bits, and blank checking disabled. 0 1: Programming/erasure, programming/erasure of lock bits, and blank checking enabled. 1 0: Programming/erasure, programming/erasure of lock bits, and blank checking disabled. 1 1: Programming/erasure, programming/erasure of lock bits, and blank checking disabled.	Flash programming and erasure enable bits b1 b0 0 0: Programming/erasure, and blank checking *1 disabled. 0 1: Programming/erasure, and blank checking *1 enabled. 1 0: Programming/erasure, and blank checking *1 disabled. 1 1: Programming/erasure, and blank checking *1 disabled.
FASTAT	ECRCT	Error flag	—
	DFAE	Data flash memory access violation flag	Data Flash Access Error Flag *1
FAEINT	ECRCTIE	Error interrupt enable bit	—
	DFAEIE	Data flash memory access violation interrupt enable bit	Data Flash Access Error Interrupt Enable *1
FEADDR	—	FACI command end address register	—
FCURAME	—	FCURAM enable register	—
FSTATR	FRCRCT	1-bit error correction monitor flag	—
	FRDTCT	2-bit error detection monitor flag	—
	FCUERR	FCU error flag	—
	FRDY	Flash ready flag 0: The programming, block erase, P/E suspend, P/E resume, forced end, blank checking, configuration settings, lock bit programming, or lock bit read command is being processed. 1: The above processing is not running.	Flash ready flag 0: Programming, block erase, multi-block erase, P/E suspend, P/E resume, forced stop, blank check, or configuration setting command processing is in progress. 1: None of the above is in progress.
	OTEER	—	Other error flag
	SECERR	—	Security error flag
	FESETERR	—	FENTRY setting error flag
	ILGCOMERR	—	Illegal command error flag
FENTRYR	FENTRYD	Data flash memory P/E mode entry bit	Data Flash Memory P/E Mode Entry *1
FPROTR	—	Flash protection register	—

Register	Bit	RX64M	RX65N
FSUINITR	SUINIT	Set-up initialization bit 0: The FEADDR, FPROTR, FCPSR, FSADDR, FENTRYR, and FBCCNT flash sequencer set-up registers keep their current values. 1: The FEADDR, FPROTR, FCPSR, FSADDR, FENTRYR, and FBCCNT flash sequencer set-up registers are initialized.	Set-up initialization bit 0: The FEADDR, FCPSR, FSADDR, FENTRYR, and FBCCNT flash sequencer set-up registers keep their current values. 1: The FEADDR, FCPSR, FSADDR, FENTRYR, and FBCCNT flash sequencer set-up registers are initialized.
FLKSTAT	—	Lock bit status register	—
FPESTAT	—	Flash P/E status register	—
FBCCNT	—	Data flash blank check control register	Data Flash Blank Check Control Register *1
FBCSTAT	—	Data flash blank check status register	Data Flash Blank Check Status Register *1
FPSADDR	—	Data flash programming start address register	Data Flash Programming Start Address Register *1
FAWMON	—	—	Flash access window monitor register
FSUACR	—	—	Start-up area control register
ROMCE	—	—	ROM cache enable register
ROMCIV	—	—	ROM cache invalidate register
UIDR	—	Unique ID register n (n = 0 to 2)	Unique ID register n (n = 0 to 3)
EEPFCLK	—	—	Data Flash Memory Access Frequency Setting Register *1

*1: Can be used for products with at least 1.5 Mbytes of code flash memory.

2.27 Flash Memory (Data Flash)

Table 2.50 shows a comparative overview of the flash memory (Data flash) specifications.

Table 2.50 Comparative Overview of Flash Memory (Data Flash) Specifications

Item	RX64M	RX65N *1
Memory capacity	64 Kbytes	32 Kbytes
Value after erasure	Undefined	Undefined
Block configuration	Block: 64 bytes	Block: 64 bytes
Number of blocks	1024	512

*1: Can be used for products with at least 1.5 Mbytes of code flash memory.

2.28 Package (LQFP100/144 only)

There are some differences in the outline drawing of the LQFP100, LQFP144 package, so please be careful when designing the board.

For details, see Rxxxxx.

Table 2.51 Comparison of package codes

Item	RX64M	RX65N/RX651
100 pin LFQFP	PLQP0100KB-A	PLQP0100KB-B
144 pin LFQFP	PLQP0144KA-A	PLQP0144KA-B

3. Comparison of Pin Functions

The pin functions are compared below, and a comparative overview of power supply, clock, and system control pins is provided. Items present on only one group are shown in blue, and items present on both groups but with points of difference are shown in red. Items with identical specifications on both groups are shown in **black**.

3.1 144-Pin Package

Table 3.1 lists the pin functions on products with the 144-pin package.

Table 3.1 Comparison of Pin Functions on 144-Pin Package Products

144-Pin LFQFP	145-Pin TFLGA	RX64M	RX65N
1	A1	AVSS0	AVSS0
2	B3	P05/IRQ13/DA1	P05/IRQ13/DA1
3	B1	AVCC1	AVCC1
4	D3	P03/IRQ11/DA0	P03/IRQ11/DA0
5	C1	AVSS1	AVSS1
6	C2	P02/TMCI1/SCK6/IRQ10/AN120	P02/TMCI1/SCK6/IRQ10/AN120
7	D4	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/AN119	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/AN119
8	D1	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/AN118	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/AN118
9	D2	PF5/IRQ4	PF5/IRQ4
10	E4	EMLE	EMLE
11	E3	PJ5/POE8#/ CTS2#/RTS2#/SS2#	PJ5/POE8#/CTS2#/RTS2#/SS2#
12	A10	VSS	VSS
13	F3	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/ CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0#	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/ CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0#
14	E2	VCL	VCL
15	F4	VBATT	VBATT
16	G3	MD/FINED	MD/FINED
17	F1	XCIN	XCIN
18	F2	XCOUT	XCOUT
19	G2	RES#	RES#
20	G1	P37/XTAL	P37/XTAL
21	C6	VSS	VSS
22	H1	P36/EXTAL	P36/EXTAL
23	B10	VCC	VCC
24	H4	P35/UPSEL/NMI	P35/UPSEL/NMI
25	J1	P34/TRST#/MTIOC0A/TMCI3/PO12/POE10#SCK6/SCK0/ET0_LINKSTA/IRQ4	P34/TRST#/MTIOC0A/TMCI3/PO12/POE10#/SCK6/SCK0/ET0_LINKSTA/IRQ4
26	J2	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/POE4#/POE11#/RXD6/RXD0/SMISO6/SMISO0/SSCL6/SSCL0/CRX0/ PCKO/IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/POE4#/POE11#/RXD6/RXD0/SMISO6/SMISO0/SSCL6/SSCL0/CRX0/ PCKO/IRQ3-DS
27	J3	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCOUT/RTCIC2/POE0#/POE10#/ TXD6/TXD0/SMOSI6/SMOSI0/SSDA6/ SSDA0/CTX0/USB0_VBUSEN/VSYNC/ IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCOUT/RTCIC2/POE0#/POE10#/TXD6/TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS

144-Pin LFQFP	145-Pin TFLGA	RX64M	RX65N
28	K3	P31/TMS/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/IRQ1-DS	P31/TMS/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS
29	J4	P30/TDI/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/IRQ0-DS	P30/TDI/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS
30	K1	P27/TCK/CS7#/MTIOC2B/TMCI3/PO7/SCK1	P27/TCK/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB-A
31	K2	P26/TDO/CS6#/MTIOC2A/TMO1/PO6/TXD1/CTS3#/RTS3#/SMOSI1/SS3#/SSDA1	P26/TDO/CS6#/MTIOC2A/TMO1/PO6/TXD1/CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/MOSIB-A
32	L1	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/SSIDATA1/HSYNC/ADTRG0#	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/HSYNC/ADTRG0#/(SDHI_CD)*1
33	L4	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/SSISCK1/PIXCLK	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/PIXCLK/(SDHI_WP)*1
34	L2	P23/EDACK0/MTIOC3D/MTCLKD/GTIOC0A-B/TIOCD3/PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/SSDA3/SSISCK0/PIXD7	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/SSDA3/PIXD7/(SDHI_D1-C)*1
35	M1	P22/EDREQ0/MTIOC3B/MTCLKC/GTIOC1A-B/TIOCC3/TMO0/PO2/SCK0/USB0_OVRCURB/AUDIO_MCLK/PIXD6	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_OVRCURB/PIXD6/(SDHI_D0-C)*1
36	N1	P21/MTIOC1B/MTIOC4A/GTIOC2A-B/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/USB0_EXICEN/SSIWS0/PIXD5/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/USB0_EXICEN/PIXD5/IRQ9/(SCL1/SDHI_CLK-C)*1
37	N2	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/USB0_ID/SSIRXD0/PIXD4/IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/USB0_ID/PIXD4/IRQ8/(SDA1/SDHI_CMD-C)*1
38	M2	P17/MTIOC3A/MTIOC3B/MTIOC4B/GTIOC0B-B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/SSITXD0/PIXD3/IRQ7/ADTRG1#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/PIXD3/IRQ7/ADTRG1#/(SDHI_D3-C)*1
39	N3	P87/MTIOC4C/GTIOC1B-B/TIOCA2/TXD10/PIXD2	P87/MTIOC4C/TIOCA2/TXD10/SMOSI10/SSDA10/PIXD2/(SDHI_D2-C)*1
40	L3	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/SMISO3/SSDA1/SSCL3/SCL2-DS/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/SMISO3/SSDA1/SSCL3/SCL2-DS/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/IRQ6/ADTRG0#
41	M3	P86/MTIOC4D/GTIOC2B-B/TIOCA0/RXD10/PIXD1	P86/MTIOC4D/TIOCA0/RXD10/SMISO10/SSCL10/PIXD1
42	K4	P15/MTIOC0B/MTCLKB/GTETRG-B/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/CRX1-DS/SSIWS1/PIXD0/IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/CRX1-DS/PIXD0/IRQ5
43	N4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA/IRQ4

144-Pin LFQFP	145-Pin TFLGA	RX64M	RX65N
44	L5	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG1#	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG1#
45	M4	P12/TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/IRQ2	P12/TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/IRQ2
46	M5	VCC_USB	VCC_USB
47	N5	USB0_DM	USB0_DM
48	N6	USB0_DP	USB0_DP
49	M6	VSS_USB	VSS_USB
50	L6	P56/EDACK1/MTIOC3C/TIOCA1	P56/EDACK1/MTIOC3C/TIOCA1/(SCK7)*1
51	N7	P55/TRDATA3/WAIT#/EDREQ0/MTIOC4D/TMO3/CRX1/ET0_EXOUT/IRQ10	P55/TRDATA3/WAIT#/EDREQ0/MTIOC4D/TMO3/CRX1/ET0_EXOUT/IRQ10/(D0[A0/D0]/TXD7/SMOSI7/SSDA7)*1
52	K5	P54/TRDATA2/ALE/EDACK0/MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/CTX1/ET0_LINKSTA	P54/TRDATA2/ALE/EDACK0/MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/CTX1/ET0_LINKSTA/(D1[A1/D1])*1
53	K6	P53/BCLK	P53/BCLK
54	L7	P52/RD#/RXD2/SMISO2/SSCL2	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A
55	K7	P51/WR1#/BC1#/WAIT#/SCK2	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A
56	M7	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1-A
57	C13	VSS	VSS
58	L8	P83/TRCLK/EDACK1/MTIOC4C/GTIOC0A-D/CTS10#/ET0_CRS/RMII0_CRS_DV/SCK10	P83/TRCLK/EDACK1/MTIOC4C/CTS10#/SS10#/ET0_CRS/RMII0_CRS_DV/SCK10
59	D5	VCC	VCC
60	N9	PC7/UB/A23/CS0#/MTIOC3A/MTCLKB/GTIOC3A-D/TMO2/TOC0/PO31/CACREF/TXD8/MISOA-A/ET0_COL/MMC_D7-A/IRQ14	PC7/UB/A23/CS0#/MTIOC3A/MTCLKB/TMO2/TOC0/PO31/CACREF/TXD8/SMOSI8/SSDA8/MISOA-A/ET0_COL/TXD10/SMOSI10/SSDA10/MMC_D7-A/IRQ14
61	M8	PC6/A22/CS1#/MTIOC3C/MTCLKA/GTIOC3B-D/TMCI2/TIC0/PO30/RXD8/MOSIA-A/ET0_ETXD3/MMC_D6-A/IRQ13	PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/TIC0/PO30/RXD8/SMISO8/SSCL8/MOSIA-A/ET0_ETXD3/RXD10/SMISO10/SSCL10/MMC_D6-A/IRQ13/(D2[A2/D2])*1
62	L9	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/GTIOC1A-D/TMRI2/PO29/SCK8/RSPCKA-A/RTS8#/ET0_ETXD2/MMC_D5-A	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMRI2/PO29/SCK8/RSPCKA-A/ET0_ETXD2/SCK10/MMC_D5-A/(D3[A3/D3])*1
63	N10	P82/TRSYNC/EDREQ1/MTIOC4A/GTIOC2A-D/PO28/TXD10/ET0_ETXD1/RMII0_TXD1/MMC_D4-A	P82/TRSYNC/EDREQ1/MTIOC4A/PO28/TXD10/SMOSI10/SSDA10/ET0_ETXD1/RMII0_TXD1/MMC_D4-A
64	M9	P81/TRDATA1/EDACK0/MTIOC3D/GTIOC0B-D/PO27/RXD10/ET0_ETXD0/RMII0_TXD0/MMC_D3-A/SDHI_CD-A/QIO3-A	P81/TRDATA1/EDACK0/MTIOC3D/PO27/RXD10/SMISO10/SSCL10/ET0_ETXD0/RMII0_TXD0/MMC_D3-A/SDHI_CD-A/QIO3-A/(SDHI_CD)*1

144-Pin LFQFP	145-Pin TFLGA	RX64M	RX65N
65	K9	P80/TRDATA0/EDREQ0/MTIOC3B/PO26/SCK10/RTS10#/ET0_TX_EN/RMII0_TXD_EN/MMC_D2-A/SDHI_WP-A/QIO2-A	P80/TRDATA0/EDREQ0/MTIOC3B/PO26/SCK10/RTS10#/ET0_TX_EN/RMII0_TXD_EN/MMC_D2-A/SDHI_WP-A/QIO2-A/(SDHI_WP)*1
66	L10	PC4/A20/CS3#/MTIOC3D/MTCLKC/GTETRG-D/TMCI1/PO25/POE0#/SCK5/CTS8#/SSLA0-A/ET0_TX_CLK/MMC_D1-A/SDHI_D1-A/QIO1-A/QMI-A	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0-A/ET0_TX_CLK/CTS10#/RTS10#/SS10#/MMC_D1-A/SDHI_D1-A/SDSI_D1-A/QIO1-A/QMI-A
67	N11	PC3/A19/MTIOC4D/GTIOC1B-D/TCLKB/PO24/TXD5/SMOSI5/SSDA5/ET0_TX_ER/MMC_D0-A/SDHI_D0-A/QIO0-A/QMO-A	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/SMOSI5/SSDA5/ET0_TX_ER/MMC_D0-A/SDHI_D0-A/SDSI_D0-A/QIO0-A/QMO-A
68	M10	P77/CS7#/PO23/TXD11/ET0_RX_ER/RMII0_RX_ER/MMC_CLK-A/SDHI_CLK-A/QSPCLK-A	P77/TRDATA7/CS7#/PO23/TXD11/SMOSI10/SSDA10/ET0_RX_ER/RMII0_RX_ER/MMC_CLK-A/SDHI_CLK-A/SDSI_CLK-A/QSPCLK-A
69	K10	P76/CS6#/PO22/RXD11/ET0_RX_CLK/REF50CK0/MMC_CMD-A/SDHI_CMD-A/QSSL-A	P76/TRDATA6/CS6#/PO22/RXD11/SMISO11/SSCL11/ET0_RX_CLK/REF50CK0/MMC_CMD-A/SDHI_CMD-A/SDSI_CMD-A/QSSL-A
70	L11	PC2/A18/MTIOC4B/GTIOC2B-D/TCLKA/PO21/RXD5/SMISO5/SSCL5/SSLA3-A/ET0_RX_DV/MMC_CD-A/SDHI_D3-A	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/SMISO5/SSCL5/SSLA3-A/ET0_RX_DV/MMC_CD-A/SDHI_D3-A/SDSI_D3-A
71	N12	P75/CS5#/PO20/SCK11/RTS11#/ET0_ERXD0/RMII0_RXD0/MMC_RES#-A/SDHI_D2-A	P75/TRSYNC1/CS5#/PO20/SCK11/RTS11#/ET0_ERXD0/RMII0_RXD0/MMC_RES#-A/SDHI_D2-A/SDSI_D2-A
72	N13	P74/A20/CS4#/PO19/CTS11#/ET0_ERXD1/RMII0_RXD1	P74/TRDATA5/A20/CS4#/PO19/CTS11#/SS11#/ET0_ERXD1/RMII0_RXD1
73	M12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/SSLA2-A/ET0_ERXD2/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/SSLA2-A/ET0_ERXD2/IRQ12
74	D11	VCC	VCC
75	M11	PC0/A16/MTIOC3C/TCLKC/PO17CTS5#/RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14
76	E1	VSS	VSS
77	L12	P73/CS3#/PO16/ET0_WOL	P73/TRDATA4/CS3#/PO16/ET0_WOL
78	K11	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ET0_CRS/RMII0_CRS_DV	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/SMOSI9/SSDA9/ET0_CRS/RMII0_CRS_DV/TXD11/SMOSI11/SSDA11/SDSI_D1-B
79	K12	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ET0_ETXD1/RMII0_TXD1	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/SMISO9/SSCL9/ET0_ETXD1/RMII0_TXD1/RXD11/SMISO11/SSCL11/SDSI_D0-B
80	K13	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/POE4#/SCK9/RTS9#/ET0_ETXD0/RMII0_TXD0	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/POE4#/SCK9/ET0_ETXD0/RMII0_TXD0/SCK11/SDSI_CLK-B/(LCD_CLK-B)*1

144-Pin LFQFP	145-Pin TFLGA	RX64M	RX65N
81	J11	PB4/A12/TIOCA4/PO28/CTS9#/ET0_TX_EN/RMII0_TXD_EN	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/SS9#/ET0_TX_EN/RMII0_TXD_EN/CTS11#/RTS11#/SS11#/SDSI_CMD-B/(LCD_TCON0-B)*1
82	J10	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ET0_RX_ER/RMII0_RX_ER	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ET0_RX_ER/RMII0_RX_ER/SDSI_D3-B/(LCD_TCON1-B)*1
83	J12	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/RTS4#/CTS6#/RTS6#/SS4#/SS6#/ET0_RX_CLK/REF50CK0	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/RTS4#/CTS6#/RTS6#/SS4#/SS6#/ET0_RX_CLK/REF50CK0/SDSI_D2-B/(LCD_TCON2-B)*1
84	J13	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/TXD4/TXD6/SMOSI4/SMOSI6/SSDA4/SSDA6/ET0_ERXD0/RMII0_RXD0/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/TXD4/TXD6/SMOSI4/SMOSI6/SSDA4/SSDA6/ET0_ERXD0/RMII0_RXD0/IRQ4-DS/(LCD_TCON3-B)*1
85	H10	P72/A19/CS2#/ET0_MDC	P72/A19/CS2#/ET0_MDC
86	H11	P71/A18/CS1#/ET0_MDIO	P71/A18/CS1#/ET0_MDIO
87	H12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/RXD6/SMISO4/SMISO6/SSCL4/SSCL6/ET0_ERXD1/RMII0_RXD1/IRQ12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/RXD6/SMISO4/SMISO6/SSCL4/SSCL6/ET0_ERXD1/RMII0_RXD1/IRQ12/(LCD_DATA0-B)*1
88	H13	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/(LCD_DATA1-B)*1
89	G11	PA6/A6/MTIC5V/MTCLKB/GTETRG-C/TIOCA2/TMCI3/PO22/POE10#/CTS5#/RTS5#/SS5#/MOSIA-B/ET0_EXOUT	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE10#/CTS5#/RTS5#/SS5#/MOSIA-B/ET0_EXOUT/(LCD_DATA2-B)*1
90	G10	PA5/A5/MTIOC6B/TIOCB1/GTIOC0A-C/PO21/RSPCKA-B/ET0_LINKSTA	PA5/A5/MTIOC6B/TIOCB1/PO21/RSPCKA-B/ET0_LINKSTA/(LCD_DATA3-B)*1
91	G12	VCC	VCC
92	G13	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ET0_MDC/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ET0_MDC/IRQ5-DS/(LCD_DATA4-B)*1
93	F11	VSS	VSS
94	F10	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/RXD5/SMISO5/SSCL5/ET0_MDIO/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/RXD5/SMISO5/SSCL5/ET0_MDIO/IRQ6-DS/(LCD_DATA5-B)*1
95	F13	PA2/A2/MTIOC7A/GTIOC1A-C/PO18/RXD5/SMISO5/SSCL5/SSLA3-B	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/SSCL5/SSLA3-B/(LCD_DATA6-B)*1
96	F12	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/GTIOC2A-C/TIOCB0/PO17/SCK5/SSLA2-B/ET0_WOL/IRQ11	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/PO17/SCK5/SSLA2-B/ET0_WOL/IRQ11/(LCD_DATA7-B)*1
97	E10	PA0/A0/BC0#/MTIOC4A/MTIOC6D/GTIOC0B-C/TIOCA0/CACREF/PO16/SSLA1-B/ET0_TX_EN/RMII0_TXD_EN	PA0/A0/BC0#/MTIOC4A/MTIOC6D/TIOCA0/CACREF/PO16/SSLA1-B/ET0_TX_EN/RMII0_TXD_EN/(LCD_DATA8-B)*1
98	E13	P67/CS7#/DQM1/MTIOC7C/GTIOC1B-C/CRX2/IRQ15	P67/CS7#/DQM1/MTIOC7C/IRQ15
99	E11	P66/CS6#/DQM0/MTIOC7D/GTIOC2B-C/CTX2	P66/CS6#/DQM0/MTIOC7D

144-Pin LFQFP	145-Pin TFLGA	RX64M	RX65N
100	E12	P65/CS5#/CKE	P65/CS5#/CKE
101	D10	PE7/D15[A15/D15]/MTIOC6A/GTIOC3A-E/TOC1/MMC_RES#-B/SDHI_WP-B/IRQ7/AN105	PE7/D15[A15/D15]/MTIOC6A/TOC1/MISOB-B/MMC_RES#-B/SDHI_WP-B/IRQ7/AN105/(D7[A7/D7]/LCD_DATA9-B)*1
102	D13	PE6/D14[A14/D14]/MTIOC6C/GTIOC3B-E/TIC1/MMC_CD-B/SDHI_CD-B/IRQ6/AN104	PE6/D14[A14/D14]/MTIOC6C/TIC1/MOSIB-B/MMC_CD-B/SDHI_CD-B/IRQ6/AN104/(D6[A6/D6]/SDHI_CD/LCD_DATA10-B)*1
103	H2	VCC	VCC
104	C12	P70/SDCLK	P70/SDCLK
105	H3	VSS	VSS
106	D12	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/GTIOC0A-A/ET0_RX_CLK/REF50CK0/IRQ5/AN103	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/ET0_RX_CLK/REF50CK0/RSPCKB-B/IRQ5/AN103/(D5[A5/D5]/LCD_DATA11-B)*1
107	B13	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/GTIOC1A-A/PO28/ET0_ERXD2/AN102	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/PO28/ET0_ERXD2/SSLB0-B/AN102/(D4[A4/D4]/LCD_DATA12-B)*1
108	A13	PE3/D11[A11/D11]/MTIOC4B/GTIOC2A-A/PO26/POE8#/TOC3/CTS12#/RTS12#/SS12#/ET0_ERXD3/MMC_D7-B/AN101	PE3/D11[A11/D11]/MTIOC4B/PO26/POE8#/TOC3/CTS12#/RTS12#/SS12#/ET0_ERXD3/MMC_D7-B/AN101/(D3[A3/D3]/LCD_DATA13-B)*1
109	B12	PE2/D10[A10/D10]/MTIOC4A/GTIOC0B-A/PO23/TIC3/RXD12/SMISO12/SSCL12/RXDX12/MMC_D6-B/IRQ7-DS/AN100	PE2/D10[A10/D10]/MTIOC4A/PO23/TIC3/RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B/MMC_D6-B/IRQ7-DS/AN100/(D2[A2/D2]/LCD_DATA14-B)*1
110	A12	PE1/D9[A9/D9]/MTIOC4C/MTIOC3B/GTIOC1B-A/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/MMC_D5-B/ANEX1	PE1/D9[A9/D9]/MTIOC4C/MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2-B/MMC_D5-B/ANEX1/(D1[A1/D1]/LCD_DATA15-B)*1
111	C11	PE0/D8[A8/D8]/MTIOC3D/GTIOC2B-A/SCK12/MMC_D4-B/ANEX0	PE0/D8[A8/D8]/MTIOC3D/SCK12/SSLB1-B/MMC_D4-B/ANEX0/(D0[A0/D0]/LCD_DATA16-B)*1
112	D9	P64/CS4#/WE#	P64/CS4#/WE#/(D3[A3/D3])*1
113	C10	P63/CS3#/CAS#	P63/CS3#/CAS#/(D2[A2/D2])*1
114	A11	P62/CS2#/RAS#	P62/CS2#/RAS#/(D1[A1/D1])*1
115	B11	P61/CS1#/SDCS#	P61/CS1#/SDCS#/(D0[A0/D0])*1
116	L13	VSS	VSS
117	D8	P60/CS0#	P60/CS0#
118	K8	VCC	VCC
119	C9	PD7/D7[A7/D7]/MTIC5U/POE0#/MMC_D1-B/SDHI_D1-B/QIO1-B/QMI-B/IRQ7/AN107	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3/MMC_D1-B/SDHI_D1-B/QIO1-B/QMI-B/IRQ7/AN107/(SSLC3-A/LCD_DATA17-B)*1

144-Pin LFQFP	145-Pin TFLGA	RX64M	RX65N
120	A9	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/MMC_D0-B/SDHI_D0-B/QIO0-B/QMO-B/IRQ6/AN106	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/SSLC2/MMC_D0-B/SDHI_D0-B/QIO0-B/QMO-B/IRQ6/AN106/(SSLC2-A/LCD_DATA18-B)*1
121	D7	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/MMC_CLK-B/SDHI_CLK-B/QSPCLK-B/IRQ5/AN113	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/SSLC1/MMC_CLK-B/SDHI_CLK-B/QSPCLK-B/IRQ5/AN113/(SSLC1-A/LCD_DATA19-B)*1
122	B9	PD4/D4[A4/D4]/MTIOC8B/POE11#/MMC_CMD-B/SDHI_CMD-B/QSSL-B/IRQ4/AN112	PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0/MMC_CMD-B/SDHI_CMD-B/QSSL-B/IRQ4/AN112/(SSLC0-A/LCD_DATA20-B)*1
123	C8	PD3/D3[A3/D3]/MTIOC8D/GTIOC0A-E/POE8#/TOC2/MMC_D3-B/SDHI_D3-B/QIO3-B/IRQ3/AN111	PD3/D3[A3/D3]/MTIOC8D/POE8#/TOC2/RSPCKC/MMC_D3-B/SDHI_D3-B/QIO3-B/IRQ3/AN111/(RSPCKC-A/LCD_DATA21-B)*1
124	A8	PD2/D2[A2/D2]/MTIOC4D/GTIOC0B-E/TIC2/CRX0/MMC_D2-B/SDHI_D2-B/QIO2-B/IRQ2/AN110	PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0/MISOC/MMC_D2-B/SDHI_D2-B/QIO2-B/IRQ2/AN110/(MISOC-A/LCD_DATA22-B)*1
125	C7	PD1/D1[A1/D1]/MTIOC4B/GTIOC1A-E/POE0#/CTX0/IRQ1/AN109	PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0/MOSIC/IRQ1/AN109/(MOSIC-A/LCD_DATA23-B)*1
126	B8	PD0/D0[A0/D0]/GTIOC1B-E/POE4#/IRQ0/AN108	PD0/D0[A0/D0]/POE4#/IRQ0/AN108/(LCD_EXTCLK-B)*1
127	D6	P93/A19/POE0#/CTS7#/RTS7#/SS7#/AN117	P93/A19/POE0#/CTS7#/RTS7#/SS7#/AN117
128	A7	P92/A18/POE4#/RXD7/SMISO7/SSCL7 AN116	P92/A18/POE4#/RXD7/SMISO7/SSCL7 AN116
129	B7	P91/A17/SCK7/AN115	P91/A17/SCK7/AN115
130	N8	VSS	VSS
131	A6	P90/A16/TXD7/SMOSI7/SSDA7/AN114	P90/A16/TXD7/SMOSI7/SSDA7AN114
132	M13	VCC	VCC
133	B6	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
134	C5	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
135	A5	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
136	E5	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
137	B5	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
138	A4	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
139	C4	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
140	B4	VREFL0	VREFL0
141	A3	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
142	C3	VREFH0	VREFH0
143	B2	AVCC0	AVCC0
144	A2	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#
—	G4	BSCANP	BSCANP

*1: Can be used for products with at least 1.5 Mbytes of code flash memory.

3.2 100-Pin Package

Table 3.2 lists the pin functions on products with the 100-pin package.

Table 3.2 Comparison of Pin Functions on 100-Pin Package Products

100-Pin LFQFP	100-Pin TFLGA	RX64M	RX65N
1	A2	AVCC1	AVCC1
2	B1	EMLE	EMLE
3	C2	AVSS1	AVSS1
4	C3	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0#	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0#
5	C1	VCL	VCL
6	D4	VBATT	VBATT
7	D3	MD/FINED	MD/FINED
8	D1	XCIN	XCIN
9	D2	XCOUT	XCOUT
10	E3	RES#	RES#
11	E1	P37/XTAL	P37/XTAL
12	E2	VSS	VSS
13	F1	P36/EXTAL	P36/EXTAL
14	F2	VCC	VCC
15	F3	P35/UPSEL/NMI	P35/UPSEL/NMI
16	E4	P34/TRST#/MTIOC0A/TMCI3/PO12/POE10#/SCK6/SCK0/ET0_LINKSTA/IRQ4	P34/TRST#/MTIOC0A/TMCI3/PO12/POE10#/SCK6/SCK0/ET0_LINKSTA/IRQ4
17	G1	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/POE4#/POE11#/RXD6/RXD0/SMISO6/SMISO0/SSCL6/SSCL0/CRX0/IRQ3-DS	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/POE4#/POE11#/RXD6/RXD0/SMISO6/SMISO0/SSCL6/SSCL0/CRX0/IRQ3-DS
18	F4	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCOUT/RTCIC2/POE0#/POE10#/TXD6/TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/CTX0/USB0_VBUSEN/IRQ2-DS	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCOUT/RTCIC2/POE0#/POE10#/TXD6/TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/CTX0/USB0_VBUSEN/IRQ2-DS
19	G2	P31/TMS/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/IRQ1-DS	P31/TMS/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS
20	G3	P30/TDI/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/IRQ0-DS	P30/TDI/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS
21	G4	P27/TCK/CS7#/MTIOC2B/TMCI3/PO7/SCK1	P27/TCK/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB-A
22	H1	P26/TDO/CS6#/MTIOC2A/TMO1/PO6/TXD1/CTS3#/RTS3#/SMOSI1/SS3#/SSDA1	P26/TDO/CS6#/MTIOC2A/TMO1/PO6/TXD1/CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/MOSIB_A
23	H2	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/SSIDATA1/ADTRG0#	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/TIOCA4/PO5/RXD3/SMISO3/SSCL3/ADTRG0#
24	J1	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/SSISCK1	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN

100-Pin LFQFP	100-Pin TFLGA	RX64M	RX65N
25	K1	P23/EDACK0/MTIOC3D/MTCLKD/GTIOC0A-B/TIOCD3/PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/SSDA3/SSISCK0	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/SSDA3
26	K2	P22/EDREQ0/MTIOC3B/MTCLKC/GTIOC1A-B/TIOCC3/TMO0/PO2/SCK0/USB0_OVRCURB/AUDIO_MCLK	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_OVRCURB
27	J2	P21/MTIOC1B/MTIOC4A/GTIOC2A-B/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/USB0_EXICEN/SSIWS0/IRQ9	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/USB0_EXICEN/IRQ9/(SCL1)*1
28	K3	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/USB0_ID/SSIRXD0/IRQ8	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/USB0_ID/IRQ8/(SDA1)*1
29	J3	P17/MTIOC3A/MTIOC3B/MTIOC4B/GTIOC0B-B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/SSITXD0/IRQ7/ADTRG1#	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/IRQ7/ADTRG1#
30	H3	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/SMISO3/SSDA1/SSCL3/SCL2-DS/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/SMISO3/SSDA1/SSCL3/SCL2-DS/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/IRQ6/ADTRG0#
31	H4	P15/MTIOC0B/MTCLKB/GTETRG-B/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/CRX1-DS/SSIWS1/IRQ5	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/CRX1-DS/IRQ5
32	K4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA/IRQ4
33	J4	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG1#	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG1#
34	F5	P12/TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/IRQ2	P12/TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/IRQ2
35	J6	VCC_USB	VCC_USB
36	K5	USB0_DM	USB0_DM
37	K6	USB0_DP	USB0_DP
38	J5	VSS_USB0	VSS_USB0
39	H5	P55/WAIT#/EDREQ0/MTIOC4D/TMO3/CRX1/ET0_EXOUT/IRQ10	P55/WAIT#/EDREQ0/MTIOC4D/TMO3/CRX1/ET0_EXOUT/IRQ10/(D0[A0/D0])*1
40	H6	P54/ALE/EDACK0/MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/CTX1/ET0_LINKSTA	P54/ALE/EDACK0/MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/CTX1/ET0_LINKSTA/(D1[A1/D1])*1
41	G5	P53/BCLK	P53/BCLK
42	G6	P52/RD#/RXD2/SMISO2/SSCL2	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A
43	K7	P51/WR1#/BC1#/WAIT#/SCK2	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A
44	J7	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1-A

100-Pin LFQFP	100-Pin TFLGA	RX64M	RX65N
45	H7	PC7/UB/A23/CS0#/MTIOC3A/MTCLKB/GTIOC3A-D/TMO2/TOC0/PO31/CACREF/TXD8/MISOA-A/ET0_COL/IRQ14	PC7/UB/A23/CS0#/MTIOC3A/MTCLKB/TMO2/TOC0/PO31/CACREF/TXD8/SMOSI8/SSDA8/MISOA-A/ET0_COL/TXD10/SMOSI10/SSDA10/IRQ14
46	H8	PC6/A22/CS1#/MTIOC3C/MTCLKA/GTIOC3B-D/TMCI2/TIC0/PO30/RXD8/MOSIA-A/ET0_ETXD3/IRQ13	PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/TIC0/PO30/RXD8/SMISO8/SSCL8/MOSIA-A/ET0_ETXD3/RXD10/SMISO10/SSCL10/IRQ13/(D2[A2/D2])*1
47	K8	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/GTIOC1A-D/TMRI2/PO29/SCK8/RSPCKA-A/RTS8#/ET0_ETXD2	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMRI2/PO29/SCK8/RSPCKA-A/ET0_ETXD2/SCK10/(D3[A3/D3])*1
48	J8	PC4/A20/CS3#/MTIOC3D/MTCLKC/GTETRG-D/TMCI1/PO25/POE0#/SCK5/CTS8#/SSLA0-A/ET0_TX_CLK	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0-A/ET0_TX_CLK/CTS10#/RTS10#/SS10#
49	K9	PC3/A19/MTIOC4D/GTIOC1B-D/TCLKB/PO24/TXD5/SMOSI5/SSDA5/ET0_TX_ER	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/SMOSI5/SSDA5/ET0_TX_ER
50	K10	PC2/A18/MTIOC4B/GTIOC2B-D/TCLKA/PO21/RXD5/SMISO5/SSCL5/SSLA3-A/ET0_RX_DV	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/SMISO5/SSCL5/SSLA3-A/ET0_RX_DV
51	J10	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/SSLA2-A/ET0_ERXD2/IRQ12	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/SSLA2-A/ET0_ERXD2/IRQ12
52	J9	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/SS5#/SSLA1-A/ET0_ERXD3/IRQ14
53	H10	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ET0_CRS/RMII0_CRS_DV	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/SMOSI9/SSDA9/ET0_CRS/RMII0_CRS_DV/TXD11/SMOSI11/SSDA11/SDSI_D1-B
54	H9	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ET0_ETXD1/RMII0_TXD1	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/SMISO9/SSCL9/ET0_ETXD1/RMII0_TXD1/RXD11/SMISO11/SSCL11/SDSI_D0-B
55	G7	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/POE4#/SCK9/RTS9#/ET0_ETXD0/RMII0_TXD0	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/POE4#/SCK9/ET0_ETXD0/RMII0_TXD0/SCK11/SDSI_CLK-B/(LCD_CLK-B)*1
56	G8	PB4/A12/TIOCA4/PO28/CTS9#/ET0_TX_EN/RMII0_TXD_EN	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/SS9#/ET0_TX_EN/RMII0_TXD_EN/CTS11#/RTS11#/SS11#/SDSI_CMD-B/(LCD_TCON0-B)*1
57	F6	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE11#/SCK6/ET0_RX_ER/RMII0_RX_ER	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE11#/SCK6/ET0_RX_ER/RMII0_RX_ER/SDSI_D3-B/(LCD_TCON1-B)*1
58	F7	PB2/A10/TIOCC3/TCLKC/PO26/CTS6#/RTS6#/SS6#/ET0_RX_CLK/REF50CK0	PB2/A10/TIOCC3/TCLKC/PO26/CTS6#/RTS6#/SS6#/ET0_RX_CLK/REF50CK0/SDSI_D2-B/(LCD_TCON2-B)*1

100-Pin LFQFP	100-Pin TFLGA	RX64M	RX65N
59	G9	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/TXD6/SMOSI6/SSDA6/ET0_ERXD0/RMII0_RXD0/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/TXD6/SMOSI6/SSDA6/ET0_ERXD0/RMII0_RXD0/IRQ4-DS/(LCD_TCON3-B)*1
60	G10	VCC	VCC
61	F8	PB0/A8/MTIC5W/TIOCA3/PO24/RXD6/SMISO6/SSCL6/ET0_ERXD1/RMII0_RXD1/IRQ12	PB0/A8/MTIC5W/TIOCA3/PO24/RXD6/SMISO6/SSCL6/ET0_ERXD1/RMII0_RXD1/IRQ12/(LCD_DATA0-B)*1
62	F10	VSS	VSS
63	F9	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL	PA7/A7/TIOCB2/PO23/MISOA-B/ET0_WOL/(LCD_DATA1-B)*1
64	E7	PA6/A6/MTIC5V/MTCLKB/GTETRG-C/TIOCA2/TMCI3/PO22/POE10#/CTS5#/RTS5#/SS5#/MOSIA-B/ET0_EXOUT	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE10#/CTS5#/RTS5#/SS5#/MOSIA-B/ET0_EXOUT/(LCD_DATA2-B)*1
65	E9	PA5/A5/MTIOC6B/TIOCB1/GTIOC0A-C/PO21/RSPCKA-B/ET0_LINKSTA	PA5/A5/MTIOC6B/TIOCB1/PO21/RSPCKA-B/ET0_LINKSTA/(LCD_DATA3-B)*1
66	E8	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ET0_MDC/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ET0_MDC/IRQ5-DS/(LCD_DATA4-B)*1
67	E10	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/RXD5/SMISO5/SSCL5/ET0_MDIO/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19/RXD5/SMISO5/SSCL5/ET0_MDIO/IRQ6-DS/(LCD_DATA5-B)*1
68	E6	PA2/A2/MTIOC7A/GTIOC1A-C/PO18/RXD5/SMISO5/SSCL5/SSLA3-B	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/SSCL5/SSLA3-B/(LCD_DATA6-B)*1
69	D9	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/GTIOC2A-C/TIOCB0/PO17/SCK5/SSLA2-B/ET0_WOL/IRQ11	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/PO17/SCK5/SSLA2-B/ET0_WOL/IRQ11/(LCD_DATA7-B)*1
70	D10	PA0/A0/BC0#/MTIOC4A/MTIOC6D/GTIOC0B-C/TIOCA0/CACREF/PO16/SSLA1-B/ET0_TX_EN/RMII0_TXD_EN	PA0/A0/BC0#/MTIOC4A/MTIOC6D/TIOCA0/CACREF/PO16/SSLA1-B/ET0_TX_EN/RMII0_TXD_EN/(LCD_DATA8-B)*1
71	D8	PE7/D15[A15/D15]/MTIOC6A/GTIOC3A-E/TOC1/MMC_RES#-B/SDHI_WP-B/IRQ7/AN105	PE7/D15[A15/D15]/MTIOC6A/TOC1/MISOB-B/MMC_RES#-B/SDHI_WP-B/IRQ7/AN105/(D7[A7/D7]/LCD_DATA9-B)*1
72	D7	PE6/D14[A14/D14]/MTIOC6C/GTIOC3B-E/TIC1/MMC_CD-B/SDHI_CD-B/IRQ6/AN104	PE6/D14[A14/D14]/MTIOC6C/TIC1/MOSIB-B/MMC_CD-B/SDHI_CD-B/IRQ6/AN104/(D6[A6/D6]/SDHI_CD/LCD_DATA10-B)*1
73	C9	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/GTIOC0A-A/ET0_RX_CLK/REF50CK0/IRQ5/AN103	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/ET0_RX_CLK/REF50CK0/RSPCKB-B/IRQ5/AN103/(D5[A5/D5]/LCD_DATA11-B)*1
74	C10	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/GTIOC1A-A/PO28/ET0_ERXD2/AN102	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/PO28/ET0_ERXD2/SSLB0-B/AN102/(D4[A4/D4]/LCD_DATA12-B)*1

100-Pin LFQFP	100-Pin TFLGA	RX64M	RX65N
75	B10	PE3/D11[A11/D11]/MTIOC4B/GTIOC2A-A/PO26/POE8#/TOC3/CTS12#/RTS12#/SS12#/ET0_ERXD3/MMC_D7-B/AN101	PE3/D11[A11/D11]/MTIOC4B/PO26/POE8#/TOC3/CTS12#/RTS12#/SS12#/ET0_ERXD3/MMC_D7-B/AN101/(D3[A3/D3]/LCD_DATA13-B)*1
76	A10	PE2/D10[A10/D10]/MTIOC4A/GTIOC0B-A/PO23/TIC3/RXD12/SMISO12/SSCL12/RXDX12/MMC_D6-B/IRQ7-DS/AN100	PE2/D10[A10/D10]/MTIOC4A/PO23/TIC3/RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B/MMC_D6-B/IRQ7-DS/AN100/(D2[A2/D2]/LCD_DATA14-B)*1
77	A9	PE1/D9[A9/D9]/MTIOC4C/MTIOC3B/GTIOC1B-A/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/MMC_D5-B/ANEX1	PE1/D9[A9/D9]/MTIOC4C/MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2-B/MMC_D5-B/ANEX1/(D1[A1/D1]/LCD_DATA15-B)*1
78	A8	PE0/D8[A8/D8]/MTIOC3D/GTIOC2B-A/SCK12/MMC_D4-B/ANEX0	PE0/D8[A8/D8]/MTIOC3D/SCK12/SSLB1-B/MMC_D4-B/ANEX0/(D0[A0/D0]/LCD_DATA16-B)*1
79	B9	PD7/D7[A7/D7]/MTIC5U/POE0#/MMC_D1-B/SDHI_D1-B/QIO1-B/QMI-B/IRQ7/AN107	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3/MMC_D1-B/SDHI_D1-B/QIO1-B/QMI-B/IRQ7/AN107/(SSLC3-A/LCD_DATA17-B)*1
80	B8	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/MMC_D0-B/SDHI_D0-B/QIO0-B/QMO-B/IRQ6/AN106	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/SSLC2/MMC_D0-B/SDHI_D0-B/QIO0-B/QMO-B/IRQ6/AN106/(SSLC2-A/LCD_DATA18-B)*1
81	C8	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/MMC_CLK-B/SDHI_CLK-B/QSPCLK-B/IRQ5/AN113	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/SSLC1/MMC_CLK-B/SDHI_CLK-B/QSPCLK-B/IRQ5/AN113/(SSLC1-A/LCD_DATA19-B)*1
82	A7	PD4/D4[A4/D4]/MTIOC8B/POE11#/MMC_CMD-B/SDHI_CMD-B/QSSL-B/IRQ4/AN112	PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0/MMC_CMD-B/SDHI_CMD-B/QSSL-B/IRQ4/AN112/(SSLC0-A/LCD_DATA20-B)*1
83	B7	PD3/D3[A3/D3]/MTIOC8D/GTIOC0A-E/POE8#/TOC2/MMC_D3-B/SDHI_D3-B/QIO3-B/IRQ3/AN111	PD3/D3[A3/D3]/MTIOC8D/POE8#/TOC2/RSPCKC/MMC_D3-B/SDHI_D3-B/QIO3-B/IRQ3/AN111/(RSPCKC-A/LCD_DATA21-B)*1
84	C7	PD2/D2[A2/D2]/MTIOC4D/GTIOC0B-E/TIC2/CRX0/MMC_D2-B/SDHI_D2-B/QIO2-B/IRQ2/AN110	PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0/MISOC/MMC_D2-B/SDHI_D2-B/QIO2-B/IRQ2/AN110/(MISOC-A/LCD_DATA22-B)*1
85	B6	PD1/D1[A1/D1]/MTIOC4B/GTIOC1A-E/POE0#/CTX0/IRQ1/AN109	PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0/MOSIC/IRQ1/AN109/(MOSIC-A/LCD_DATA23-B)*1
86	A6	PD0/D0[A0/D0]/GTIOC1B-E/POE4#/IRQ0/AN108	PD0/D0[A0/D0]/POE4#/IRQ0/AN108/(LCD_EXTCLK-B)*1
87	C6	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
88	D6	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
89	D5	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
90	B5	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004

100-Pin LFQFP	100-Pin TFLGA	RX64M	RX65N
91	A5	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
92	C5	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
93	E5	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
94	A4	VREFL0	VREFL0
95	B4	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
96	C4	VREFH0	VREFH0
97	B3	AVCC0	AVCC0
98	A3	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#
99	B2	AVSS0	AVSS0
100	A1	P05/IRQ13/DA1	P05/IRQ13/DA1

*1: Can be used for products with at least 1.5 Mbytes of code flash memory.

3.3 176/177-Pin Package

Table 3.3 lists the pin functions on products with the 176/176-pin package.

Table 3.3 Comparison of Pin Functions on 176/177-Pin Package Products

176-Pin LFQFP	176/177 -Pin TFLGA LFBGA	RX64M	RX65N (Code flash more than 1.5 MB)
1	A1	AVSS0	AVSS0
2	B1	P05/ IRQ13/ DA1	P05/ IRQ13/ DA1
3	C2	AVCC1	AVCC1
4	D3	P03/ IRQ11/ DA0	P03/ IRQ11/ DA0
5	C1	AVSS1	AVSS1
6	D2	P02/ TMCI1/ SCK6/ IRQ10/ AN120	P02/ TMCI1/ SCK6/ IRQ10/ AN120
7	D1	P01/ TMCI0/ RXD6/ SMISO6/ SSCL6/ IRQ9/ AN119	P01/ TMCI0/ RXD6/ SMISO6/ SSCL6/ IRQ9/ AN119
8	D4	P00/ TMRI0/ TXD6/ SMOSI6/ SSDA6/ IRQ8/ AN118	P00/ TMRI0/ TXD6/ SMOSI6/ SSDA6/ IRQ8/ AN118
9	E3	PF5/ IRQ4	PF5/ IRQ4
10	E2	EMLE	EMLE
11	E1	PJ5/ POE8#/ CTS2#/ RTS2#/ SS2#	PJ5/ POE8#/ CTS2#/ RTS2#/ SS2#
12	A7	VSS	VSS
13	F3	PJ3/ EDACK1/ MTIOC3C/ ET0_EXOUT/ CTS6#/ RTS6#/ CTS0#/ RTS0#/ SS6#/ SS0#	PJ3/ EDACK1/ MTIOC3C/ ET0_EXOUT/ CTS6#/ RTS6#/ SS6#/ CTS0#/ RTS0#/ SS0#
14	F2	VCL	VCL
15	F1	VBATT	VBATT
16	-	NC	NC
17	G4	TRST#/ PF4	TRST#/ PF4
18	G3	MD/ FINED	MD/ FINED
19	G1	XCIN	XCIN
20	G2	XCOUT	XCOUT
21	H3	RES#	RES#
22	H1	XTAL/ P37	XTAL/ P37
23	B12	VSS	VSS
24	J1	EXTAL/ P36	EXTAL/ P36
25	A6	VCC	VCC
26	H4	UPSEL/ P35/ NMI	UPSEL/ P35
27	J3	P34/ MTIOC0A/ TMCI3/ PO12/ POE10#/ SCK6/ SCK0/ ET0_LINKSTA/ IRQ4	P34/ MTIOC0A/ TMCI3/ PO12/ POE10#/ ET0_LINKSTA/ SCK6/ SCK0/ IRQ4
28	K1	P33/ EDREQ1/ MTIOC0D/ TIOCD0/ TMRI3/ PO11/ POE4#/ POE11#/ RXD6/ RXD0/ SMISO6/ SMISO0/ SSCL6/ SSCL0/ CRX0/ PCKO/ IRQ3-DS	P33/ EDREQ1/ MTIOC0D/ TIOCD0/ TMRI3/ PO11/ POE4#/ POE11#/ RXD6/ SMISO6/ SSCL6/ RXD0/ SMISO0/ SSCL0/ CRX0/ PCKO/ IRQ3-DS

176-Pin LFQFP	176/177 -Pin TFLGA LFBGA	RX64M	RX65N (Code flash more than 1.5 MB)
29	K2	P32/ MTIOC0C/ TIOCC0/ TMO3/ PO10/ RTCOUT/ RTCIC2/ POE0#/ POE10#/ TXD6/ TXD0/ SMOSI6/ SMOSI0/ SSDA6/ SSDA0/ CTX0/ USB0_VBUSEN/ VSYNC/ IRQ2-DS	P32/ MTIOC0C/ TIOCC0/ TMO3/ PO10/ RTCIC2/ RTCOUT/ POE0#/ POE10#/ TXD6/ SMOSI6/ SSDA6/ TXD0/ SMOSI0/ SSDA0/ CTX0/ USB0_VBUSEN/ VSYNC/ IRQ2-DS
30	J4	TMS/ PF3	TMS/ PF3
31	K3	TDI/ PF2/ RXD1/ SMISO1/ SSCL1	TDI/ PF2/ RXD1/ SMISO1/ SSCL1
32	L1	P31/ MTIOC4D/ TMCI2/ PO9/ RTCIC1/ CTS1#/ RTS1#/ SS1#/ ET1_MDC/ IRQ1-DS	P31/ MTIOC4D/ TMCI2/ PO9/ RTCIC1/ CTS1#/ RTS1#/ SS1#/ SSLB0-A/ IRQ1-DS
33	L2	P30/ MTIOC4B/ TMRI3/ PO8/ RTCIC0/ POE8#/ RXD1/ SMISO1/ SSCL1/ ET1_MDIO/ IRQ0-DS	P30/ MTIOC4B/ TMRI3/ PO8/ RTCIC0/ POE8#/ RXD1/ SMISO1/ SSCL1/ MISOB-A/ IRQ0-DS
34	K4	TCK/ PF1/ SCK1	TCK/ PF1/ SCK1
35	L3	TDO/ PF0/ TXD1/ SMOSI1/ SSDA1	TDO/ PF0/ TXD1/ SMOSI1/ SSDA1
36	M1	P27/ CS7#/ MTIOC2B/ TMCI3/ PO7/ SCK1/ ET1_WOL	P27/ CS7#/ MTIOC2B/ TMCI3/ PO7/ SCK1/ RSPCKB-A
37	M2	P26/ CS6#/ MTIOC2A/ TMO1/ PO6/ TXD1/ CTS3#/ RTS3#/ SMOSI1/ SS3#/ SSDA1/ ET1_EXOUT	P26/ CS6#/ MTIOC2A/ TMO1/ PO6/ TXD1/ SMOSI1/ SSDA1/ CTS3#/ RTS3#/ SS3#/ MOSIB-A
38	L4	P25/ CS5#/ EDACK1/ MTIOC4C/ MTCLKB/ TIOCA4/ PO5/ RXD3/ SMISO3/ SSCL3/ SSIDATA1/ HSYNC/ ADTRG0#	P25/ CS5#/ EDACK1/ MTIOC4C/ MTCLKB/ TIOCA4/ PO5/ RXD3/ SMISO3/ SSCL3/ SDHI_CD/ HSYNC/ ADTRG0#
39	A9	VCC	VCC
40	M3	P24/ CS4#/ EDREQ1/ MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/ PO4/ SCK3/ USB0_VBUSEN/ SSISCK1/ PIXCLK	P24/ CS4#/ EDREQ1/ MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/ PO4/ SCK3/ USB0_VBUSEN/ SDHI_WP/ PIXCLK
41	C14	VSS	VSS
42	N2	P23/ EDACK0/ MTIOC3D/ MTCLKD/ GTIOC0A-B/ TIOCD3/ PO3/ TXD3/ CTS0#/ RTS0#/ SMOSI3/ SS0#/ SSDA3/ SSISCK0/ PIXD7	P23/ EDACK0/ MTIOC3D/ MTCLKD/ TIOCD3/ PO3/ TXD3/ SMOSI3/ SSDA3/ CTS0#/ RTS0#/ SS0#/ SDHI_D1-C/ PIXD7
43	N3	P22/ EDREQ0/ MTIOC3B/ MTCLKC/ GTIOC1A-B/ TIOCC3/ TMO0/ PO2/ SCK0/ USB0_OVRCURB/ USBA_OVRCURB/ AUDIO_MCLK/ PIXD6	P22/ EDREQ0/ MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/ PO2/ SCK0/ USB0_OVRCURB/ SDHI_D0-C/ PIXD6
44	R1	P21/ MTIOC1B/ MTIOC4A/ GTIOC2A-B/ TIOCA3/ TMCI0/ PO1/ RXD0/ SMISO0/ SSCL0/ USB0_EXICEN/ USBA_EXICEN/ SSIWS0/ PIXD5/ IRQ9	P21/ MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/ PO1/ RXD0/ SMISO0/ SSCL0/ SCL1/ USB0_EXICEN/ SDHI_CLKC/ PIXD5/ IRQ9

176-Pin LFQFP	176/177 -Pin TFLGA LFBGA	RX64M	RX65N (Code flash more than 1.5 MB)
45	R2	P20/ MTIOC1A/ TIOCB3/ TMRI0/ PO0/ TXD0/ SMOSI0/ SSDA0/ USB0_ID/ USBA_ID/ SSIRXD0/ PIXD4/ IRQ8	P20/ MTIOC1A/ TIOCB3/ TMRI0/ PO0/ TXD0/ SMOSI0/ SSDA0/ SDA1/ USB0_ID/ SDHI_CMD-C/ PIXD4/ IRQ8
46	P2	P17/ MTIOC3A/ MTIOC3B/ MTIOC4B/ GTIOC0B-B/ TIOCB0/ TCLKD/ TMO1/ PO15/ POE8#/ SCK1/ TXD3/ SMOSI3/ SSDA3/ SDA2-DS/ SSITXD0/ PIXD3/ IRQ7/ ADTRG1#	P17/ MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/ TMO1/ PO15/ POE8#/ SCK1/ TXD3/ SMOSI3/ SSDA3/ SDA2-DS/ SDHI_D3-C/ PIXD3/ IRQ7/ ADTRG1#
47	P3	P87/ MTIOC4C/ GTIOC1B-B/ TIOCA2/ TXD10/ PIXD2	P87/ MTIOC4C/ TIOCA2/ SMOSI10/ SSDA10/ TXD10/ SDHI_D2-C/ PIXD2
48	R3	P16/ MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/ TMO2/ PO14/ RTCOUT/ TXD1/ RXD3/ SMOSI1/ SMISO3/ SSDA1/ SSCL3/ SCL2-DS/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB/ IRQ6/ ADTRG0#	P16/ MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/ TMO2/ PO14/ RTCOUT/ TXD1/ SMOSI1/ SSDA1/ RXD3/ SMISO3/ SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCURB/ IRQ6/ ADTRG0#
49	M4	P86/ MTIOC4D/ GTIOC2B-B/ TIOCA0/ RXD10/ PIXD1	P86/ MTIOC4D/ TIOCA0/ SMISO10/ SSCL10/ RXD10/ PIXD1
50	N4	P15/ MTIOC0B/ MTCLKB/ GTETRG-B/ TIOCB2/ TCLKB/ TMCI2/ PO13/ RXD1/ SCK3/ SMISO1/ SSCL1/ CRX1-DS/ USBA_VBUSEN/ SSIWS1/ PIXD0/ IRQ5	P15/ MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/ TMCI2/ PO13/ RXD1/ SMISO1/ SSCL1/ SCK3/ CRX1-DS/ PIXD0/ IRQ5
51	P4	P14/ MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/ TMRI2/ PO15/ CTS1#/ RTS1#/ SS1#/ CTX1/ USB0_OVRCURA/ IRQ4	P14/ MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/ TMRI2/ PO15/ CTS1#/ RTS1#/ SS1#/ CTX1/ USB0_OVRCURA/ LCD_CLK-A/ IRQ4
52	R4	P13/ WR2#/ BC2#/ MTIOC0B/ TIOCA5/ TMO3/ PO13/ TXD2/ SMOSI2/ SSDA2/ SDA0[FM+]/ IRQ3/ ADTRG1#	P13/ WR2#/ BC2#/ MTIOC0B/ TIOCA5/ TMO3/ PO13/ TXD2/ SMOSI2/ SSDA2/ SDA0[FM+]/ LCD_TCON0-A/ IRQ3/ ADTRG1#
53	N5	P12/ WR3#/ BC3#/ MTIC5U/ TMCI1/ RXD2/ SMISO2/ SSCL2/ SCL0[FM+]/ IRQ2	P12/ WR3#/ BC3#/ MTIC5U/ TMCI1/ RXD2/ SMISO2/ SSCL2/ SCL0[FM+]/ LCD_TCON1-A/ IRQ2
54	M5/P6	VCC_USB	VCC_USB
55	R5	USB0_DM	USB0_DM
56	P5/R6	USB0_DP	USB0_DP
57	N6/P5	VSS_USB	VSS_USB
58	M6/M5	AVCC_USBA	PJ2/ TXD8/ SMOSI8/ SSDA8/ SSLC3-B/ LCD_TCON2-A
59	M7/M6	USBA_RREF	PJ1/ MTIOC6A/ RXD8/ SMISO8/ SSCL8/ SSLC2-B/ LCD_TCON3-A
60	P6/N6	AVSS_USBA	PJ0/ MTIOC6B/ SCK8/ SSLC1-B/ LCD_DATA0-A

176-Pin LFQFP	176/177 -Pin TFLGA LFBGA	RX64M	RX65N (Code flash more than 1.5 MB)
61	R6/M7	PVSS_USBA	P85/ MTIOC6C/ TIOCC0/ LCD_DATA1-A
62	N7	VSS2_USBA	P84/ MTIOC6D/ LCD_DATA2-A
63	P7	USBA_DM	P57/ RXD7/ SMISO7/ SSCL7/ SSLC0-B/ LCD_DATA3-A
64	R7	USBA_DP	P56/ EDACK1/ MTIOC3C/ TIOCA1/ SCK7/ RSPCKC-B/ LCD_DATA4-A
65	N8/M8	VSS1_USBA	P55/ D0[A0/D0]/ EDREQ0/ MTIOC4D/ TMO3/ ET0_EXOUT/ TXD7/ SMOSI7/ SSDA7/ MISOC-B/ CRX1/ LCD_DATA5-A/ IRQ10
66	M8/N8	VCC_USBA	P54/ D1[A1/D1]/ EDACK0/ MTIOC4B/ TMCI1/ ET0_LINKSTA/ CTS2#/ RTS2#/ SS2#/ MOSIC-B/ CTX1/ LCD_DATA6-A
67	R8	P11/ MTIC5V/ TMCI3/ SCK2/ USBA_VBUS/ USBA_VBUSEN/ IRQ1	P11/ MTIC5V/ TMCI3/ SCK2/ LCD_DATA7-A/ IRQ1
68	P8	P10/ ALE/ MTIC5W/ TMRI3/ USBA_OVRCURA/ IRQ0	P10/ ALE/ MTIC5W/ TMRI3/ IRQ0
69	R9	P53/ BCLK	P53/ BCLK
70	P9	P52/ RD#/ RXD2/ SMISO2/ SSCL2	P52/ RD#/ RXD2/ SMISO2/ SSCL2/ SSLB3-A
71	N9	P51/ WR1#/ BC1#/ WAIT#/ SCK2	P51/ WR1#/ BC1#/ WAIT#/ SCK2/ SSLB2-A
72	M9	P50/ WR0#/ WR#/ TXD2/ SMOSI2/ SSDA2	P50/ WR0#/ WR#/ TXD2/ SMOSI2/ SSDA2/ SSLB1-A
73	D8	VSS	VSS
74	P10	P83/ EDACK1/ MTIOC4C/ GTIOC0A-D/ CTS10#/ ET0_CRS/ RMII0_CRS_DV/ SCK10	P83/ EDACK1/ MTIOC4C/ ET0_CRS/ RMII0_CRS_DV/ SCK10/ SS10#/ CTS10#/ LCD_DATA8-A
75	C11	VCC	VCC
76	N10	UB/ PC7/ A23/ CS0#/ MTIOC3A/ MTCLKB/ GTIOC3A-D/ TMO2/ TOC0/ PO31/ CACREF/ TXD8/ MISOA-A/ ET0_COL/ MMC_D7-A/ IRQ14	UB/ PC7/ A23/ CS0#/ MTIOC3A/ MTCLKB/ TMO2/ PO31/ TOC0/ CACREF/ ET0_COL/ TXD8/ SMOSI8/ SSDA8/ SMOSI10/ SSDA10/ TXD10/ MISOA-A/ MMC_D7-A/ LCD_DATA9-A/ IRQ14
77	P11	PC6/ A22/ CS1#/ MTIOC3C/ MTCLKA/ GTIOC3B-D/ TMCI2/ TIC0/ PO30/ RXD8/ MOSIA-A/ ET0_ETXD3/ MMC_D6-A/ IRQ13	PC6/ D2[A2/D2]/ A22/ CS1#/ MTIOC3C/ MTCLKA/ TMCI2/ PO30/ TIC0/ ET0_ETXD3/ RXD8/ SMISO8/ SSCL8/ SMISO10/ SSCL10/ RXD10/ MOSIA-A/ MMC_D6-A/ LCD_DATA10-A/ IRQ13

176-Pin LFQFP	176/177 -Pin TFLGA LFBGA	RX64M	RX65N (Code flash more than 1.5 MB)
78	M10	PC5/ A21/ CS2#/ WAIT#/ MTIOC3B/ MTCLKD/ GTIOC1A-D/ TMRI2/ PO29/ SCK8/ RSPCKA-A/ RTS8#/ ET0_ETXD2/ MMC_D5-A	PC5/ D3[A3/D3]/ A21/ CS2#/ WAIT#/ MTIOC3B/ MTCLKD/ TMRI2/ PO29/ ET0_ETXD2/ SCK8/ SCK10/ RSPCKA-A/ MMC_D5-A/ LCD_DATA11-A
79	N11	P82/ EDREQ1/ MTIOC4A/ GTIOC2A-D/ PO28/ TXD10/ ET0_ETXD1/ RMII0_TXD1/ MMC_D4-A	P82/ EDREQ1/ MTIOC4A/ PO28/ ET0_ETXD1/ RMII0_TXD1/ SMOSI10/ SSDA10/ TXD10/ MMC_D4-A/ LCD_DATA12-A
80	M11	P81/ EDACK0/ MTIOC3D/ GTIOC0B-D/ PO27/ RXD10/ ET0_ETXD0/ RMII0_TXD0/ MMC_D3-A/ SDHI_CDA/ QIO3-A	P81/ EDACK0/ MTIOC3D/ PO27/ ET0_ETXD0/ RMII0_TXD0/ SMISO10/ SSCL10/ RXD10/ QIO3-A/ SDHI_CD/ MMC_D3-A/ LCD_DATA13-A
81	R12	P80/ EDREQ0/ MTIOC3B/ PO26/ SCK10/ RTS10#/ ET0_TX_EN/ RMII0_TXD_EN/ MMC_D2-A/ SDHI_WP-A/ QIO2-A	P80/ EDREQ0/ MTIOC3B/ PO26/ ET0_TX_EN/ RMII0_TXD_EN/ SCK10/ RTS10#/ QIO2-A/ SDHI_WP/ MMC_D2-A/ LCD_DATA14-A
82	P12	PC4/ A20/ CS3#/ MTIOC3D/ MTCLKC/ GTETRG-D/ TMCI1/ PO25/ POE0#/ SCK5/ CTS8#/ SSLA0-A/ ET0_TX_CLK/ MMC_D1-A/ SDHI_D1-A/ QIO1-A/ QMI-A	PC4/ A20/ CS3#/ MTIOC3D/ MTCLKC/ TMCI1/ PO25/ POE0#/ ET0_TX_CLK/ SCK5/ CTS8#/ RTS8#/ SS8#/ SS10#/ CTS10#/ RTS10#/ SSLA0-A/ QMI-A/ QIO1-A/ SDHI_D1-A/ SDSI_D1-A/ MMC_D1-A/ LCD_DATA15-A
83	N12	PC3/ A19/ MTIOC4D/ GTIOC1B-D/ TCLKB/ PO24/ TXD5/ SMOSI5/ SSDA5/ ET0_TX_ER/ MMC_D0-A/ SDHI_D0-A/ QIO0-A/ QMO-A	PC3/ A19/ MTIOC4D/ TCLKB/ PO24/ ET0_TX_ER/ TXD5/ SMOSI5/ SSDA5/ QMO-A/ QIO0-A/ SDHI_D0-A/ SDSI_D0-A/ MMC_D0-A/ LCD_DATA16-A
84	M12	P77/ CS7#/ PO23/ TXD11/ ET0_RX_ER/ RMII0_RX_ER/ MMC_CLK-A/ SDHI_CLK-A/ QSPCLK-A	P77/ CS7#/ PO23/ ET0_RX_ER/ RMII0_RX_ER/ SMOSI11/ SSDA11/ TXD11/ QSPCLK-A/ SDHI_CLKA/ SDSI_CLKA/ MMC_CLKA/ LCD_DATA17-A
85	R13	P76/ CS6#/ PO22/ RXD11/ ET0_RX_CLK/ REF50CK0/ MMC_CMD-A/ SDHI_CMD-A/ QSSL-A	P76/ CS6#/ PO22/ ET0_RX_CLK/ REF50CK0/ SMISO11/ SSCL11/ RXD11/ QSSL-A/ SDHI_CMD-A/ SDSI_CMDA/ MMC_CMD-A/ LCD_DATA18-A
86	P13	PC2/ A18/ MTIOC4B/ GTIOC2B-D/ TCLKA/ PO21/ RXD5/ SMISO5/ SSCL5/ SSLA3-A/ ET0_RX_DV/ MMC_CD-A/ SDHI_D3-A	PC2/ A18/ MTIOC4B/ TCLKA/ PO21/ ET0_RX_DV/ RXD5/ SMISO5/ SSCL5/ SSLA3-A/ SDHI_D3-A/ SDSI_D3-A/ MMC_CD-A/ LCD_DATA19-A

176-Pin LFQFP	176/177 -Pin TFLGA LFBGA	RX64M	RX65N (Code flash more than 1.5 MB)
87	P14	P75/ CS5#/ PO20/ SCK11/ RTS11#/ ET0_ERXD0/ RMII0_RXD0/ MMC_RES#-A/ SDHI_D2-A	P75/ CS5#/ PO20/ ET0_ERXD0/ RMII0_RXD0/ SCK11/ RTS11#/ SDHI_D2-A/ SDSI_D2-A/ MMC_RES#-A/ LCD_DATA20-A
88	R14	P74/ A20/ CS4#/ PO19/ CTS11#/ ET0_ERXD1/ RMII0_RXD1	P74/ A20/ CS4#/ PO19/ ET0_ERXD1/ RMII0_RXD1/ SS11#/ CTS11#/ LCD_DATA21-A
89	R15	PC1/ A17/ MTIOC3A/ TCLKD/ PO18/ SCK5/ SSLA2-A/ ET0_ERXD2/ IRQ12	PC1/ A17/ MTIOC3A/ TCLKD/ PO18/ ET0_ERXD2/ SCK5/ SSLA2-A/ LCD_DATA22-A/ IRQ12
90	D13	VCC	VCC
91	N13	PC0/ A16/ MTIOC3C/ TCLKC/ PO17/ CTS5#/ RTS5#/ SS5#/ SSLA1-A/ ET0_ERXD3/ IRQ14	PC0/ A16/ MTIOC3C/ TCLKC/ PO17/ ET0_ERXD3/ CTS5#/ RTS5#/ SS5#/ SSLA1-A/ IRQ14
92	E4	VSS	VSS
93	N14	P73/ CS3#/ PO16/ ET0_WOL	P73/ CS3#/ PO16/ ET0_WOL/ LCD_EXTCLK-A
94	M13	PB7/ A15/ MTIOC3B/ TIOCB5/ PO31/ TXD9/ ET0_CRS/ RMII0_CRS_DV	PB7/ A15/ MTIOC3B/ TIOCB5/ PO31/ ET0_CRS/ RMII0_CRS_DV/ TXD9/ SMOSI9/ SSDA9/ SMOSI11/ SSDA11/ TXD11/ SDSI_D1-B
95	L12	PB6/ A14/ MTIOC3D/ TIOCA5/ PO30/ RXD9/ ET0_ETXD1/ RMII0_TXD1	PB6/ A14/ MTIOC3D/ TIOCA5/ PO30/ ET0_ETXD1/ RMII0_TXD1/ RXD9/ SMISO9/ SSCL9/ SMISO11/ SSCL11/ RXD11/ SDSI_D0-B
96	M14	PB5/ A13/ MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/ PO29/ POE4#/ SCK9/ RTS9#/ ET0_ETXD0/ RMII0_TXD0	PB5/ A13/ MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/ PO29/ POE4#/ ET0_ETXD0/ RMII0_TXD0/ SCK9/ SCK11/ SDSI_CLKB/ LCD_CLK-B
97	M15	PB4/ A12/ TIOCA4/ PO28/ CTS9#/ ET0_TX_EN/ RMII0_TXD_EN	PB4/ A12/ TIOCA4/ PO28/ ET0_TX_EN/ RMII0_TXD_EN/ CTS9#/ RTS9#/ SS9#/ SS11#/ CTS11#/ RTS11#/ SDSI_CMDB/ LCD_TCON0-B
98	L13	PB3/ A11/ MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/ TMO0/ PO27/ POE11# / SCK4/ SCK6/ ET0_RX_ER/ RMII0_RX_ER	PB3/ A11/ MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/ TMO0/ PO27/ POE11#/ ET0_RX_ER/ RMII0_RX_ER/ SCK4/ SCK6/ SDSI_D3-B/ LCD_TCON1-B
99	K12	PB2/ A10/ TIOCC3/ TCLKC/ PO26/ CTS4#/ RTS4#/ CTS6#/ RTS6#/ SS4#/ SS6#/ ET0_RX_CLK/ REF50CK0	PB2/ A10/ TIOCC3/ TCLKC/ PO26/ ET0_RX_CLK/ REF50CK0/ CTS4#/ RTS4#/ SS4#/ CTS6#/ RTS6#/ SS6#/ SDSI_D2-B/ LCD_TCON2-B

176-Pin LFQFP	176/177 -Pin TFLGA LFBGA	RX64M	RX65N (Code flash more than 1.5 MB)
100	L14	PB1/ A9/ MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/ PO25/ TXD4/ TXD6/ SMOSI4/ SMOSI6/ SSDA4/ SSDA6/ ET0_ERXD0/ RMII0_RXD0/ IRQ4-DS	PB1/ A9/ MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/ PO25/ ET0_ERXD0/ RMII0_RXD0/ TXD4/ SMOSI4/ SSDA4/ TXD6/ SMOSI6/ SSDA6/ LCD_TCON3-B/ IRQ4-DS
101	L15	P72/ A19/ CS2#/ ET0_MDC	P72/ A19/ CS2#/ ET0_MDC/ LCD_DATA23-A
102	K13	P71/ A18/ CS1#/ ET0_MDIO	P71/ A18/ CS1#/ ET0_MDIO
103	G15	VCC	VCC
104	K15	PB0/ A8/ MTIC5W/ TIOCA3/ PO24/ RXD4/ RXD6/ SMISO4/ SMISO6/ SSCL4/ SSCL6/ ET0_ERXD1/ RMII0_RXD1/ IRQ12	PB0/ A8/ MTIC5W/ TIOCA3/ PO24/ ET0_ERXD1/ RMII0_RXD1/ RXD4/ SMISO4/ SSCL4/ RXD6/ SMISO6/ SSCL6/ LCD_DATA0-B/ IRQ12
105	F15	VSS	VSS
106	J14	PA7/ A7/ TIOCB2/ PO23/ MISOA-B/ ET0_WOL	PA7/ A7/ TIOCB2/ PO23/ ET0_WOL/ MISOA-B/ LCD_DATA1-B
107	J15	PA6/ A6/ MTIC5V/ MTCLKB/ GTETRG-C/ TIOCA2/ TMCI3/ PO22/ POE10#/ CTS5#/ RTS5#/ SS5#/ MOSIA-B/ ET0_EXOUT	PA6/ A6/ MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/ PO22/ POE10#/ ET0_EXOUT/ CTS5#/ RTS5#/ SS5#/ MOSIA-B/ LCD_DATA2-B
108	J12	PA5/ A5/ MTIOC6B/ GTIOC0A-C/ TIOCB1/ PO21/ RSPCKA-B/ ET0_LINKSTA	PA5/ A5/ MTIOC6B/ TIOCB1/ PO21/ ET0_LINKSTA/ RSPCKA-B/ LCD_DATA3-B
109	H12	PA4/ A4/ MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/ PO20/ TXD5/ SMOSI5/ SSDA5/ SSLA0-B/ ET0_MDC/ IRQ5-DS	PA4/ A4/ MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/ PO20/ ET0_MDC/ TXD5/ SMOSI5/ SSDA5/ SSLA0-B/ LCD_DATA4-B/ IRQ5-DS
110	H13	PA3/ A3/ MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/ PO19/ RXD5/ SMISO5/ SSCL5/ ET0_MDIO/ IRQ6-DS	PA3/ A3/ MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/ PO19/ ET0_MDIO/ RXD5/ SMISO5/ SSCL5/ LCD_DATA5-B/ IRQ6-DS
111	H15	TRDATA3/ PG7/ D31/ ET1_TX_ER	TRDATA3/ PG7/ D31
112	H14	PA2/ A2/ MTIOC7A/ GTIOC1A-C/ PO18/ RXD5/ SMISO5/ SSCL5/ SSLA3-B	PA2/ A2/ MTIOC7A/ PO18/ RXD5/ SMISO5/ SSCL5/ SSLA3-B/ LCD_DATA6-B
113	G13	TRDATA2/ PG6/ D30/ ET1_ETXD3	TRDATA2/ PG6/ D30
114	G14	PA1/ A1/ DQM3/ MTIOC0B/ MTCLKC/ MTIOC7B/ GTIOC2A-C/ TIOCB0/ PO17/ SCK5/ SSLA2-B/ ET0_WOL/ IRQ11	PA1/ DQM3/ A1/ MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/ PO17/ ET0_WOL/ SCK5/ SSLA2-B/ LCD_DATA7-B/ IRQ11
115	J2	VCC	VCC
116	G12	TRCLK/ PG5/ D29/ ET1_ETXD2	TRCLK/ PG5/ D29
117	H2	VSS	VSS

176-Pin LFQFP	176/177 -Pin TFLGA LFBGA	RX64M	RX65N (Code flash more than 1.5 MB)
118	F14	PA0/ A0/ BC0#/ DQM2/ MTIOC4A/ MTIOC6D/ GTIOC0B-C/ TIOCA0/ CACREF/ PO16/ SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN	PA0/ DQM2/ BC0#/ A0/ MTIOC4A/ MTIOC6D/ TIOCA0/ PO16/ CACREF/ ET0_TX_EN/ RMII0_TXD_EN/ SSLA1-B/ LCD_DATA8-B
119	F13	TRSYNC/ PG4/ D28/ ET1_ETXD1/ RMII1_TXD1	TRSYNC/ PG4/ D28
120	E15	P67/ CS7#/ DQM1/ MTIOC7C/ GTIOC1B-C/ CRX2/ IRQ15	P67/ DQM1/ CS7#/ MTIOC7C/ IRQ15
121	E14	TRDATA1/ PG3/ D27/ ET1_ETXD0/ RMII1_TXD0	TRDATA1/ PG3/ D27
122	F12	P66/ CS6#/ DQM0/ MTIOC7D/ GTIOC2B-C/ CTX2	P66/ DQM0/ CS6#/ MTIOC7D
123	E13	TRDATA0/ PG2/ D26/ ET1_TX_CLK	TRDATA0/ PG2/ D26
124	D15	P65/ CS5#/ CKE	P65/ CKE/ CS5#
125	D14	PE7/ D15[A15/D15]/ MTIOC6A/ GTIOC3A-E/ TOC1/ MMC_RES#-B/ SDHI_WP-B/ IRQ7/ AN105	PE7/ D15[A15/D15]/ D7[A7/D7]/ MTIOC6A/ TOC1/ MISOB-B/ SDHI_WP/ MMC_RES#-B/ LCD_DATA9-B/ IRQ7/ AN105
126	E12	PE6/ D14[A14/D14]/ MTIOC6C/ GTIOC3B-E/ TIC1/ MMC_CD-B/ SDHI_CD-B/ IRQ6/ AN104	PE6/ D14[A14/D14]/ D6[A6/D6]/ MTIOC6C/ TIC1/ MOSIB-B/ SDHI_CD/ MMC_CD-B/ LCD_DATA10-B/ IRQ6/ AN104
127	K14	VCC	VCC
128	C15	P70/ SDCLK	P70/ SDCLK
129	J13	VSS	VSS
130	D12	PE5/ D13[A13/D13]/ MTIOC4C/ MTIOC2B/ GTIOC0A-A/ ET0_RX_CLK/ REF50CK0/ IRQ5/ AN103	PE5/ D13[A13/D13]/ D5[A5/D5]/ MTIOC4C/ MTIOC2B/ ET0_RX_CLK/ REF50CK0/ RSPCKB-B/ LCD_DATA11-B/ IRQ5/ AN103
131	C13	PE4/ D12[A12/D12]/ MTIOC4D/ MTIOC1A/ GTIOC1A-A/ PO28/ ET0_ERXD2/ AN102	PE4/ D12[A12/D12]/ D4[A4/D4]/ MTIOC4D/ MTIOC1A/ PO28/ ET0_ERXD2/ SSLB0-B/ LCD_DATA12-B/ AN102
132	B15	PE3/ D11[A11/D11]/ MTIOC4B/ GTIOC2A-A/ PO26/ POE8#/ TOC3/ CTS12#/ RTS12#/ SS12#/ ET0_ERXD3/ MMC_D7-B/ AN101	PE3/ D11[A11/D11]/ D3[A3/D3]/ MTIOC4B/ PO26/ TOC3/ POE8#/ ET0_ERXD3/ CTS12#/ RTS12#/ SS12#/ MMC_D7-B/ LCD_DATA13-B/ AN101
133	A15	PE2/ D10[A10/D10]/ MTIOC4A/ GTIOC0B-A/ PO23/ TIC3/ RXD12/ SMISO12/ SSCL12/ RXDX12/ MMC_D6-B/ IRQ7-DS/ AN100	PE2/ D10[A10/D10]/ D2[A2/D2]/ MTIOC4A/ PO23/ TIC3/ RXD12/ SMISO12/ SSCL12/ RXDX12/ SSLB3-B/ MMC_D6-B/ LCD_DATA14-B/ IRQ7-DS/ AN100

176-Pin LFQFP	176/177 -Pin TFLGA LFBGA	RX64M	RX65N (Code flash more than 1.5 MB)
134	A14	PE1/ D9[A9/D9]/ MTIOC4C/ MTIOC3B/ GTIOC1B-A/ PO18/ TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12/ MMC_D5-B/ ANEX1	PE1/ D9[A9/D9]/ D1[A1/D1]/ MTIOC4C/ MTIOC3B/ PO18/ TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12/ SSLB2-B/ MMC_D5-B/ LCD_DATA15-B/ ANEX1
135	B14	PE0/ D8[A8/D8]/ MTIOC3D/ GTIOC2B-A/ SCK12/ MMC_D4-B/ ANEX0	PE0/ D8[A8/D8]/ D0[A0/D0]/ MTIOC3D/ SCK12/ SSLB1-B/ MMC_D4-B/ LCD_DATA16-B/ ANEX0
136	B13	P64/ CS4#/ WE#	P64/ WE#/ D3[A3/D3]/ CS4#
137	A13	P63/ CS3#/ CAS#	P63/ CAS#/ D2[A2/D2]/ CS3#
138	C12	P62/ CS2#/ RAS#	P62/ RAS#/ D1[A1/D1]/ CS2#
139	D11	P61/ CS1#/ SDCS#	P61/ SDCS#/ D0[A0/D0]/ CS1#
140	N15	VSS	VSS
141	A12	P60/ CS0#/ ET1_TX_EN/ RMII1_TXD_EN	P60/ CS0#
142	N1	VCC	VCC
143	D10	PD7/ D7[A7/D7]/ MTIC5U/ POE0#/ MMC_D1-B/ SDHI_D1-B/ QIO1-B/ QMI-B/ IRQ7/ AN107	PD7/ D7[A7/D7]/ MTIC5U/ POE0#/ SSLC3-A/ QMI-B/ QIO1-B/ SDHI_D1-B/ MMC_D1-B/ LCD_DATA17-B/ IRQ7/ AN107
144	B11	PG1/ D25/ ET1_RX_ER/ RMII1_RX_ER	TRDATA7/ PG1/ D25
145	A11	PD6/ D6[A6/D6]/ MTIC5V/ MTIOC8A/ POE4#/ MMC_D0-B/ SDHI_D0-B/ QIO0-B/ QMO-B/ IRQ6/ AN106	PD6/ D6[A6/D6]/ MTIC5V/ MTIOC8A/ POE4#/ SSLC2-A/ QMO-B/ QIO0-B/ SDHI_D0-B/ MMC_D0-B/ LCD_DATA18-B/ IRQ6/ AN106
146	C10	PG0/ D24/ ET1_RX_CLK/ REF50CK1	TRDATA6/ PG0/ D24
147	D9	PD5/ D5[A5/D5]/ MTIC5W/ MTIOC8C/ POE10#/ MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B/ IRQ5/ AN113	PD5/ D5[A5/D5]/ MTIC5W/ MTIOC8C/ POE10#/ SSLC1-A/ QSPCLK-B/ SDHI_CLKB/ MMC_CLKB/ LCD_DATA19-B/ IRQ5/ AN113
148	B10	PD4/ D4[A4/D4]/ MTIOC8B/ POE11#/ MMC_CMD-B/ SDHI_CMD-B/ QSSLB/ IRQ4/ AN112	PD4/ D4[A4/D4]/ MTIOC8B/ POE11#/ SSLC0-A/ QSSL-B/ SDHI_CMD-B/ MMC_CMD-B/ LCD_DATA20-B/ IRQ4/ AN112
149	A10	P97/ A23/ D23/ ET1_ERXD3	TRSYNC1/ P97/ D23/ A23
150	C9	PD3/ D3[A3/D3]/ MTIOC8D/ GTIOC0A-E/ POE8#/ TOC2/ MMC_D3-B/ SDHI_D3-B/ QIO3-B/ IRQ3/ AN111	PD3/ D3[A3/D3]/ MTIOC8D/ TOC2/ POE8#/ RSPCKC-A/ QIO3-B/ SDHI_D3-B/ MMC_D3-B/ LCD_DATA21-B/ IRQ3/ AN111
151	P1	VSS	VSS
152	B9	P96/ A22/ D22/ ET1_ERXD2	TRDATA5/ P96/ D22/ A22
153	P15	VCC	VCC

176-Pin LFQFP	176/177-Pin TFLGA LFBGA	RX64M	RX65N (Code flash more than 1.5 MB)
154	C8	PD2/ D2[A2/D2]/ MTIOC4D/ GTIOC0B-E/ TIC2/ CRX0/ MMC_D2-B/ SDHI_D2-B/ QIO2_B/ IRQ2/ AN110	PD2/ D2[A2/D2]/ MTIOC4D/ TIC2/ MISOC-A/ CRX0/ QIO2-B/ SDHI_D2-B/ MMC_D2-B/ LCD_DATA22-B/ IRQ2/ AN110
155	D7	P95/ A21/ D21/ ET1_ERXD1/ RMII1_RXD1	TRDATA4/ P95/ D21/ A21
156	B8	PD1/ D1[A1/D1]/ MTIOC4B/ GTIOC1A-E/ POE0#/ CTX0/ IRQ1/ AN109	PD1/ D1[A1/D1]/ MTIOC4B/ POE0#/ MOSIC-A/ CTX0/ LCD_DATA23-B/ IRQ1/ AN109
157	A8	P94/ A20/ D20/ ET1_ERXD0/ RMII1_RXD0	P94/ D20/ A20
158	C7	PD0/ D0[A0/D0]/ GTIOC1B-E/ POE4#/ IRQ0/ AN108	PD0/ D0[A0/D0]/ POE4#/ LCD_EXTCLK-B/ IRQ0/ AN108
159	D6	P93/ A19/ D19/ POE0#/ ET1_LINKSTA/ CTS7#/ RTS7#/ SS7#/ AN117	P93/ D19/ A19/ POE0#/ CTS7#/ RTS7#/ SS7#/ AN117
160	B7	P92/ A18/ D18/ POE4#/ ET1_CRS/ RMII1_CRS_DV/ RXD7/ SMISO7/ SSCL7/ AN116	P92/ D18/ A18/ POE4#/ RXD7/ SMISO7/ SSCL7/ AN116
161	B6	P91/ A17/ D17/ ET1_COL/ SCK7/ AN115	P91/ D17/ A17/ SCK7/ AN115
162	R10	VSS	VSS
163	C6	P90/ A16/ D16/ ET1_RX_DV/ TXD7/ SMOSI7/ SSDA7/ AN114	P90/ D16/ A16/ TXD7/ SMOSI7/ SSDA7/ AN114
164	R11	VCC	VCC
165	B5	P47/ IRQ15-DS/ AN007	P47/ IRQ15-DS/ AN007
166	A5	P46/ IRQ14-DS/ AN006	P46/ IRQ14-DS/ AN006
167	C5	P45/ IRQ13-DS/ AN005	P45/ IRQ13-DS/ AN005
168	D5	P44/ IRQ12-DS/ AN004	P44/ IRQ12-DS/ AN004
169	C4	P43/ IRQ11-DS/ AN003	P43/ IRQ11-DS/ AN003
170	A4	P42/ IRQ10-DS/ AN002	P42/ IRQ10-DS/ AN002
171	B4	P41/ IRQ9-DS/ AN001	P41/ IRQ9-DS/ AN001
172	A3	VREFL0	VREFL0
173	B3	P40/ IRQ8-DS/ AN000	P40/ IRQ8-DS/ AN000
174	C3	VREFH0	VREFH0
175	A2	AVCC0	AVCC0
176	B2	P07/ IRQ15/ ADTRG0#	P07/ IRQ15/ ADTRG0#
-	F4	BSCANP	BSCANP

4. Notes on Migration

4.1 Notes on Pin Design

4.1.1 VCL Pin (External Capacitor)

Connect a decoupling capacitor rated at 0.22 μF to the VCL pin of the RX65N Group for stabilization of the internal power supply.

4.1.2 Serial Communication Interface RTS9# Pin

The RTS9# pin of the serial communication interface is assigned to PB5 on the RX64M Group and to PB4 on the RX65N Group. Bear this in mind when making settings.

4.2 Notes on Function Settings

4.2.1 Setting Number of Flash Memory Access Wait States

On the RX65N Group it is necessary to specify the number of access wait states to be used when accessing the flash memory, based on the system clock (ICLK) frequency of the microcontroller. This setting is made to the ROMWT register.

The number of flash memory access wait states, according to ICLK frequency, is listed below.

Table 4.1 Flash Memory Access Wait States by ICLK Frequency

	ICLK ≤ 50 MHz	50 MHz < ICLK ≤ 100 MHz	100 MHz < ICLK ≤ 120 MHz
Wait states	0 to 2	1 or 2	2

Note: For details on external connection circuits, see RX65N Group, RX651 Group User's Manual: Hardware, listed in section 5, Reference Documents.

4.2.2 User Boot Mode

UB code A, UB code B, and user boot mode are implemented on the RX64M Group but not on the RX65N Group.

When using the startup program protection function on the RX65N Group, it is possible to use any interface to program and erase the user area in flash memory as an alternative to user boot mode. For details, see 7.3.1, Startup Program Protection Function, in RX65N Group, RX651 Group Flash Memory User's Manual: Hardware Interface, cited in 5, Reference Documents.

4.2.3 Transferring Firmware to FCU RAM

On the RX64M Group it was necessary to store the FCU firmware in the FCU RAM, but on the RX65N Group this step is not necessary.

4.2.4 Flash Access Window Setting Register (FAW)

On the RX65N Group, once the access window protect bit (FSPR) in the flash access window setting register (FAW) is cleared to 0, it cannot be reset to 1.

For details, see RX65N Group, RX651 Group User's Manual: Hardware, cited in 5, Reference Documents.

5. Reference Documents

User's Manual: Hardware

RX64M Group, User's Manual: Hardware Rev.1.10 (R01UH0377EJ0110)
(The latest version can be downloaded from the Renesas Electronics website.)

RX65N Group, RX651 Group User's Manual: Hardware Rev.2.10 (R01UH0590EJ0210)
(The latest version can be downloaded from the Renesas Electronics website.)

RX65N Group, RX651 Group Flash Memory User's Manual: Hardware Interface Rev.1.00 (R01UH0602EJ0100)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest version can be downloaded from the Renesas Electronics website.)

Consistency with Technical Updates

This application note reflects the contents of the following technical updates:

- TN-RX*-A127A/J
- TN-RX*-A122A/J
- TN-RX*-A119A/J

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Nov. 30, 2015	—	First edition issued
0.50	Mar. 18, 2016		Revisions accompanying update of User's Manual: Hardware from revision 0.4 to 0.5
		5	(1) Boot mode (FINE interface) added
		14	(2) Content of CPU bus and memory bus items changed due to deletion of AFU
		17	(3) IR2C bit in DTC mode register A deleted
		33	(4) Specifications for 16-bit data size deleted
		38	(5) Ring buffer deleted from compare function
		40	(6) Due to change in number of channels in A/D sampling state register n (ADSSTRn), item deleted from points of difference from RX64M
			(7) Due to change in symbol names of A/D compare function window A extended input select register (ADCMPANSER), item deleted from points of difference from RX64M
		41	(8) Due to change in symbol names of A/D compare function window A extended input compare condition setting register (ADCMPLER), item deleted from points of difference from RX64M
			(9) Due to deletion of A/D data storage buffer register n (ADBUFn), A/D data storage buffer enable register (ADBUFEN), and A/D data storage buffer pointer register (ADBUFPTR), items deleted from points of difference from RX64M
		42	(10) Temperature calibration data register (TSCDR) added
		45	(11) Content of cache and read cycle items changed due to deletion of AFU
		46	(12) Boot mode (FINE interface) added to onboard programming item
		47	(13) Unique ID register n (UIDRn) added
			Other revisions
		18	(14) Errors related to event link setting register (ELSEn) of RX65N corrected
		22	(15) Errors in communication speed item corrected
		33	(16) Errors in 32-bit polynomial expression corrected
		42	(17) Deleted temperature sensor correction register because it not implemented on RX64M
		47	(18) Deleted peripheral clock notification register because it not implemented on RX64M
0.51	May 31, 2016	3	(1) USB 2.0 FS Host/Function module (USBb) in table 1.1 amended to "differences exist"
		4	(2) Temperature sensor in table 1.1 amended to "function implemented"
			(3) Meanings of symbols in table 1.1 amended
		16	(4) BSIZE bit added to CSn control register (CSnCR)
			(5) BSIZE bit added to SDC control register (SDCCR)
			(6) BPHB bit added to bus priority control register (BUSPRI)
		19	(7) Value of n in event link setting register n (ELSRn) amended
		22	(8) MTU/GPT pin function select register (MGSEL) added
		24	(9) FIFO depth register (FDR) added

Rev.	Date	Description Page	Summary
0.51	May 31, 2016		(10) RFDO bit added to flow control start FIFO threshold setting register (FCFTR)
		25	(11) PHY crosspoint adjustment register (PHYSLEW) added
		34	(12) MODF bit added to RSPI status register (SPSR)
		37	(13) CLKSEL bit added to SDHI clock control register (SDCLKCR)
		42	(14) Unit 0 of A/D channel select register A0 (ADANSA0) amended
		42	(15) Unit 1 of A/D channel select register A0 (ADANSA0) added
			(16) A/D channel select register A1 (ADANSA1) added
			(17) Unit 0 of A/D channel select register B0 (ADANSB0) amended
			(18) Unit 1 of A/D channel select register B0 (ADANSB0) added
			(19) A/D channel select register B1 (ADANSB1) added
		43	(20) Unit 0 of A/D-converted value addition/average mode select register 0 (ADADS0) amended
			(21) Unit 1 of A/D-converted value addition/average mode select register 0 (ADADS0) added
			(22) A/D-converted value addition/average mode select register 1 (ADADS1) added
			(23) Details of ADC bit in A/D-converted value addition/average count select register (ADADC) added
		44	(24) A/D compare function window A channel select register 0 (ADCMPANSR0) amended
			(25) Channel 0 of A/D compare function window A compare condition setting register 0 (ADCMPLR0) amended
			(26) Channel 1 of A/D compare function window A compare condition setting register 0 (ADCMPLR0) added
			(27) A/D compare function window A compare condition setting register 1 (ADCMPLR1) added
			(28) Channel 0 of A/D compare function window A channel status register 0 (ADCMPSR0) amended
			(29) Channel 1 of A/D compare function window A channel status register 0 (ADCMPSR0) added
			(30) A/D compare function window A channel status register 1 (ADCMPSR1) amended
		49	(19) Unique ID item amended
		50	(20) FLWE bit added to flash P/E protect register (FWEPROR)
			(21) ECRCT bit added to flash access status register (FASTAT)
			(22) FRDY bit added to flash status register (FSTATR)
			(23) SUINIT bit added to flash sequencer setting initialization register (FSUINITR)
0.80	Jul. 29, 2016	1	(1) Summary amended
		3, 12	(2) Interrupt control abbreviation changed
		3	(3) I/O port changed to “differences exist”
		4	(4) 12-bit D/A converter changed to “differences exist”
		6	(5) ROM code protection register (ROMCODE) added
		13	(6) RAM error interrupt added
		14	(7) RAM error interrupt status flag (RAMST) added
			(8) RAM error interrupt enable bit (RAMEN) added
			(9) Range of k for selectable interrupt A request register k (PIARk) changed

Rev.	Date	Description	
		Page	Summary
0.80	Jul. 29, 2016	15	(10) SDSI added to peripheral modules connected to internal main bus 2 of RX65N
		16	(11) SDSI added to details of bus master code bits
		18	(12) Read skip, write-back skip, and sequence transfer sections changed
			(13) Displacement addition item added
			(14) Name of write-back disable bit changed
		21	(15) Drive capacity control register 2 (DSCR2) added
			(16) ADRHMS bit deleted from external bus control register 0 (PFBCR0)
		25	(17) Address error flag (ADE) and address error interrupt enable bit (ADEIP) added
			(18) Receive request reset bit (RNC) deleted from RX65N
		30	(19) Item names related to FIFO changed
		35	(20) RSPI data register (SPDR) added
			(21) RSPI byte access setting bit (SPBYT) added
		40	(22) PCLKB:ADCLK frequency ratio changed in A/D conversion clock item
			(23) Japanese notation in sections changed
		40 to 42, 46	(24) A/D successive approximation time setting register (ADSAM) and A/D successive approximation time setting protection cancel register (ADSAMPR) added
			(25) D/A output disable register (DAODISR) added
			(26) RX65N register bit (FLWE) name changed
			(27) Comparison tables amended
		51	(28) Table number added (table 4.1)
		53 to 60	(29) Sections 4.2.2 and 4.2.3 added
		67	(30) Reference documents amended
		68	(31) Technical update numbers added
1.00	Oct. 1, 2016	4	(1) In Table 1.1, 12-bit D/A converter amended to “function implemented”
		5	(2) MDSR register name amended
		20	(3) Module name amended
			(4) Item section changed (target pins to be placed in high-impedance state → pins subject to high-impedance control)
			(5) Item section changed (conditions for high-impedance state → high-impedance request issuance conditions)
			(6) Details of high-impedance request issuance conditions partially amended for RX65N
		21	(7) Module name amended
		28	(8) Item added to Table 2.32 (data match detection)
		30	(9) Note added to Table 2.35
		34	(10) SSL control function errors corrected
		35	(11) Description of mode fault error flag (MODF) in RSPI status register partially amended for RX65N
		36	(12) Details of CRC data input register (CRCDIR) and CRC data output register (CRCDOR) amended
		41	(13) RX65N conversion time indicated
		51	(14) RX65N portion of program/erasure method section partially amended
			(15) RX65N portion of trusted memory function section amended
			(16) Details of other functions partially amended and added

Rev.	Date	Description	
		Page	Summary
1.00	Oct. 1, 2016	52	(17) Item names amended (off programming → programming/erasure using dedicated parallel programmer)
		64	(18) PB5 pin name on RX64M amended
		67	(19) 4.2.2, User Boot Mode, added
2.00	Nov. 06, 2017	All pages	Supports RX65N with at least 1.5 Mbytes of code flash memory
2.10	Nov. 27, 2018	All pages	Confirmed the contents of the description again (Addition of description mistake etc.)

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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