RX130 Group, RX220 Group

Points of Difference Between RX130 Group and RX220 Group

Introduction

This application note is intended mainly as a reference for confirming the points of difference between the outlines of the peripheral functions, the I/O registers, and the pin functions of the RX130 Group and RX220 Group, and it also includes notes on migration between the two groups.

Unless otherwise indicated, the information listed in this application note applies to 100-pin product versions of RX220 Group MCUs and to 100-pin product versions of RX130 Group MCUs. For details of differences regarding electrical characteristics, important notes, setting procedures, etc., refer to the user's manual of the specific product.

Target Devices

RX220 Group and RX130 Group

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1. Comparison of Functions of RX130 Group and RX220 Group

A comparison of the functions of the RX130 Group and RX220 Group is provided below. For details of the functions, see 2. Comparative Overview of Functions, and 5, Reference Documents.

Table 1.1 is a comparative listing of the functions of the RX130 and RX220.

Table 1.1 Comparison of Functions of RX130 and RX220

Function	RX220	RX130
CPU	○	○
Operating mode	△	△
Address Space	△	△
Reset	○	○
Option-setting memory	△	△
Voltage detection circuit (LVDAa): RX220, (LVDAb): RX130	△	△
Clock generation circuit	△	△
Clock frequency accuracy measurement circuit (CAC)	△	△
Low power consumption function	△	△
Register write protection function	△	△
Exception Handling	○	○
Interrupt controller (ICUb)	△	△
Buses	△	△
DMA controller (DMACA)	○	×
Data transfer controller (DTCa)	○	○
Event link controller (ELC)	△	△
I/O port	△	△
Multi-function pin controller (MPC)	△	△
Multi-function timer pulse unit 2 (MTU2a)	○	○
Port output enable 2 (POE2a)	○	○
8-bit timer (TMR)	○	○
Compare match timer (CMT)	△	△
Realtime clock (RTCc)	○	○
Low-power timer (LPT)	×	○
Independent watchdog timer (IWDTa)	△	△
Serial communications interface (SCIe, SCIf): RX220, (SCIg, SCIh): RX130	△	△
IrDA interface	○	×
I²C bus interface (RIIC): RX220, (RIICa): RX130	△	△
Serial peripheral interface (RSPI): RX220, (RSPIa): RX130	△	△
CRC calculator (CRC)	○	○
Capacitive touch sensing unit (CTSUa)	×	○
12-bit A/D converter (S12ADb): RX220, (S12ADE): RX130	△	△
D/A converter (DA)	×	○
Temperature sensor (TEMPSA)	×	○
Comparator A(CMPA) :RX220, Comparator B (CMPBa):RX130	△	△
Data operation circuit (DOC)	○	○
RAM	△	△
Flash memory (ROM)	△	△
Flash memory (E2 Data Flash)	△	△
Package (LFQFP48/64/100 only)	△	△

Note: ○: Function implemented, ×: Function not implemented, △: Differences exist between implementation of function on RX220 and RX130.

2. Comparative Overview of Functions

This section lists points of difference between the peripheral functions of the RX130 and RX220 groups, comparing each function in overview and the registers of each function. Specifications implemented only on one group are shown in red, specifications that exist on both groups but with points of difference are shown in red, and specifications that exist on both groups are shown in black.

2.1 Operating Modes

Table 2.1 shows a comparative listing of the operating modes specifications, and Table 2.2 shows a comparative listing of the operating modes registers.

Table 2.1 Comparative Listing of Operating Modes Specifications

Item	RX220	RX130
Operating mode	Single-chip mode	Single-chip mode
	Boot mode (SCI interface)	Boot mode (SCI interface)
	User boot mode	—
Mode pins	MD, PC7	MD

Table 2.2 Comparative Listing of Operating Mode Registers

Register	Bit	RX220	RX130
MDSR	—	Mode status register	—

2.2 Address Space

Figure 2.1 shows the comparative of memory maps.

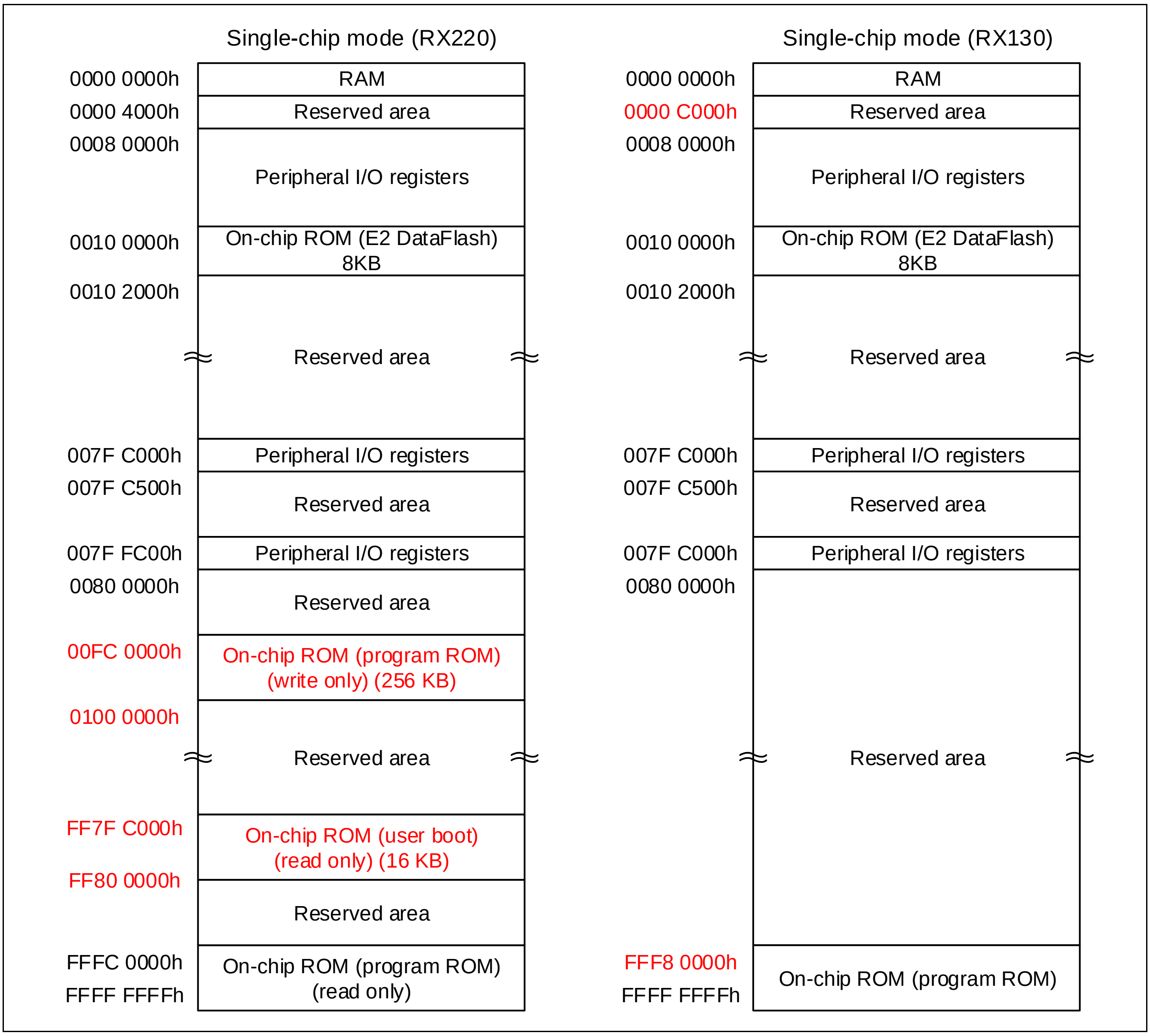
Single-chip mode (RX220)
0000 0000h
RAM
0000 4000h
Reserved area
0008 0000h
Peripheral I/O registers
0010 0000h
On-chip ROM (E2 DataFlash) 8KB
0010 2000h
Reserved area
007F C000h
Peripheral I/O registers
007F C500h
Reserved area
007F FC00h
Peripheral I/O registers
0080 0000h
Reserved area
00FC 0000h
On-chip ROM (program ROM) (write only) (256 KB)
0100 0000h
Reserved area
FF7F C000h
On-chip ROM (user boot) (read only) (16 KB)
FF80 0000h
Reserved area
FFFC 0000h
On-chip ROM (program ROM) (read only)
FFFF FFFFh
Single-chip mode (RX130)
0000 0000h
RAM
0000 C000h
Reserved area
0008 0000h
Peripheral I/O registers
0010 0000h
On-chip ROM (E2 DataFlash) 8KB
0010 2000h
Reserved area
007F C000h
Peripheral I/O registers
007F C500h
Reserved area
007F C000h
Peripheral I/O registers
0080 0000h
Reserved area
FFF8 0000h
On-chip ROM (program ROM)
FFFF FFFFh

Figure 2.1 Comparative of Memory Map

2.3 Option-Setting Memory

Table 2.3 shows a comparative listing of the option-setting memory specifications, and Table 2.4 shows a comparative listing of the option-setting memory registers, and Figure 2.2 shows a comparative of the option-setting memory.

Table 2.3 Comparative Listing of Option-Setting Memory Specifications

Item	RX220	RX130
Related to user boot mode	UB code A UB code B Endian select register B (MDEB)	—
Related to single-chip mode	Endian select register S (MDES)	Endian select register (MDE)

Table 2.4 Comparative Listing of Option-Setting Memory Registers

Register	Bit	RX220	RX130
OFS0	IWDTTOPS [1:0]	IWDT timeout period select bits b3 b2 0 0: 1,024 cycles (03FFh) 0 1: 4,096 cycles (0FFFh) 1 0: 8,192 cycles (1FFFh) 1 1: 16,384 cycles (3FFFh)	IWDT timeout period select bits b3 b2 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1,024 cycles (03FFh) 1 1: 2,048 cycles (07FFh)
	IWDTSLCSTP	IWDT Sleep Mode Count Stop Control 0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby, or all-module clock stop mode	IWDT Sleep Mode Count Stop Control 0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby, or deep sleep mode
OFS1	VDSEL [1:0]	Voltage detection 0 level select bits b1 b0 0 0: 3.80 V is selected 0 1: 2.80 V is selected 1 0: 1.90 V is selected 1 1: 1.72 V is selected	Voltage detection 0 level select bits b1 b0 0 0: 3.84 V is selected 0 1: 2.82 V is selected 1 0: 2.51 V is selected 1 1: 1.90 V is selected
	FASTSTUP	—	Power-on fast startup time bit
MDEB	—	Endian select register B	—
MDES	—	Endian select register S	—
MDE	—	—	Endian select register

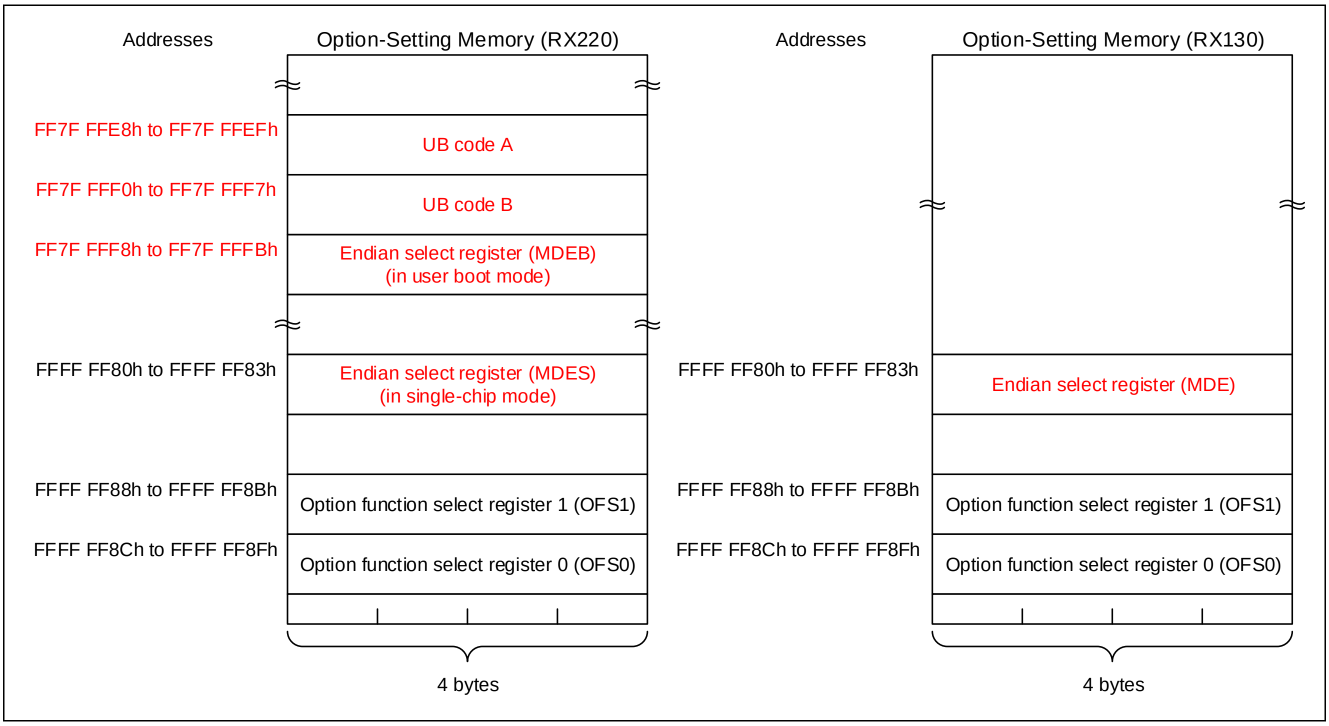
Addresses
Option-Setting Memory (RX220)
FF7F FFE8h to FF7F FFEFh
UB code A
FF7F FFF0h to FF7F FFF7h
UB code B
FF7F FFF8h to FF7F FFFBh
Endian select register (MDEB) (in user boot mode)
FFFF FF80h to FFFF FF83h
Endian select register (MDES) (in single-chip mode)
FFFF FF88h to FFFF FF8Bh
Option function select register 1 (OFS1)
FFFF FF8Ch to FFFF FF8Fh
Option function select register 0 (OFS0)
4 bytes
Addresses
Option-Setting Memory (RX130)
FFFF FF80h to FFFF FF83h
Endian select register (MDE)
FFFF FF88h to FFFF FF8Bh
Option function select register 1 (OFS1)
FFFF FF8Ch to FFFF FF8Fh
Option function select register 0 (OFS0)
4 bytes

Figure 2.2 Comparative of Option-Setting Memory

2.4 Voltage Detection Circuit

Table 2.5 shows a comparative listing of the voltage detection circuit specifications, and Table 2.6 shows a comparative listing of the voltage detection circuit registers.

Table 2.5 Comparative Listing of Voltage Detection Circuit Specifications

		RX220 (LVDAa)			RX130 (LVDAb)		
Item		**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detection target	Voltage falls lower than Vdet0.	Voltage rises or falls past Vdet1.	Voltage rises or falls past Vdet2.	Voltage falls lower than Vdet0.	Voltage rises or falls past Vdet1.	Voltage rises or falls past Vdet2.
				The EXVCCINP2 bit in LVCMPCR can be used to select between VCC and the voltage input to the CMPA2 pin.			The EXVCCINP2 bit in LVCMPCR can be used to select between VCC and the voltage input to the CMPA2 pin.
	Detection voltage	Selectable from four levels using OFS1.VDSEL [1:0] bits.	Selectable from 16 levels using LVDLVLR.LVD1LVL[3:0] bits	Differs depending on whether VCC or CMPA2 pin input voltage is selected. Selectable from 16 levels using LVDLVLR.LVD2LVL[3:0] bits	Selectable from four levels using OFS1.VDSEL [1:0] bits.	Selectable from 14 levels using LVDLVLR.LVD1LVL[3:0] bits.	Selectable from four levels using LVDLVLR.LVD2LVL[1:0] bits.
	Monitor flag	—	LVD1SR.LVD1MON flag: Monitors if higher or lower than Vdet1.	LVD2SR.LVD2MON flag: Monitors if higher or lower than Vdet2.	—	LVD1SR.LVD1MON flag: Monitors if higher or lower than Vdet1.	LVD2SR.LVD2MON flag: Monitors if higher or lower than Vdet2.
			LVD1SR.LVD1DET flag: Detects rise or fall past Vdet1.	LVD2SR.LVD2DET flag: Detects rise or fall past Vdet2.		LVD1SR.LVD1DET flag: Detects rise or fall past Vdet1.	LVD2SR.LVD2DET flag: Detects rise or fall past Vdet2.
Voltage detection processing	Reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet0 > VCC: CPU operation restarts a fixed period of time after VCC > Vdet0.	Reset when Vdet1 > VCC: Selectable between CPU operation restarts a fixed period of time after VCC > Vdet1 and CPU operation restarts a fixed period of time after Vdet1 > VCC.	Reset when Vdet2 > VCC: Selectable between CPU operation restarts a fixed period of time after VCC > Vdet2 and CPU operation restarts a fixed period of time after Vdet2 > VCC.	Reset when Vdet0 > VCC: CPU operation restarts a fixed period of time after VCC > Vdet0.	Reset when Vdet1 > VCC: Selectable between CPU operation restarts a fixed period of time after VCC > Vdet1 and CPU operation restarts a fixed period of time after Vdet1 > VCC.	Reset when Vdet2 > VCC or CMPA2 pin voltage: Selectable between CPU operation restarts a fixed period of time after VCC or CMPA2 pin voltage > Vdet2 and CPU operation restarts a fixed period of time after Vdet2 > VCC or CMPA2 pin voltage.

Item		RX220 (LVDAa)			RX130 (LVDAb)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
Voltage detection processing	Interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
			Selectable between non-maskable interrupt and interrupt.	Selectable between non-maskable interrupt and interrupt.		Selectable between non-maskable interrupt and interrupt.	Selectable between non-maskable interrupt and interrupt.
			Interrupt request generated both when Vdet1 > VCC and when VCC > Vdet1, or one or the other.	Interrupt request generated both when Vdet2 > VCC and when VCC > Vdet2, or one or the other.		Interrupt request generated both when Vdet1 > VCC and when VCC > Vdet1, or one or the other.	Interrupt request generated both when Vdet2 > VCC or CMPA2 pin voltage and when VCC or CMPA2 pin voltage > Vdet2, or one or the other.
Digital filter	Enable/ disable switching	—	Available	Available	—	—	—
	Sampling time	—	1/n LOCO frequency × 2 (n: 1, 2, 4, 8)	1/n LOCO frequency × 2 (n: 1, 2, 4, 8)	—	—	—
Analog filter		—	—	—	Available	Available	Available
Event link function		—	Available: Vdet1 pass-through detection event output	—	—	Available: Vdet1 pass-through detection event output	—

Table 2.6 Comparative Listing of Voltage Detection Circuit Registers

Register	Bit	RX220 (LVDAa)	RX130 (LVDAb)
LVD2CR1	LVD2IDTSEL [1:0]	Voltage monitoring 2/comparator A2 interrupt generation condition select bits b1 b0 0 0: When VCC ≥ Vdet2 (rise) is detected 0 1: When VCC < Vdet2 (drop) is detected 1 0: When drop and rise are detected 1 1: Do not set.	Voltage monitoring 2 interrupt generation condition select bits b1 b0 0 0: When VCC or CMPA2 pin voltage ≥ Vdet2 (rise) is detected 0 1: When VCC or CMPA2 pin voltage < Vdet2 (drop) is detected 1 0: When drop and rise are detected 1 1: Do not set.
LVD2SR	LVD2MON	Voltage monitoring 2/comparator A2 signal monitor flag 0: VCC < Vdet2 1: VCC ≥ Vdet2 or LVD2MON is disabled	Voltage monitoring 2 signal monitor flag 0: VCC or CMPA2 pin voltage < Vdet2 1: VCC or CMPA2 pin voltage ≥ Vdet2 or LVD2MON is disabled
LVCMPCR	EXVREFINP1	Comparator A1 reference voltage external input select bit	—
	EXVCCINP1	Comparator A1 comparison voltage external input select bit	—
	EXVREFINP2	Comparator A2 reference voltage external input select bit	—

Register	Bit	RX220 (LVDAa)	RX130 (LVDAb)
	LVD1E	Voltage Detection 1/Comparator A1 Enable 0: Voltage detection 1/comparator A1 circuit disabled 1: Voltage detection 1/comparator A1 circuit enabled	Voltage Detection 1 Enable 0: Voltage detection 1 circuit disabled 1: Voltage detection 1 circuit enabled
	LVD2E	Voltage Detection 2/Comparator A2 Enable 0: Voltage detection 2/comparator A2 circuit disabled 1: Voltage detection 2/comparator A2 circuit enabled	Voltage Detection 2 Enable 0: Voltage detection 2 circuit disabled 1: Voltage detection 2 circuit enabled
LVDLVLR	LVD1LVL[3:0]	Voltage detection 1 level select bits (standard voltage during drop in voltage) b3 b0 0 0 0 0: 4.15 V 0 0 0 1: 4.00 V 0 0 1 0: 3.85 V 0 0 1 1: 3.70 V 0 1 0 0: 3.55 V 0 1 0 1: 3.40 V 0 1 1 0: 3.25 V 0 1 1 1: 3.10 V 1 0 0 0: 2.95 V 1 0 0 1: 2.80 V 1 0 1 0: 2.65 V 1 0 1 1: 2.50 V 1 1 0 0: 2.35 V 1 1 0 1: 2.20 V 1 1 1 0: 2.05 V 1 1 1 1: 1.90 V	Voltage detection 1 level select bits (standard voltage during drop in voltage) b3 b0 0 0 0 0: 4.29 V 0 0 0 1: 4.14 V 0 0 1 0: 4.02 V 0 0 1 1: 3.84 V 0 1 0 0: 3.10 V 0 1 0 1: 3.00 V 0 1 1 0: 2.90 V 0 1 1 1: 2.79 V 1 0 0 0: 2.68 V 1 0 0 1: 2.58 V 1 0 1 0: 2.48 V 1 0 1 1: 2.20 V 1 1 0 0: 1.96 V 1 1 0 1: 1.86 V Do not set to values other than the above.
	LVD2LVL	Voltage detection 2 level select bits [3:0] (b4 to b7) (standard voltage during drop in voltage) (When LVCMPCR.EXVCCINP2 = 0 (VCC selected)) b7 b4 0 0 0 0: 4.15 V 0 0 0 1: 4.00 V 0 0 1 0: 3.85 V 0 0 1 1: 3.70 V 0 1 0 0: 3.55 V 0 1 0 1: 3.40 V 0 1 1 0: 3.25 V 0 1 1 1: 3.10 V 1 0 0 0: 2.95 V 1 0 0 1: 2.80 V 1 0 1 0: 2.65 V 1 0 1 1: 2.50 V 1 1 0 0: 2.35 V 1 1 0 1: 2.20 V	Voltage detection 2 level select bits [1:0] (b4, b5) (standard voltage during drop in voltage) b5 b4 0 0: 4.29 V 0 1: 4.14 V 1 0: 4.02 V 1 1: 3.84 V

Register	Bit	RX220 (LVDAa)	RX130 (LVDAb)
		1 1 1 0: 2.05 V 1 1 1 1: 1.90 V (When LVCMPCR.EXVCCINP2 = 1 (CMPA2 selected)) b7 b4 0 0 0 1: 1.33 V Do not set to values other than the above.	
LVD1CR0	LVD1DFDIS	Voltage monitoring 1/comparator A1 digital filter disable mode select bit	—
	LVD1FSAMP [1:0]	Sampling clock select bits	—
LVD2CR0	LVD2DFDIS	Voltage monitoring 2/comparator A2 digital filter disable mode select bit	—
	LVD2FSAMP [1:0]	Sampling clock select bits	—

2.5 Clock Generation Circuit

Table 2.7 shows a comparative listing of the clock generation circuit specifications, and Table 2.8 shows a comparative listing of the clock generation circuit registers.

Table 2.7 Comparative Listing of Clock Generation Circuit Specifications

Item	RX220	RX130
Uses	• Generates the system clock (ICLK) supplied to the CPU, DMAC, DTC, ROM, and RAM. • Generates the peripheral module clocks (PCLKB, PCLKD) supplied to the peripheral module clocks. Peripheral module clock PCLKD is used as the operating clock for S12AD, and peripheral module clock PCLKB is used as the operating clock for the modules other than S12AD. • Generates the FlashIF clock (FCLK) supplied to the FlashIF. • Generates the CAC clock (CACCLK) supplied to the CAC. • Generates the RTC-dedicated sub clock (RTCSCLK) supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) supplied to the IWDT.	• Generates the system clock (ICLK) supplied to the CPU, DTC, and RAM. • Generates the peripheral module clocks (PCLKB, PCLKD) supplied to the peripheral module clocks. Peripheral module clock PCLKD is used as the operating clock for S12AD, and peripheral module clock PCLKB is used as the operating clock for the modules other than S12AD. • Generates the FlashIF clock (FCLK) supplied to the FlashIF. • Generates the CAC clock (CACCLK) supplied to the CAC. • Generates the RTC-dedicated sub clock (RTCSCLK) supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) supplied to the IWDT. • Generates the LPT clock (LPTCLK) to be supplied to the LPT. • Generates the REMC clock (REMCLK) to be supplied to the REMC.
Operating frequencies	• ICLK: 32 MHz (max.) • PCLKB: 32 MHz (max.) • PCLKD: 32 MHz (max.) • FCLK: 4 MHz to 32 MHz (for programming and erasing the ROM and E2 data flash) 32 MHz (max.): (for reading from the E2 data flash) • CACCLK: Same frequency as each oscillator • RTCSCLK: 32.768 kHz • IWDTCLK: 125 kHz	• ICLK: 32 MHz (max.) • PCLKB: 32 MHz (max.) • PCLKD: 32 MHz (max.) • FCLK: 1 MHz to 32 MHz (for programming and erasing the ROM and E2 data flash) 32 MHz (max.): (for reading from the E2 data flash) • CACCLK: Same frequency as each oscillator • RTCSCLK: 32.768 kHz • IWDTCLK: 15 kHz • LPTCLK: The same frequency as that of the selected oscillator • REMCLK: Same frequency as each oscillator

Item	RX220	RX130
Main clock oscillator	• Resonator frequency: 1 MHz to 20 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When oscillation stop of the main clock is detected, the system clock source is switched to LOCO, and MTU output can be forcedly driven to high-impedance. • Drive capacity switching function	• Resonator frequency: 1 MHz to 20 MHz (VCC ≥ 2.4 V) 1 MHz to 8 MHz (VCC < 2.4 V) • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When oscillation stop of the main clock is detected, the system clock source is switched to LOCO, and MTU output can be forcedly driven to high-impedance. • Drive capacity switching function
Sub-clock oscillator	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pins: XCIN, XCOUT • Drive capacity switching function	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pins: XCIN, XCOUT • Drive capacity switching function
PLL	—	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 8 MHz • Frequency multiplication ratio: Selectable within range from 4 to 8 (increments of 0.5) • Oscillation frequency: 24 MHz to 32 MHz (VCC ≥ 2.4 V)
High-speed on-chip oscillator (HOCO)	• Oscillation frequency: 32 MHz, 36.864 MHz, 40 MHz, 50 MHz • HOCO power supply control	• Oscillation frequency: 32 MHz
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 125 kHz	Oscillation frequency: 4 MHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 125 kHz	Oscillation frequency: 15 kHz

Table 2.8 Comparative Listing of Clock Generation Circuit Registers

Register	Bit	RX220	RX130
SCKCR	BCK[3:0]	External bus clock (BCLK) select bits	—
SCKCR3	CKSEL[2:0]	Clock source select bits b10 b8 0 0 0: LOCO selected 0 0 1: HOCO selected 0 1 0: Main clock oscillator selected 0 1 1: Sub-clock oscillator selected Do not set to values other than the above.	Clock source select bits b10 b8 0 0 0: LOCO selected 0 0 1: HOCO selected 0 1 0: Main clock oscillator selected 0 1 1: Sub-clock oscillator selected 1 0 0: PLL circuit selected Do not set to values other than the above.
PLLCR	—	—	PLL control register
PLLCR2	—	—	PLL control register 2
HOFCR	—	—	High-Speed On-Chip Oscillator Forced Oscillation Control Register
HOCOCR2	—	High-speed on-chip oscillator control register 2	—
OSCOVFSR	—	—	Oscillation stabilization flag register
MOSCWTCR	MSTS[4:0]	Main clock oscillator wait time setting bits b4 b0 0 0 0 0 0: wait time = 2 cycles 0 0 0 0 1: wait time = 4 cycles 0 0 0 1 0: wait time = 8 cycles 0 0 0 1 1: wait time = 16 cycles 0 0 1 0 0: wait time = 32 cycles 0 0 1 0 1: wait time = 256 cycles 0 0 1 1 0: wait time = 512 cycles 0 0 1 1 1: wait time = 1,024 cycles 0 1 0 0 0: wait time = 2,048 cycles 0 1 0 0 1: wait time = 4,096 cycles 0 1 0 1 0: wait time = 16,384 cycles 0 1 0 1 1: wait time = 32,768 cycles 0 1 1 0 0: wait time = 65,536 cycles 0 1 1 0 1: wait time = 131,072 cycles 0 1 1 1 0: wait time = 262,144 cycles 0 1 1 1 1: wait time = 524,288 cycles Do not set to values other than the above.	Main clock oscillator wait time setting bits b4 b0 0 0 0 0 0: wait time = 2 cycles (0.5 μs) 0 0 0 0 1: wait time = 1,024 cycles (256 μs) 0 0 0 1 0: wait time = 2,048 cycles (512 μs) 0 0 0 1 1: wait time = 4,096 cycles (1.024 ms) 0 0 1 0 0: wait time = 8,192 cycles (2.048 ms) 0 0 1 0 1: wait time = 16,384 cycles (4.096 ms) 0 0 1 1 0: wait time = 32,768 cycles (8.192 ms) 0 0 1 1 1: wait time = 65,536 cycles (16.384 ms) Do not set to values other than the above. Above wait times apply when LOCO = 4.0 MHz (0.25 μs, typ.).
SOSCWTCR	—	Sub-clock oscillator wait control register	—
HOCOWTCR2	—	HOCO wait control register 2	—
CKOCR	—	—	CLKOUT output control register
MOFCR	MODRV21	—	Main clock oscillator drive capability switch bit

Register	Bit	RX220	RX130
	MODRV[2:0]	Main clock oscillator drive capability switch bits	—
	MODRV2 [1:0]	Main clock oscillator drive capability switch 2 bits	—
HOCOPCR	—	High-speed on-chip oscillator power supply control register	—
LOCOTRR	—	—	Low-speed on-chip oscillator trimming register
ILOCOTRR	—	—	IWDT-dedicated on-chip oscillator trimming register
HOCOTRR0	—	—	High-speed on-chip oscillator trimming register 0

2.6 Clock Frequency Accuracy Measurement Circuit

Table 2.9 shows a comparative listing of the clock frequency accuracy measurement circuit specifications, and Table 2.10 shows a comparative listing of the clock frequency accuracy measurement circuit registers.

Table 2.9 Comparative Listing of Low Power Consumption Functions

Item	RX220	RX130
Clock frequency measurement	The frequencies of the following clocks can be measured: • Main clock • Sub-clock • HOCO clock • LOCO clock • IWDTCLK clock	The frequencies of the following clocks can be measured: • Main clock • Sub-clock • HOCO clock • LOCO clock • IWDTCLK clock • Peripheral module clock B (PCLKB)
Measurement reference clocks	• External clock input on CACREF pin • Main clock • Sub-clock • HOCO clock • LOCO clock • IWDTCLK clock	• External clock input on CACREF pin • Main clock • Sub-clock • HOCO clock • LOCO clock • IWDTCLK clock • Peripheral module clock B (PCLKB)
Selectable function	Digital filter function	Digital filter function
Interrupt sources	• Measurement end interrupt • Frequency error interrupt • Overflow interrupt	• Measurement end interrupt • Frequency error interrupt • Overflow interrupt
Low power consumption function	It is possible to specify the module stop state.	It is possible to specify the module stop state.

Table 2.10 Comparative Listing of Low Power Consumption Function Registers

Register	Bit	RX220	RX130
CACR1	FMCS[2:0]	Frequency measurement clock select bits b3 b1 0 0 0: Main clock oscillator output clock 0 0 1: Sub-clock oscillator output clock 0 1 0: High-speed on-chip oscillator output clock 0 1 1: Low-speed on-chip oscillator output clock 1 0 0: IWDT-dedicated on-chip oscillator output clock Do not set to values other than the above.	Measurement target clock select bits b3 b1 0 0 0: Main clock 0 0 1: Sub-clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDTCLK clock 1 0 1: Peripheral module clock B (PCLKB) Do not set to values other than the above.
CACR2	RSCS[2:0]	Reference signal generation clock select bits b3 b1 0 0 0: Main clock oscillator output clock 0 0 1: Sub-clock oscillator output clock 0 1 0: High-speed on-chip oscillator output clock 0 1 1: Low-speed on-chip oscillator output clock 1 0 0: IWDT-dedicated on-chip oscillator output clock Do not set to values other than the above.	Measurement reference clock select bits b3 b1 0 0 0: Main clock 0 0 1: Sub-clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDTCLK clock 1 0 1: Peripheral module clock B (PCLKB) Do not set to values other than the above.

2.7 Low Power Consumption Functions

Table 2.11 shows a comparative listing of the low power consumption specifications, Table 2.12 to Table 2.15 shows a Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode, and Table 2.16 shows a comparative listing of the low power consumption function registers.

Table 2.11 Comparative Listing of Low Power Consumption Functions

Item	RX220	RX130
Reduction of power consumption by clock switching	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKB), S12AD clock (PCLKD), and FlashIF clock (FCLK).	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKB), S12AD clock (PCLKD), and FlashIF clock (FCLK).
Module stop function	Each peripheral module can be stopped independently.	Each peripheral module can be stopped independently.
Function for transition to low power consumption mode	It is possible to transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped.	It is possible to transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped.
Low power consumption modes	• Sleep mode • All-module clock stop mode • Software standby mode	• Sleep mode • Deep sleep mode • Software standby mode
Operating power reduction function	• Power consumption can be reduced in normal operation, sleep mode, and all-module clock stop mode by selecting an appropriate operating power consumption control mode according to the operating frequency and operating voltage. • Operating power control modes: 4 — Middle-speed operating mode 1A — Middle-speed operating mode 1B — Low-speed operating mode 1 — Low-speed operating mode 2	• Power consumption can be reduced in normal operation, sleep mode, and deep sleep mode by selecting an appropriate operating power consumption control mode according to the operating frequency and operating voltage. • Operating power control modes: 3 — High-speed operating mode — Middle-speed operating mode — Low-speed operating mode

Table 2.12 Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode (Sleep Mode)

Entering and Exiting Low Power Consumption Modes and Operating States	RX220	RX130
	Sleep Mode	**Sleep Mode**
Entry trigger	Control register + instruction	Control register + instruction
Exit trigger	Interrupt	Interrupt
After exiting from each mode, CPU begins from	Interrupt handling	Interrupt handling
Main clock oscillator	Operating possible	Operating possible
Sub-clock oscillator	Operating possible	Operating possible
High-speed on-chip oscillator	Operating possible	Operating possible
Low-speed on-chip oscillator	Operating possible	Operating possible
IWDT-dedicated on-chip oscillator	Operating possible	Operating possible
PLL	—	Operating possible
CPU	Stopped (Retained)	Stopped (Retained)
RAM0 (0000 0000h to 0000 BFFFh)	—	Operating possible (Retained)
RAM0 (0000 0000h to 0000 3FFFh)	Operating possible (Retained)	—
DTC	—	Operating possible
Flash memory	Operating	Operating
Independent watchdog timer (IWDT)	Operating possible	Operating possible
Remote control signal receiver (REMC)	—	Operating possible
Realtime clock (RTC)	Operating possible	Operating possible
8-bit timer (unit 0, unit 1) (TMR)	Operating possible	Operating possible
Low power timer (LPT)	—	Operating possible
Voltage detection circuit (LVD)	Operating possible	Operating possible
Power-on reset circuit	Operating	Operating
Peripheral modules	Operating possible	Operating possible
I/O ports	Operating	Operating
RTCOUT	—	Operating possible
CLKOUT	—	Operating possible
Comparator B	—	Operating possible

Table 2.13 Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode (All-Module Clock Stop Mode)

Entering and Exiting Low Power Consumption Modes and Operating States	RX220	RX130
	All-Module Clock Stop Mode	All-Module Clock Stop Mode
Entry trigger	Control register + instruction	—
Exit trigger	Interrupt	—
After exiting from each mode, CPU begins from	Interrupt handling	—
Main clock oscillator	Operating possible	—
Sub-clock oscillator	Operating possible	—
High-speed on-chip oscillator	Operating possible	—
Low-speed on-chip oscillator	Operating possible	—
IWDT-dedicated on-chip oscillator	Operating possible	—
PLL	—	—
CPU	Stopped (Retained)	—
RAM0 (0000 0000h to 0000 BFFFh)	—	—
RAM0 (0000 0000h to 0000 3FFFh)	Stopped (Retained)	—
DTC	—	—
Flash memory	Operating	—
Independent watchdog timer (IWDT)	Operating possible	—
Remote control signal receiver (REMC)	—	—
Realtime clock (RTC)	Operating possible	—
8-bit timer (unit 0, unit 1) (TMR)	Operating possible	—
Low power timer (LPT)	—	—
Voltage detection circuit (LVD)	Operating possible	—
Power-on reset circuit	Operating	—
Peripheral modules	Operating possible	—
I/O ports	Retained	—
RTCOUT	—	—
CLKOUT	—	—
Comparator B	—	—

Table 2.14 Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode (Software Standby Mode)

Entering and Exiting Low Power Consumption Modes and Operating States	RX220	RX130
	Software Standby Mode	Software Standby Mode
Entry trigger	Control register + instruction	Control register + instruction
Exit trigger	Interrupt	Interrupt
After exiting from each mode, CPU begins from	Interrupt handling	Interrupt handling
Main clock oscillator	Stopped	Stopped
Sub-clock oscillator	Operating possible	Operating possible
High-speed on-chip oscillator	Stopped	Operating possible
Low-speed on-chip oscillator	Stopped	Stopped
IWDT-dedicated on-chip oscillator	Operating possible	Operating possible
PLL	—	Stopped
CPU	Stopped (Retained)	Stopped (Retained)
RAM0 (0000 0000h to 0000 BFFFh)	—	Stopped (Retained)
RAM0 (0000 0000h to 0000 3FFFh)	Stopped (Retained)	—
DTC	—	Stopped (Retained)
Flash memory	Stopped (Retained)	Stopped (Retained)
Independent watchdog timer (IWDT)	Operating possible	Operating possible
Remote control signal receiver (REMC)	—	Operating possible
Realtime clock (RTC)	Operating possible	Operating possible
8-bit timer (unit 0, unit 1) (TMR)	Stopped (Retained)	Stopped (Retained)
Low power timer (LPT)	—	Operating possible
Voltage detection circuit (LVD)	Operating possible	Operating possible
Power-on reset circuit	Operating	Operating
Peripheral modules	Stopped (Retained)	Stopped (Retained)
I/O ports	Retained	Retained
RTCOUT	—	Operating possible
CLKOUT	—	Operating possible
Comparator B	—	Operating possible

Table 2.15 Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode (Deep Sleep Mode)

Entering and Exiting Low Power Consumption Modes and Operating States	RX220	RX130
	Deep Sleep Mode	Deep Sleep Mode
Entry trigger	—	Control register + instruction
Exit trigger	—	Interrupt
After exiting from each mode, CPU begins from	—	Interrupt handling
Main clock oscillator	—	Operating possible
Sub-clock oscillator	—	Operating possible
High-speed on-chip oscillator	—	Operating possible
Low-speed on-chip oscillator	—	Operating possible
IWDT-dedicated on-chip oscillator	—	Operating possible
PLL	—	Operating possible
CPU	—	Stopped (Retained)
RAM0 (0000 0000h to 0000 BFFFh)	—	Stopped (Retained)
RAM0 (0000 0000h to 0000 3FFFh)	—	—
DTC	—	Stopped (Retained)
Flash memory	—	Stopped (Retained)
Independent watchdog timer (IWDT)	—	Operating possible
Remote control signal receiver (REMC)	—	Operating possible
Realtime clock (RTC)	—	Operating possible
8-bit timer (unit 0, unit 1) (TMR)	—	Operating possible
Low power timer (LPT)	—	Operating possible
Voltage detection circuit (LVD)	—	Operating possible
Power-on reset circuit	—	Operating
Peripheral modules	—	Operating possible
I/O ports	—	Operating
RTCOUT	—	Operating possible
CLKOUT	—	Operating possible
Comparator B	—	Operating possible

Table 2.16 Comparative Listing of Low Power Consumption Function Registers

Register	Bit	RX220	RX130
SBYCR	(b14)	Reserved bit This bit is read as 1. The write value should be 1.	Reserved bit This bit is read as 0. The write value should be 0.
	SSBY	Software Standby 0: Shifts to sleep mode or all-module clock stop mode after the WAIT instruction is executed 1: Shifts to software standby mode after the WAIT instruction is executed	Software Standby 0: Set entry to sleep mode or deep sleep mode after the WAIT instruction is executed 1: Set entry to software standby mode after the WAIT instruction is executed
MSTPCRA	MSTPA14	Compare match timer (unit 1) module stop setting bit	—
	MSTPA19	—	D/A converter module stop setting bit
	MSTPA24	Module stop A24 setting bit	—
	MSTPA27	Module stop A27 setting bit	—
	MSTPA28	DMA Controller/Data Transfer Controller Module Stop Target module: DMAC/DTC 0: The module stop state is canceled 1: Transition to the module stop state is made	Data Transfer Controller Module Stop Target module: DTC 0: This module clock is enabled 1: This module clock is disabled
	MSTPA29	Module stop A29 setting bit	—
	ACSE	All-module clock stop mode enable bit	—
MSTPCRB	MSTPB10	—	Comparator module stop setting bit
	MSTPB31	—	Target module: SCI0 0: This module clock is enabled 1: This module clock is disabled
MSTPCRC	MSTPC20	IrDA module stop setting bit	—
	MSTPC27	—	Serial Communication Interface 8 Module Stop
	MSTPC28	—	Remote control signal receiver 1 Module Stop
	MSTPC29	—	Remote control signal receiver 0 Module Stop
	DSLPE	—	Deep sleep mode enable bit
MSTPCRD	—	—	Module stop control register D

Register	**Bit**	**RX220**	**RX130**
OPCCR	OPCM[2:0]	Operating power control mode select bits b2 b0 0 1 0: Middle-speed operating mode 1A 0 1 1: Middle-speed operating mode 1B 1 1 0: Low-speed operating mode 1 1 1 1: Low-speed operating mode 2 Do not set to values other than the above.	Operating power control mode select bits b2 b0 0 0 0: High-speed operating mode 0 1 0: Middle-speed operating mode Do not set to values other than the above.
SOPCCR	—	—	Sub-operating power control register
RSTCKCR	RSTCKSEL [2:0]	Sleep mode return clock source select bits b2 b0 0 0 1: HOCO selected 0 1 0: Main clock oscillator selected Settings other than the above are prohibited while the RSTCKEN bit is set to 1.	Sleep mode return clock source select bits b2 b0 0 0 0: LOCO selected 0 0 1: HOCO selected 0 1 0: Main clock oscillator selected Settings other than the above are prohibited while the RSTCKEN bit is set to 1.
FHSSBYCR	—	Flash HOCO software standby control register	—

2.8 Register Write Protection Function

Table 2.17 shows a comparative overview of the register write protection function specifications, and Table 2.18 shows a comparative listing of the register write protection function registers.

Table 2.17 Comparative Overview of Register Write Protection Function

Item	RX220	RX130
PRC0 bit	Registers related to the clock generation circuit SCKCR, SCKCR3, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, HOCOCR2	Registers related to the clock generation circuit SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOFCR, OSTDCR, OSTDSR, CKOCR, LOCOTRR, ILOCOTRR, HOCOTRR0
PRC1 bit	• Registers related to the operating modes SYSCR1 • Registers related to the low power consumption functions SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR, RSTCKCR, MOSCWTCR, SOSCWTCR, FHSSBYCR, HOCOWTCR2 • Registers related to the clock generation circuit MOFCR, HOCOPCR • Software reset register SWRR	• Registers related to the operating modes SYSCR1 • Registers related to the low power consumption functions SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, SOPCCR • Registers related to the clock generation circuit MOFCR, MOSCWTCR • Software reset register SWRR
PRC2 bit	—	Registers related to the low power timer LPTCR1, LPTCR2, LPTCR3, LPTPRD, LPCMR0, LPWUCR
PRC3 bit	Registers related to the LVD LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	Registers related to the LVD LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

Table 2.18 Comparative Listing of Register Write Protection Function Registers

Register	Bit	RX220	RX130
PRCR	PRC1	Protect Bit 1 Enables writing to the registers related to operating modes, low power consumption, and software reset. 0: Write disabled 1: Write enabled	Protect Bit 1 Enables writing to the registers related to operating modes, low power consumption functions, the clock generation circuit, and software reset. 0: Write disabled 1: Write enabled
	PRC2	—	Protect bit 2

2.9 Interrupt Controller

Table 2.19 shows a comparative listing of the interrupt controller specifications, and Table 2.20 shows a comparative listing of the interrupt controller registers.

Table 2.19 Comparative Listing of Interrupt Controller Specifications

Item		RX220 (ICUb)	RX130 (ICUb)
Interrupt	Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection Edge detection or level detection is determined independently for each source of the connected peripheral modules.	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection Edge detection or level detection is determined independently for each source of the connected peripheral modules.
	External pin interrupts	• Interrupts from pins IRQ0 to IRQ7 • Sources: 8 • Interrupt detection: One detection method among low level, falling edge, rising edge, and rising and falling edges can be set for each source. • Digital filter function: Supported	• Interrupts from pins IRQ0 to IRQ7 • Sources: 8 • Interrupt detection: One detection method among low level, falling edge, rising edge, and rising and falling edges can be set for each source. • Digital filter function: Supported
	Software interrupt	• Interrupt generated by writing to a register. • Source: 1	• Interrupt generated by writing to a register. • Source: 1
	Event link interrupt	The ELSR18I interrupt is generated by an ELC event.	The ELSR8I or ELSR18I interrupt is generated by an ELC event.
	Interrupt priority level	Priority is specified by register settings.	Priority is specified by register settings.
	Fast interrupt function	Faster interrupt processing by the CPU can be specified only for a single interrupt source.	Faster interrupt processing by the CPU can be specified only for a single interrupt source.
	DTC control	Interrupt sources can be used to start the DTC and DMAC.	Interrupt sources can be used to start the DTC.
Non-maskable interrupts	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter function: Supported	• Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter function: Supported
	Oscillation stop detection interrupt	Interrupt at oscillation stop detection	Interrupt at oscillation stop detection
	IWDT underflow/refresh error	Interrupt at an underflow of the down counter or at the occurrence of a refresh error	Interrupt at an underflow of the down counter or at the occurrence of a refresh error
	Voltage monitoring 1 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)	Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)

Item	RX220 (ICUb)	RX130 (ICUb)
Return from low power consumption modes	• Sleep mode: Return is initiated by a non-maskable interrupt or any other interrupt source. • All-module clock stop mode: Return is initiated by a non-maskable interrupts, interrupt IRQ0 to IRQ7, TMR interrupt or RTC alarm/period interrupt. • Software standby mode: Return is initiated by a non-maskable interrupt, interrupt IRQ0 to IRQ7, or RTC alarm/period interrupt.	• Sleep mode and deep sleep mode: Return is initiated by a non-maskable interrupt or any other interrupt source. • Software standby mode: Return is initiated by a non-maskable interrupt, interrupt IRQ0 to IRQ7, or RTC alarm/period interrupt.

Table 2.20 Comparative Listing of Interrupt Controller Registers

Register	Bit	RX220 (ICUb)	RX130 (ICUb)
DMRSRm	—	DMAC activation request select register m (m = DMAC channel number)	—
DTCERn	DTCE	DTC Activation Enable 0: DTC activation is disabled 1: DTC activation is enabled	DTC Transfer Request Enable 0: The corresponding interrupt source is not selected as the DTC trigger. 1: The corresponding interrupt source is selected as the DTC trigger.

2.10 Bus

Table 2.21 shows a comparative listing of the bus specifications, and Table 2.22 shows a comparative listing of the bus registers.

Table 2.21 Comparative Listing of Bus Specifications

Item		RX220	RX130
CPU bus	Instruction bus	• Connected to the CPU (for instructions). • Connected to the on-chip memory (RAM and ROM). • Operates in synchronization with the system clock (ICLK).	• Connected to the CPU (for instructions). • Connected to the on-chip memory (RAM and ROM). • Operates in synchronization with the system clock (ICLK).
	Operand bus	• Connected to the CPU (for operand). • Connected to the on-chip memory (RAM and ROM). • Operates in synchronization with the system clock (ICLK).	• Connected to the CPU (for operand). • Connected to the on-chip memory (RAM and ROM). • Operates in synchronization with the system clock (ICLK).
Memory buses	Memory bus 1	Connected to the RAM.	Connected to the RAM.
	Memory bus 2	Connected to the ROM.	Connected to the ROM.
Internal main buses	Internal main bus 1	• Connected to the CPU. • Operates in synchronization with the system clock (ICLK).	• Connected to the CPU. • Operates in synchronization with the system clock (ICLK).
	Internal main bus 2	• Connected to the DMAC and DTC. • Connected to the on-chip memory (RAM and ROM). • Operates in synchronization with the system clock (ICLK).	• Connected to the DTC. • Connected to the on-chip memory (RAM and ROM). • Operates in synchronization with the system clock (ICLK).
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section). • Operates in synchronization with the system clock (ICLK).	• Connected to peripheral modules (DTC, interrupt controller, and bus error monitoring section). • Operates in synchronization with the system clock (ICLK).
	Internal peripheral bus 2	• Connected to peripheral modules (modules other than those connected to internal peripheral bus 1). • Operates in synchronization with the peripheral module clock (PCLKB, PCLKD).	• Connected to peripheral modules. • Operates in synchronization with the peripheral module clock (PCLKB, PCLKD).
	Internal peripheral bus 3	—	• Connected to peripheral modules (Touch). • Operates in synchronization with the peripheral module clock (PCLKB).
	Internal peripheral bus 6	• Connected to the on-chip ROM (P/E) and E2 data flash memory. • Operates in synchronization with the FlashIF clock (FCLK).	• Connected to the on-chip ROM (P/E) and E2 data flash memory. • Operates in synchronization with the FlashIF clock (FCLK).

Table 2.22 Comparative Listing of Bus Registers

Register	Bit	RX220	RX130
BEREN	TOEN	—	Timeout detection enable bit
BERSR1	TO	—	Timeout bit
	MST[2:0]	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC/DMAC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved
BUSPRI	BPGB[1:0]	Internal peripheral bus 2 priority control bits	Internal peripheral bus 2 and 3 priority control bits

2.11 Event Link Controller

Table 2.23 shows a comparative listing of the event link controller specifications, Table 2.24 shows a comparative listing of the event link controller registers, and Table 2.25 shows a comparative listing of ELSRn register setting values.

Table 2.23 Comparative Listing of Bus Specifications

Item	RX220 (ELC)	RX130 (ELC)
Event link function	• 46 event signals can be directly connected to modules. • It is possible to specify that timer modules operate when an event is input. • Event link operation is possible for port B. — Single-port: Event link operation can be enabled for a specified single bit in a port. — Port group: Event link operation can be enabled for a group of specified bits within an 8-bit port.	• 47 event signals can be directly connected to modules. • It is possible to specify that timer modules operate when an event is input. • Event link operation is possible for port B. — Single-port: Event link operation can be enabled for a specified single bit in a port. — Port group: Event link operation can be enabled for a group of specified bits within an 8-bit I/O port.
Low power consumption function	It is possible to specify the module stop state.	It is possible to specify the module stop state.

Table 2.24 Comparative Listing of Bus Registers

Register	Bit	RX220 (ELC)	RX130 (ELC)
ELSR7	ELS[7:0]	—	Event link setting register 7 [CMT1]
ELSR8	ELS[7:0]	—	Event link setting register 8 [ICU (dedicated LPT interrupt)]
ELSR14	ELS[7:0]	—	Event link setting register 14 [CTSU]
ELSR16	ELS[7:0]	—	Event link setting register 16 [DA0]
ELOPC	—	—	Event Link Option Setting Register C

Table 2.25 Comparative Listing of ELSRn Register Setting Values

Setting Value	RX220	RX130	Event
1Fh	—	○	CMT1, compare match 1
32h	—	○	LPT, compare match
34h	—	○	S12AD, compare condition met
35h	—	○	S12AD, compare condition unmet
52h	○	—	RSPI0 error (mode fault, overrun, or parity error)
53h	○	—	RSPI0 idle
54h	○	—	RSPI0 receive data full
55h	○	—	RSPI0 transmit data empty
56h	○	—	RSPI0 transmit end (except during clock synchronous operation in slave mode)
59h	—	○	Comparator B0, comparison result change
5Ah	—	○	Comparator B0 and B1, common comparison result change

2.12 I/O Ports

Table 2.26 to Table 2.28 shows a comparative listing of specifications of I/O ports, and Table 2.29 shows a comparative listing of I/O port functions, and Table 2.30 shows a comparative listing of the I/O port registers.

Table 2.26 Comparative Listing of Specifications of I/O Ports (100 Pins)

Port	RX220	RX130
PORT0	P03, P05, P07	P03 to P07
PORT1	P12 to P17	P12 to P17
PORT2	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P55	P50 to P55
PORTA	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7
PORTH	PH0 to PH3	PH0 to PH3
PORTJ	PJ1, PJ3	PJ1, PJ3, PJ6, PJ7

Table 2.27 Comparative Listing of Specifications of I/O Ports (64 Pins)

Port	RX220	RX130
PORT0	P03, P05	P03, P05
PORT1	P14 to P17	P14 to P17
PORT2	P26, P27	P26, P27
PORT3	P30 to P32, P35 to P37	P30 to P32, P35 to P37
PORT4	P40 to P44, P46	P40 to P47
PORT5	P54, P55	P54, P55
PORTA	PA0, PA1, PA3, PA4, PA6	PA0, PA1, PA3, PA4, PA6
PORTB	PB0, PB1, PB3, PB5 to PB7	PB0, PB1, PB3, PB5 to PB7
PORTC	PC2 to PC7	PC0 to PC7*[1]
PORTD	Not provided	Not provided
PORTE	PE0 to PE5	PE0 to PE5
PORTH	PH0 to PH3	PH0 to PH3
PORTJ	Not provided	PJ6, PJ7

Note 1. PC0 and PC1 are valid only when switching by the port switching register A.

Table 2.28 Comparative Listing of Specifications of I/O Ports (48 Pins)

Port	RX220	RX130
PORT0	Not provided	Not provided
PORT1	P14 to P17	P14 to P17
PORT2	P26, P27	P26, P27
PORT3	P30, P31, P35 to P37	P30, P31, P35 to P37
PORT4	P40 to P42, P46	P40 to P42, P45 to P47
PORT5	Not provided	Not provided
PORTA	PA1, PA3, PA4, PA6	PA1, PA3, PA4, PA6
PORTB	PB0, PB1, PB3, PB5	PB0, PB1, PB3, PB5
PORTC	PC4 to PC7	PC0 to PC7*[1]
PORTD	Not provided	Not provided
PORTE	PE1 to PE4	PE1 to PE4
PORTH	PH0 to PH3	PH0 to PH3
PORTJ	Not provided	PJ6, PJ7

Note 1. PC0 to PC3 are valid only when switching by the port switching register B.

Table 2.29 Comparative Listing of I/O Port Functions

Item	Port Symbol	RX220	RX130
Input pull-up function	PORT0	P03, P05, P07	P03, P04, P05, P06, P07
	PORT1	P12, P13, P14, P15, P16, P17	P12, P13, P14, P15, P16, P17
	PORT2	P20, P21, P22, P23, P24, P25, P26, P27	P20, P21, P26, P27
	PORT3	P30, P31, P32, P33, P34, P36, P37	P30, P31, P32, P34, P36, P37
	PORT4	P40, P41, P42, P43, P44, P45, P46, P47	P40, P41, P42, P43, P44, P45, P46, P47
	PORT5	P50, P51, P52, P53, P54, P55	P54, P55
	PORTA	PA0, PA1, PA2, PA3, PA4, PA5, PA6, PA7	PA0, PA1, PA2, PA3, PA4, PA5, PA6
	PORTB	PB0*[2], PB1*[2], PB2, PB3*[2], PB4, PB5*[2], PB6*[1], PB7*[1]	PB0*[2], PB1*[2], PB2, PB3*[2], PB4, PB5*[2], PB6*[1], PB7*[1]
	PORTC	PC0*[1]*[2], PC1*[1]*[2], PC2*[2], PC3*[2], PC4, PC5, PC6, PC7	PC0*[1]*[2], PC1*[1]*[2], PC2*[2], PC3*[2], PC4, PC5, PC6, PC7
	PORTD	PD0, PD1, PD2, PD3, PD4, PD5, PD6, PD7	PD0, PD1, PD2
	PORTE	PE0, PE1, PE2, PE3, PE4, PE5, PE6, PE7	PE0, PE1, PE2, PE3, PE4, PE5
	PORTH	PH0, PH1, PH2, PH3	PH0, PH1, PH2, PH3
	PORTJ	PJ1, PJ3	PJ1, PJ6, PJ7
Open-drain output function	PORT1	P12, P13, P15, P16, P17	P12, P13, P14, P15, P16, P17
	PORT2	P26, P27	P26, P27
	PORT3	P30, P32, P33, P34	P30, P31, P32, P34, P36, P37
	PORTA	PA1, PA2, PA3, PA4, PA5, PA6, PA7	PA0, PA1, PA2, PA3, PA4, PA5, PA6
	PORTB	PB0*[2], PB1*[2], PB3, PB5, PB6, PB7	PB0*[2], PB1*[2], PB2, PB3
	PORTC	PC0*[1]*[2], PC1*[1]*[2], PC2*[2], PC3*[2], PC4, PC5, PC6, PC7	PC0*[1]*[2], PC1*[1]*[2], PC2*[2], PC3*[2], PC4, PC5, PC6, PC7
	PORTD	—	PD0, PD1, PD2

Item	Port Symbol	RX220	RX130
	PORTE	PE0, PE1, PE2	PE0, PE1, PE2, PE3
Drive capacity switching function	PORT1	P12, P13, P14, P15, P16, P17	P12, P13, P14, P15, P16, P17
	PORT2	—	P20, P21, P26, P27
	PORT3	—	P30, P31, P32, P34
	PORT5	—	P54, P55
	PORTA	—	PA0, PA1, PA2, PA3, PA4, PA5, PA6
	PORTB	PB0*2, PB1*2, PB2, PB3*2, PB4, PB5*2, PB6*1, PB7*1	PB0*2, PB1*2, PB2, PB3*2, PB4, PB5*2, PB6*1, PB7*1
	PORTC	PC0*1*2, PC1*1*2, PC2*2, PC3*2, PC4, PC5, PC6, PC7	PC0*1*2, PC1*1*2, PC2*2, PC3*2, PC4, PC5, PC6, PC7
	PORTD	—	PD0, PD1, PD2
	PORTE	—	PE0, PE1, PE2, PE3, PE4, PE5
	PORTH	—	PH0, PH1, PH2, PH3
	PORTJ	—	PJ1, PJ6, PJ7
5 V tolerant	PORT1	P12, P13, P16, P17	P12, P13, P16, P17

Notes: 1. On 80-pin (RX130 only) and 64-pin package products, pins PB6 and PC0, and PB7 and PC1 have multiplexed functions. These can be switched by making settings to the PSRA register. The pin functions conform to the settings of the selected port.

2. On 48-pin package products, pins PB0 and PC0, PB1 and PC1, PB3 and PC2, and PB5 and PC3 have multiplexed functions. These can be switched by making settings to the PSRB register. The pin functions conform to the settings of the selected port.

Table 2.30 Comparative Listing of I/O Port Registers

Register	Bit	RX220	RX130
ODR0	B2, B3	Pn1 output type select bit • PA1, PB1, PC1 b2 0: CMOS output 1: N-channel open-drain output b3 This bit is read as 0. The write value should be 0. • PE1 b3 b2 00: CMOS output 01: N-channel open-drain output 10: P-channel open-drain output 11: Hi-Z	Pm1 output type select bit • P31, PA1, PB1, PC1,PD1 b2 0: CMOS output 1: N-channel open-drain output b3 This bit is read as 0. The write value should be 0. • PE1 b3 b2 00: CMOS output 01: N-channel open-drain output 10: P-channel open-drain output 11: Hi-Z

2.13 Multi-Function Pin Controller

Table 2.31 shows a comparative listing of functions assigned to each multiplexed pin, and Table 2.32 shows a comparative listing of the multi-function pin controller port registers.

Blue characters exist only in the RX220, and orange characters exist only in the RX130. "√" indicates pin implemented, "×" indicates pin not implemented, "-" indicates no assignment pin for function, Grey hatching indicates pin function not implemented.

Table 2.31 Comparative Listing of Functions Assigned to Each Multiplexed Pin

Module/Function	Pin Functions	Allocation Port	RX220			RX130		
			100 pin	64 pin	48 pin	100 pin	64 pin	48 pin
Interrupt	NMI(input)	P35	○	○	○	○	○	○
	IRQ0(input)	P30	○	○	○	○	○	○
		PD0	○	×	×	○	×	×
		PH1	○	○	○	○	○	○
	IRQ1(input)	P31	○	○	○	○	○	○
		PD1	○	×	×	○	×	×
		PH2	○	○	○	○	○	○
	IRQ2(input)	P32	○	○	×	○	○	×
		P12	○	×	×	○	×	×
		PD2	○	×	×	○	×	×
	IRQ3(input)	P33	○	×	×	○	×	×
		P13	○	×	×	○	×	×
		PD3	○	×	×	○	×	×
	IRQ4(input)	PB1	○	○	○	○	○	○
		P14	○	○	○	○	○	○
		P34	○	×	×	○	×	×
		PD4	○	×	×	○	×	×
	IRQ5(input)	PA4	○	○	○	○	○	○
		P15	○	○	○	○	○	○
		PD5	○	×	×	○	×	×
		PE5	○	○	×	○	○	×
	IRQ6(input)	PA3	○	○	○	○	○	○
		P16	○	○	○	○	○	○
		PD6	○	×	×	○	×	×
		PE6	○	×	×	○	×	×
	IRQ7(input)	PE2	○	○	○	○	○	○
		P17	○	○	○	○	○	○
		PD7	○	×	×	○	×	×
		PE7	○	×	×	○	×	×
Clock generation circuit	CLKOUT (output)	PE3	▨	▨	▨	○	○	○
		PE4	▨	▨	▨	○	○	○
Multi-function timer unit 2	MTIOC0A(input/ output)	P34	○	×	×	○	×	×
		PB3	○	○	○	○	○	○
	MTIOC0B(input/ output)	P13	○	×	×	○	×	×
		P15	○	○	○	○	○	○
		PA1	○	○	○	○	○	○
	MTIOC0C(input/ output)	P32	○	○	×	○	○	×
		PB1	○	○	○	○	○	○

Module/Function	**Pin Functions**	**Allocation Port**	**RX220**			**RX130**		
			100 pin	**64 pin**	**48 pin**	**100 pin**	**64 pin**	**48 pin**
Multi-function timer unit 2	MTIOC0D(input/ output)	P33	○	×	×	○	×	×
		PA3	○	○	○	○	○	○
	MTIOC1A(input/ output)	P20	○	×	×	○	×	×
		PE4	○	○	○	○	○	○
	MTIOC1B(input/ output)	P21	○	×	×	○	×	×
		PB5	○	○	○	○	○	○
	MTIOC2A(input/ output)	P26	○	○	○	○	○	○
		PB5	○	○	○	○	○	○
	MTIOC2B(input/ output)	P27	○	○	○	○	○	○
		PE5	○	○	×	○	○	×
	MTIOC3A(input/ output)	P14	○	○	○	○	○	○
		P17	○	○	○	○	○	○
		PC1	○	×	×	○	×	×
		PC7	○	○	○	○	○	○
		PJ1	○	×	×	○	×	×
	MTIOC3B(input/ output)	P17	○	○	○	○	○	○
		P22	○	×	×	○	×	×
		PB7	○	○	×	○	○	×
		PC5	○	○	○	○	○	○
	MTIOC3C(input/ output)	P16	○	○	○	○	○	○
		PC0	○	×	×	○	×	×
		PC6	○	○	○	○	○	○
		PJ3	○	×	×	○	×	×
	MTIOC3D(input/ output)	P16	○	○	○	○	○	○
		P23	○	×	×	○	×	×
		PB6	○	○	×	○	○	×
		PC4	○	○	○	○	○	○
	MTIOC4A(input/ output)	P24	○	×	×	○	×	×
		PA0	○	○	×	○	○	×
		PB3	○	○	○	○	○	○
		PE2	○	○	○	○	○	○
	MTIOC4B(input/ output)	P30	○	○	○	○	○	○
		P54	○	○	×	○	○	×
		PC2	○	○	×	○	○	×
		PD1	○	×	×	○	×	×
		PE3	○	○	○	○	○	○
	MTIOC4C(input/ output)	P25	○	×	×	○	×	×
		PB1	○	○	○	○	○	○
		PE1	○	○	○	○	○	○
		PE5	○	○	×	○	○	×
	MTIOC4D(input/ output)	P31	○	○	○	○	○	○
		P55	○	○	×	○	○	×
		PC3	○	○	×	○	○	×
		PD2	○	×	×	○	×	×
		PE4	○	○	○	○	○	○

Module/Function	**Pin Functions**	**Allocation Port**	**RX220**			**RX130**		
			100 pin	**64 pin**	**48 pin**	**100 pin**	**64 pin**	**48 pin**
Multi-function timer unit 2	MTIC5U(input)	PA4	○	○	○	○	○	○
		PD7	○	×	×	○	×	×
	MTIC5V(input)	PA6	○	○	○	○	○	○
		PD6	○	×	×	○	×	×
	MTIC5W(input)	PB0	○	○	○	○	○	○
		PD5	○	×	×	○	×	×
	MTCLKA(input)	P14	○	○	○	○	○	○
		P24	○	×	×	○	×	×
		PA4	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	MTCLKB(input)	P15	○	○	○	○	○	○
		P25	○	×	×	○	×	×
		PA6	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	MTCLKC(input)	P22	○	×	×	○	×	×
		PA1	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	MTCLKD(input)	P23	○	×	×	○	×	×
		PA3	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
Port output enable 2	POE0#(input)	PC4	○	○	○	○	○	○
		PD7	○	×	×	○	×	×
	POE1#(input)	PB5	○	○	○	○	○	○
		PD6	○	×	×	○	×	×
	POE2#(input)	P34	○	×	×	○	×	×
		PA6	○	○	○	○	○	○
		PD5	○	×	×	○	×	×
	POE3#(input)	P33	○	×	×	○	×	×
		PB3	○	○	○	○	○	○
		PD4	○	×	×	○	×	×
	POE8#(input)	P17	○	○	○	○	○	○
		P30	○	○	○	○	○	○
		PD3	○	×	×	○	×	×
		PE3	○	○	○	○	○	○
8-bit timer	TMO0(output)	P22	○	×	×	○	×	×
		PB3	○	○	○	○	○	○
		PH1	○	○	○	○	○	○
	TMCI0(input)	P21	○	×	×	○	×	×
		PB1	○	○	○	○	○	○
		PH3	○	○	○	○	○	○
	TMRI0(input)	P20	○	×	×	○	×	×
		PA4	○	○	○	○	○	○
		PH2	○	○	○	○	○	○
	TMO1(output)	P17	○	○	○	○	○	○
		P26	○	○	○	○	○	○

Module/Function	**Pin Functions**	**Allocation Port**	**RX220**			**RX130**		
			100 pin	**64 pin**	**48 pin**	**100 pin**	**64 pin**	**48 pin**
8-bit timer	TMCI1(input)	P12	○	×	×	○	×	×
		P54	○	○	×	○	○	×
		PC4	○	○	○	○	○	○
	TMRI1(input)	P24	○	×	×	○	×	×
		PB5	○	○	○	○	○	○
	TMO2(output)	P16	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	TMCI2(input)	P15	○	○	○	○	○	○
		P31	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	TMRI2(input)	P14	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
	TMO3(output)	P13	○	×	×	○	×	×
		P32	○	○	×	○	○	×
		P55	○	○	×	○	○	×
	TMCI3(input)	P27	○	○	○	○	○	○
		P34	○	×	×	○	×	×
		PA6	○	○	○	○	○	○
	TMRI3(input)	P30	○	○	○	○	○	○
		P33	○	×	×	○	×	×
Serial communications interface	RXD0 (input)/ SMISO0 (input/output)/ SSCL0 (input/output)	P21				○	×	×
	TXD0 (output)/ SMOSI0 (input/output)/ SSDA0 (input/output)	P20				○	×	×
	SCK0 (input/output)	P22				○	×	×
	CTS0# (input)/ RTS0# (output)/ SS0# (input)	P23				○	×	×
	RXD1(input)/ SMISO1(input/output)/ SSCL1(input/output)	P15	○	○	○	○	○	○
		P30	○	○	○	○	○	○
	TXD1(output)/ SMOSI1(input/output)/ SSDA1(input/output)	P16	○	○	○	○	○	○
		P26	○	○	○	○	○	○
	SCK1(input/output)	P17	○	○	○	○	○	○
		P27	○	○	○	○	○	○
	CTS1#(input)/ RTS1#(output)/ SS1#(input)	P14	○	○	○	○	○	○
		P31	○	○	○	○	○	○
	RXD5(input)/ SMISO5(input/output)/ SSCL5(input/output)/ IRRXD5(input)	PA2	○	×	×	○	×	×
		PA3	○	○	○	○	○	○
		PC2	○	○	×	○	○	×

Module/Function	Pin Functions	Allocation Port	RX220			RX130		
			100 pin	64 pin	48 pin	100 pin	64 pin	48 pin
Serial communications interface	TXD5(output)/ SMOSI5(input/output)/ SSDA5(input/output)/ IRTXD5(output)	PA4	○	○	○	○	○	○
		PC3	○	○	×	○	○	×
	SCK5(input/output)	PA1	○	○	○	○	○	○
		PC1	○	×	×	○	×	×
		PC4	○	○	○	○	○	○
	CTS5#(input)/ RTS5#(output)/ SS5#(input)	PA6	○	○	○	○	○	○
		PC0	○	×	×	○	×	×
	RXD6(input)/ SMISO6(input/output)/ SSCL6(input/output)	P33	○	×	×	○	×	×
		PB0	○	○	○	○	○	○
		PD1	−	−	−	○	×	×
	TXD6(output)/ SMOSI6(input/output)/ SSDA6(input/output)	P32	○	○	×	○	○	×
		PB1	○	○	○	○	○	○
		PD0	−	−	−	○	×	×
	SCK6(input/output)	P34	○	×	×	○	×	×
		PB3	○	○	○	○	○	○
		PD2	−	−	−	○	×	×
	CTS6#(input)/ RTS6#(output)/ SS6#(input)	PB2	○	×	×	○	×	×
		PJ3	○	×	×	○	×	×
	RXD8 (input)/ SMISO8 (input/output)/ SSCL8 (input/output)	PC6	▨	▨	▨	○	×	×
	TXD8 (output)/ SMOSI8 (input/output)/ SSDA8 (input/output)	PC7	▨	▨	▨	○	×	×
	SCK8 (input/output)	PC5	▨	▨	▨	○	×	×
	CTS8# (input)/ RTS8# (output)/ SS8# (input)	PC4	▨	▨	▨	○	×	×
	RXD9(input)/ SMISO9(input/output)/ SSCL9(input/output)	PB6	○	○	×	○	×	×
	TXD9(output)/ SMOSI9(input/output)/ SSDA9(input/output)	PB7	○	○	×	○	×	×
	SCK9(input/output)	PB5	○	○	×	○	×	×
	CTS9#(input)/ RTS9#(output)/ SS9#(input)	PB4	○	×	×	○	×	×

Module/Function	Pin Functions	Allocation Port	RX220			RX130		
			100 pin	64 pin	48 pin	100 pin	64 pin	48 pin
Serial communications interface	RXD12(input)/ SMISO12(input/ output)/ SSCL12(input/ output)/ RXDX12(input)	PE2	○	○	○ (SMISO12 function is not available)	○	○	○ (SMISO12 function is not available)
	TXD12(output)/ SMOSI12(input/ output)/ SSDA12(input/ output)/ TXDX12(output)/ SIOX12(input/output)	PE1	○	○	○ (SMOSI12 function is not available)	○	○	○ (SMOSI12 function is not available)
	SCK12(input/ output)	PE0	○	○	×	○	○	×
	CTS12#(input)/ RTS12#(output)/ SS12#(input)	PE3	○	○	○ (SS12# function is not available)	○	○	○ (SS12# function is not available)
I2C bus interface	SCL(input/output)	P16	○	○	○	○	○	○
		P12	○	×	×	○	×	×
	SDA(input/output)	P17	○	○	○	○	○	○
		P13	○	×	×	○	×	×
Serial peripheral interface	RSPCKA(input/ output)	PA5	○	×	×	○	×	×
		PB0	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
	MOSIA(input/ output)	P16	○	○	○	○	○	○
		PA6	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	MISOA(input/ output)	P17	○	○	○	○	○	○
		PA7	○	×	×	○	×	×
		PC7	○	○	○	○	○	○
	SSLA0(input/ output)	PA4	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	SSLA1(output)	PA0	○	○	×	○	○	×
		PC0	○	×	×	○	×	×
	SSLA2(output)	PA1	○	○	○	○	○	○
		PC1	○	×	×	○	×	×
	SSLA3(output)	PA2	○	×	×	○	×	×
		PC2	○	○	×	○	○	×
Realtime clock	RTCOUT(output)	P16	○	○	×	○	○	×
		P32	○	○	×	○	○	×

Module/Function	**Pin Functions**	**Allocation Port**	**RX220**			**RX130**		
			100 pin	**64 pin**	**48 pin**	**100 pin**	**64 pin**	**48 pin**
12-bit A/D converter	AN000(input)*1	P40	○	○	○	○	○	○
	AN001(input)*1	P41	○	○	○	○	○	○
	AN002(input)*1	P42	○	○	○	○	○	○
	AN003(input)*1	P43	○	○	×	○	○	×
	AN004(input)*1	P44	○	○	×	○	○	×
	AN005(input)*1	P45	○	×	×	○	○	○
	AN006(input)*1	P46	○	○	○	○	○	○
	AN007(input)*1	P47	○	×	×	○	○	○
	AN008(input)*1	PE0	○	○	×			
	AN009(input)*1	PE1	○	○	○			
	AN010(input)*1	PE2	○	○	○			
	AN011(input)*1	PE3	○	○	○			
	AN012(input)*1	PE4	○	○	○			
	AN013(input)*1	PE5	○	○	×			
	AN014(input)*1	PE6	○	×	×			
	AN015(input)*1	PE7	○	×	×			
	AN016(input)*1	PE0				○	○	×
	AN017(input)*1	PE1				○	○	○
	AN018(input)*1	PE2				○	○	○
	AN019(input)*1	PE3				○	○	○
	AN020 (input) *1	PE4				○	○	○
	AN021 (input) *1	PE5				○	○	×
	AN022 (input) *1	PE6				○	×	×
	AN023 (input) *1	PE7				○	×	×
	AN024 (input) *1	PD0				○	×	×
	AN025 (input) *1	PD1				○	×	×
	AN026 (input) *1	PD2				○	×	×
	AN027 (input) *1	PD3				○	×	×
	AN028 (input) *1	PD4				○	×	×
	AN029 (input) *1	PD5				○	×	×
	AN030 (input) *1	PD6				○	×	×
	AN031 (input) *1	PD7				○	×	×
	ADTRG0#(input)	P07	○	×	×	○	×	×
		P16	○	○	○	○	○	○
		P25	○	×	×	○	×	×
D/A converter	DA0 (output) *1	P03				○	○	×
	DA1 (output) *1	P05				○	○	×
Clock frequency accuracy measurement circuit	CACREF(input)	PA0	○	○	×	○	○	×
		PC7	○	○	○	○	○	○
		PH0	○	○	○	○	○	○
Comparator A	CMPA1(input)*1	PE3	○	○	○			
	CMPA2(input)*1	PE4	○	○	○	○	○	○
	CVREFA(input)*1	PA1	○	○	○			
Comparator B	CMPB0 (input) *1	PE1				○	○	○
	CVREFB0 (input) *1	PE2				○	○	○
	CMPOB0 (output)	PE5				○	○	×
	CMPB1 (input) *1	PA3				○	○	○

Module/Function	**Pin Functions**	**Allocation Port**	**RX220**			**RX130**		
			100 pin	**64 pin**	**48 pin**	**100 pin**	**64 pin**	**48 pin**
Comparator B	CVREFB1 (input) *1	PA4				○	○	○
	CMPOB1 (output)	PB1				○	○	○
Capacitive touch sensing unit (CTSU)	TSCAP (—)	PC4				○	○	○
	TS0 (input/output)	P32				○	○	×
Capacitive touch sensing unit (CTSU)	TS1 (input/output)	P31				○	○	○
	TS2 (output)	P30				○	○	○
	TS3 (output)	P27				○	○	○
	TS4 (output)	P26				○	○	○
	TS5 (output)	P15				○	○	○
	TS6 (output)	P14				○	○	○
	TS7 (output)	PH3				○	○	○
	TS8 (output)	PH2				○	○	○
	TS9 (output)	PH1				○	○	○
	TS10 (output)	PH0				○	○	○
	TS11 (output)	P55				○	○	×
	TS12 (output)	P54				○	○	×
	TS13 (output)	PC7				○	○	○
	TS14 (output)	PC6				○	○	○
	TS15 (output)	PC5				○	○	○
	TS16 (output)	PC3				○	○	×
	TS17 (output)	PC2				○	○	×
	TS18 (output)	PB7				○	○	×
	TS19 (output)	PB6				○	○	×
	TS20 (output)	PB5				○	○	○
	TS21 (output)	PB4				○	×	×
	TS22 (output)	PB3				○	○	○
	TS23 (output)	PB2				○	×	×
	TS24 (output)	PB1				○	○	○
	TS25 (output)	PB0				○	○	○
	TS26 (output)	PA6				○	○	○
	TS27 (output)	PA5				○	×	×
	TS28 (output)	PA4				○	○	○
	TS29 (output)	PA3				○	○	○
	TS30 (output)	PA2				○	×	×
	TS31 (output)	PA1				○	○	○
	TS32 (output)	PA0				○	○	×
	TS33 (output)	PE4				○	○	○
	TS34 (output)	PE3				○	○	○
	TS35 (output)	PE2				○	○	○
Remote control signal receiver (REMC)	PMC0	P51				○	×	×
	PMC1	P52				○	×	×

Note 1. Select general input (by setting the Bm bits for the given pin in the PDR and PMR for the given port to 0) for the pin if this pin function is to be used.

Table 2.32 Comparative Listing of Multi-Function Pin Controller Registers

Register	Bit	RX220 (MPC)	RX130 (MPC)
P07PFS	−	P07 Pin Function Control Register	-
P0nPFS (n = 3, 5, 7)	-	-	P0n Pin Function Control Register
P1nPFS (n = 2 to 7)	PSEL	Pin function select (PSEL[3:0]) b3 to b0	Pin function select (PSEL[4:0]) b4 to b0
	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin P12: IRQ2 input switch (100 pins) P13: IRQ3 input switch (100 pins) P14: IRQ4 input switch (100/64/48 pins) P15: IRQ5 input switch (100/64/48 pins) P16: IRQ6 input switch (100/64/48 pins) P17: IRQ7 input switch (100/64/48 pins)	Interrupt Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin P12: IRQ2 input switch (100/80 pins) P13: IRQ3 input switch (100/80 pins) P14: IRQ4 input switch (100/80/64/48 pins) P15: IRQ5 input switch (100/80/64/48 pins) P16: IRQ6 input switch (100/80/64/48 pins) P17: IRQ7 input switch (100/80/64/48 pins)
P2nPFS (n = 0 to 7)	PSEL	Pin function select (PSEL[3:0]) b3 to b0	Pin function select (PSEL[4:0]) b4 to b0
P3nPFS (n = 0 to 4)	PSEL	Pin function select (PSEL[3:0]) b3 to b0	Pin function select (PSEL[4:0]) b4 to b0
	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0 input switch (100/64/48 pins) P31: IRQ1 input switch (100/64/48 pins) P32: IRQ2 input switch (100/64 pins) P33: IRQ3 input switch (100 pins) P34: IRQ4 input switch (100 pins)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0 input switch (100/80/64/48 pins) P31: IRQ1 input switch (100/80/64/48 pins) P32: IRQ2 input switch (100/80/64 pins) P33: IRQ3 input switch (100 pins) P34: IRQ4 input switch (100/80 pins)
P4nPFS (n = 0 to 7)	ASEL	Analog Function Select 0: Not used as an analog pin 1: Used as an analog pin P40: AN000 (100/64/48 pins) P41: AN001 (100/64/48 pins) P42: AN002 (100/64/48 pins) P43: AN003 (100/64 pins) P44: AN004 (100/64 pins) P45: AN005 (100 pins) P46: AN006 (100/64/48 pins) P47: AN007 (100 pins)	Analog Function Select 0: Not used as an analog pin 1: Used as an analog pin P40: AN000 (100/80/64/48 pins) P41: AN001 (100/80/64/48 pins) P42: AN002 (100/80/64/48 pins) P43: AN003 (100/80/64 pins) P44: AN004 (100/80/64 pins) P45: AN005 (100/80/64/48 pins) P46: AN006 (100/80/64/48 pins) P47: AN007 (100/80/64/48 pins)

Register	Bit	RX220 (MPC)	RX130 (MPC)
P5nPFS (n = 4, 5) (RX220) (n = 1, 2, 4, 5) (RX130)	PSEL	Pin function select (PSEL[3:0]) b3 to b0	Pin function select (PSEL[4:0]) b4 to b0
PAnPFS (n = 0 to 7)	PSEL	Pin function select (PSEL[3:0]) b3 to b0	Pin function select (PSEL[4:0]) b4 to b0
	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PA3: IRQ6 input switch (100/64/48 pins) PA4: IRQ5 input switch (100/64/48 pins)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PA3: IRQ6 input switch (100/80/64/48 pins) PA4: IRQ5 input switch (100/80/64/48 pins)
	ASEL	0: Not used as an analog pin 1: Used as an analog pin PA1: CVREFA (100/64/48 pins)	0: Not used as an analog pin 1: Used as an analog pin PA3: CMPB1 (100/80/64/48 pins) PA4: CVREFB1 (100/80/64/48 pins)
PBnPFS (n = 0 to 7)	PSEL	Pin function select (PSEL[3:0]) b3 to b0	Pin function select (PSEL[4:0]) b4 to b0
	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PB1: IRQ4 (100/64/48 pins)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PB1: IRQ4 (100/80/64/48 pins)
PCnPFS (n = 0 to 7)	PSEL	Pin function select (PSEL[3:0]) b3 to b0	Pin function select (PSEL[4:0]) b4 to b0
PDnPFS (n = 0 to 7)	PSEL	Pin function select (PSEL[3:0]) b3 to b0	Pin function select (PSEL[4:0]) b4 to b0
	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PD0: IRQ0 input switch (100 pins) PD1: IRQ1 input switch (100 pins) PD2: IRQ2 input switch (100 pins) PD3: IRQ3 input switch (100 pins) PD4: IRQ4 input switch (100 pins) PD5: IRQ5 input switch (100 pins) PD6: IRQ6 input switch (100 pins) PD7: IRQ7 input switch (100 pins)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PD0: IRQ0 input switch (100/80 pins) PD1: IRQ1 input switch (100/80 pins) PD2: IRQ2 input switch (100/80 pins) PD3: IRQ3 input switch (100 pins) PD4: IRQ4 input switch (100 pins) PD5: IRQ5 input switch (100 pins) PD6: IRQ6 input switch (100 pins) PD7: IRQ7 input switch (100 pins)
	ASEL	Reserved	Analog function select
PEnPFS (n = 0 to 7)	PSEL	Pin function select (PSEL[3:0]) b3 to b0	Pin function select (PSEL[4:0]) b4 to b0

Register	**Bit**	**RX220 (MPC)**	**RX130 (MPC)**
	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PE2: IRQ7 input switch (100/64/48 pins) PE5: IRQ5 input switch (100/64 pins) PE6: IRQ6 input switch (100 pins) PE7: IRQ7 input switch (100 pins)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PE2: IRQ7 input switch (100/80/64/48 pins) PE5: IRQ5 input switch (100/80/64 pins) PE6: IRQ6 input switch (100 pins) PE7: IRQ7 input switch (100 pins)
	ASEL	Analog Function Select 0: Not used as an analog pin 1: Used as an analog pin PE0:AN008 (100/64 pins) PE1:AN009 (100/64/48 pins) PE2:AN010 (100/64/48 pins) PE3:AN011 or CMPA1 (100/64/48 pins) PE4:AN012 or CMPA2 (100/64/48 pins) PE5:AN013 (100/64 pins) PE6:AN014 (100 pins) PE7:AN015 (100 pins)	Analog Function Select 0: Not used as an analog pin 1: Used as an analog pin PE0:AN016 (100/80/64 pins) PE1:AN017 or CMPB0 (100/80/64/48 pins) PE2:AN018 or CVREFB0 (100/80/64/48 pins) PE3:AN019 (100/80/64/48 pins) PE4:AN020 or CMPA2 (100/80/64/48 pins) PE5:AN021 (100/80/64 pins) PE6:AN022 (100 pins) PE7:AN023 (100 pins)
PHnPFS (n = 0 to 3)	PSEL	Pin function select (PSEL[3:0]) b3 to b0	Pin function select (PSEL[4:0]) b4 to b0
	ISEL	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PH1: IRQ0 (100/64/48 pins) PH2: IRQ1 (100/64/48 pins)	Interrupt Input Function Select 0: Not used as IRQn input pin 1: Used as IRQn input pin PH1: IRQ0 input switch (100/80/64/48 pins) PH2: IRQ1 input switch (100/80/64/48 pins)
PJnPFS (n = 1, 3) (RX220) (n = 1, 3, 6, 7) (RX130)	PSEL	Pin function select (PSEL[3:0]) b3 to b0	Pin function select (PSEL[4:0]) b4 to b0
	ASEL	Reserved	Analog function select

2.14 8-Bit Timer

Table 2.33 shows a comparative overview of the 8-Bit Timer specification.

Table 2.33 Comparative Overview of 8-Bit Timer

Item	RX220 (CMT)	RX130 (CMT)
Count clock	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192 • External clock: external count clock	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192 • External clock: external count clock
Number of channels	(8 bits × 2 channels) × 2 units	(8 bits × 2 channels) × 2 units
Compare match	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)
Counter clear	Selected by compare match A or B, or an external reset signal.	Selected by compare match A or B, or an external reset signal.
Timer output	Output pulses with a desired duty cycle or PWM output	Output pulses with a desired duty cycle or PWM output
Cascading of two channels	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).
Interrupt sources	Compare match A, compare match B, and overflow	Compare match A, compare match B, and overflow
Event link function (Output)	Compare match A, compare match B, and overflow (TMR0, TMR2)	Compare match A, compare match B, and overflow (TMR0, TMR2)
Event link function (Input)	One of the following three operations proceeds in response to an event reception: (1) Counting start operation (TMR0, TMR2) (2) Event counting operation (TMR0, TMR2) (3) Counting restart operation (TMR0, TMR2)	One of the following three operations proceeds in response to an event reception: (1) Counting start operation (TMR0, TMR2) (2) Event counting operation (TMR0, TMR2) (3) Counting restart operation (TMR0, TMR2)
DTC activation	DTC can be activated by compare match A interrupts or compare match B interrupts.	DTC can be activated by compare match A interrupts or compare match B interrupts.
Capable of generating baud rate clock for SCI	Generates baud rate clock for SCI.	Generates baud rate clock for SCI.
Capable of generating receive clock for REMC	—	Generates operating clock for remote control signal receiver (REMC)
Low power consumption function	Each unit can be placed in a module stop state	Each unit can be placed in a module stop state

2.15 Compare Match Timer

Table 2.34 shows a comparative overview of the compare match timer specification, and Table 2.35 shows a comparative listing of the compare match timer registers.

Table 2.34 Comparative Overview of Compare Match Timer

Item	RX220 (CMT)	RX130 (CMT)
Number of units	2 units	1 unit
Number of channels	4 channels	2 channels
Count clocks	Four frequency-divided clocks One clock from PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected independently for each channel.	Four frequency-divided clocks One clock from PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.
Interrupt	A compare match interrupt can be requested independently for each channel.	A compare match interrupt can be requested for each channel.
Event link function (output)	—	Event signal output at CMT1 compare match
Event link function (input)	—	• Support for linked operation of specified module • Support for CMT1 counter start, event counter, and count restart
Low power consumption function	It is possible to specify the module stop state.	It is possible to specify the module stop state.

Table 2.35 Comparative Listing of Compare Match Timer Registers

Register	Bit	RX220 (CMT)	RX130 (CMT)
CMSTR1	—	Compare match timer start register 1	—

2.16 Independent Watchdog Timer

Table 2.36 shows a comparative overview of the independent watchdog timer specification, and Table 2.37 shows a comparative listing of the independent watchdog timer registers.

Table 2.36 Comparative Overview of Independent Watchdog Timer

Item	RX220 (IWDTa)	RX130 (IWDTa)
Count source	IWDTCLK (125 kHz)	IWDTCLK (15 kHz)

Table 2.37 Comparative Listing of Independent Watchdog Timer Registers

Register	Bit	RX220 (IWDTa)	RX130 (IWDTa)
IWDTCR	TOPS[1:0]	Timeout period select bits b1 b0 0 0: 1,024 cycles (03FFh) 0 1: 4,096 cycles (0FFFh) 1 0: 8,192 cycles (1FFFh) 1 1: 16,384 cycles (3FFFh)	Timeout period select bits b1 b0 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1,024 cycles (03FFh) 1 1: 2,048 cycles (07FFh)
IWDTCSTPR	SLCSTP	Sleep Mode Count Stop Control 0: Count stop is disabled 1: Count is stopped at a transition to sleep mode, software standby mode, or all-module clock stop mode	Sleep Mode Count Stop Control 0: Count stop is disabled. 1: Count is stopped at a transition to sleep mode, software standby mode, or deep sleep mode.

2.17 Serial Communication Interface

Table 2.38, Table 2.39 shows a comparative overview of the serial communication interface specifications, and Table 2.40 shows a comparative listing of the serial communications interface registers.

Table 2.38 Comparative Overview of Serial Communication Interface (SCIe: RX220, SCIg:RX130)

Item	**RX220 (SCIe)**	**RX130 (SCIg)**
Number of channels	4 channels (SCI1, SCI5, SCI6, SCI9)	6 channels (SCI0, SCI1, SCI5, SCI6, SCI8, SCI9)
Serial communication modes	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed	Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication	• Transmitter: Continuous transmission possible using double-buffer configuration. • Receiver: Continuous reception possible using double-buffer configuration.	• Transmitter: Continuous transmission possible using double-buffer configuration. • Receiver: Continuous reception possible using double-buffer configuration.
I/O pins	• SCI I/O pins (asynchronous mode and clock synchronous mode) SCK1, RXD1, TXD1, CTS1#/RTS1# SCK5, RXD5, TXD5, CTS5#/RTS5# SCK6, RXD6, TXD6, CTS6#/RTS6# SCK9, RXD9, TXD9, CTS9#/RTS9# • SCI I/O pins (simple I²C mode) SSCL1, SSDA1, SSCL5, SSDA5, SSCL6, SSDA6, SSCL9, SSDA9, • SCI I/O pins (simple SPI mode) SCK1, SMISO1, SMOSI1, SS1#, SCK5, SMISO5, SMOSI5, SS5#, SCK6, SMISO6, SMOSI6, SS6#, SCK9, SMISO9, SMOSI9, SS9#,	• SCI I/O pins (asynchronous mode and clock synchronous mode) SCK0, RXD0, TXD0, CTS0#/RTS0# SCK1, RXD1, TXD1, CTS1#/RTS1# SCK5, RXD5, TXD5, CTS5#/RTS5# SCK6, RXD6, TXD6, CTS6#/RTS6# SCK8, RXD8, TXD8, CTS8#/RTS8# SCK9, RXD9, TXD9, CTS9#/RTS9# • SCI I/O pins (simple I²C mode) SSCL0, SSDA0, SSCL1, SSDA1, SSCL5, SSDA5, SSCL6, SSDA6, SSCL8, SSDA8, SSCL9, SSDA9, • SCI I/O pins (simple SPI mode) SCK0, SMISO0, SMOSI0, SS0#, SCK1, SMISO1, SMOSI1, SS1#, SCK5, SMISO5, SMOSI5, SS5#, SCK6, SMISO6, SMOSI6, SS6#, SCK8, SMISO8, SMOSI8, SS8#, SCK9, SMISO9, SMOSI9, SS9#,
Data transfer	Selectable between LSB-first or MSB-first transfer.	Selectable between LSB-first or MSB-first transfer.

Item		**RX220 (SCIe)**	**RX130 (SCIg)**
Interrupt sources		Transmit end, transmit data empty, receive data full, receive error, completion of generation of start condition, restart condition, or stop condition (simple I^{2}C mode)	Transmit end, transmit data empty, receive data full, receive error, completion of generation of start condition, restart condition, or stop condition (simple I^{2}C mode)
Low power consumption function		The module stop state can be specified for each channel.	The module stop state can be specified for each channel.
Asynchronous mode	Data length	7 or 8 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	The CTSn# and RTSn# pins can be used to control transmission and reception.	The CTSn# and RTSn# pins can be used to control transmission and reception.
	Start bit detection	Selectable between low level and falling edge.	Selectable between low level and falling edge.
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.
	Clock source	An internal or external clock can be selected. Transfer rate clock input from the TMR can be used (SCI5 and SCI6).	An internal or external clock can be selected. Transfer rate clock input from the TMR can be used (SCI5 and SCI6).
	Double-speed mode	—	Baud rate generator double-speed mode is selectable.
	Multi-processor communication function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate on-chip digital noise filters.	The signal paths from input on the RXDn pins incorporate on-chip digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	The CTSn# and RTSn# pins can be used to control transmission and reception.	The CTSn# and RTSn# pins can be used to control transmission and reception.
Smart card interface mode	Error processing	An error signal can be transmitted automatically when a parity error is detected during reception.	An error signal can be transmitted automatically when a parity error is detected during reception.
		Data can be retransmitted automatically when an error signal is received during transmission.	Data can be retransmitted automatically when an error signal is received during transmission.
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.

Item		RX220 (SCIe)	RX130 (SCIg)
Simple I^{2}C mode	Communication format	I^{2}C bus format	I^{2}C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer speed	Fast mode is supported.	Fast mode is supported.
	Noise canceler	The signal paths from input on the SSCLn and SSDAn pins incorporate on-chip digital noise filters, and the noise cancellation bandwidth is adjustable.	The signal paths from input on the SSCLn and SSDAn pins incorporate on-chip digital noise filters, and the noise cancellation bandwidth is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Error detection	Overrun error	Overrun error
	SS input pin function	Applying a high-level signal to the SSn# pin causes the output pins to enter the high-impedance state.	Applying a high-level signal to the SSn# pin causes the output pins to enter the high-impedance state.
	Clock settings	Selectable among four clock phase and clock polarity settings.	Selectable among four clock phase and clock polarity settings.
Bit rate modulation function		—	On-chip baud rate generator output correction can reduce errors.
Event link function (supported by SCI5 only)		Error (receive error or error signal detection) event output	Error (receive error or error signal detection) event output
		Receive data full event output	Receive darta full event output
		Transmit data empty event output	Transmit data empty event output
		Transmit end event output	Transmit end event output

Table 2.39 Comparative Overview of Serial Communication Interface (SCIf: RX220, SCIg: SCIh)

Item	RX220 (SCIf)	RX130 (SCIh)
Number of channels	1 channels (SCI12)	1 channels (SCI12)
Serial communication modes	• Asynchronous • Clock synchronous • Smart card interface • Simple I^{2}C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I^{2}C bus • Simple SPI bus
Transfer speed	Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication	• Transmitter: Continuous transmission possible using double-buffer configuration. • Receiver: Continuous reception possible using double-buffer configuration.	• Transmitter: Continuous transmission possible using double-buffer configuration. • Receiver: Continuous reception possible using double-buffer configuration.

Item		RX220 (SCIf)	RX130 (SCIh)
I/O pins		• SCI I/O pins (asynchronous mode and clock synchronous mode) SCK12, RXD12, TXD12, CTS12#/RTS12# • SCI I/O pins (simple I^{2}C mode) SSCL12, SSDA12 • SCI I/O pins (simple SPI mode) SCK12, SMISO12, SMOSI12, SS12# • SCI I/O pins (extended serial mode) RXDX12, TXDX12, SIOX12	• SCI I/O pins (asynchronous mode and clock synchronous mode) SCK12, RXD12, TXD12, CTS12#/RTS12# • SCI I/O pins (simple I^{2}C mode) SSCL12, SSDA12 • SCI I/O pins (simple SPI mode) SCK12, SMISO12, SMOSI12, SS12# • SCI I/O pins (extended serial mode) RXDX12, TXDX12, SIOX12
Data transfer		Selectable between LSB-first or MSB-first transfer.	Selectable between LSB-first or MSB-first transfer.
Interrupt sources		Transmit end, transmit data empty, receive data full, receive error, completion of generation of start condition, restart condition, or stop condition (simple I^{2}C mode)	Transmit end, transmit data empty, receive data full, receive error, completion of generation of start condition, restart condition, or stop condition (simple I^{2}C mode)
Low power consumption function		The module stop state can be specified for each channel.	The module stop state can be specified for each channel.
Asynchronous mode	Data length	7 or 8 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	The CTSn# and RTSn# pins can be used to control transmission and reception.	The CTSn# and RTSn# pins can be used to control transmission and reception.
	Start bit detection	Selectable between low level and falling edge.	Selectable between low level and falling edge.
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.
	Clock source	An internal or external clock can be selected. Transfer rate clock input from the TMR can be used (SCI5 and SCI6).	An internal or external clock can be selected. Transfer rate clock input from the TMR can be used (SCI5 and SCI6).
	Double-speed mode	—	Baud rate generator double-speed mode is selectable.
	Multi-processor communication function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate on-chip digital noise filters.	The signal paths from input on the RXDn pins incorporate on-chip digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error

Item		**RX220 (SCIf)**	**RX130 (SCIh)**
	Hardware flow control	The CTSn# and RTSn# pins can be used to control transmission and reception.	The CTSn# and RTSn# pins can be used to control transmission and reception.
Smart card interface mode	Error processing	An error signal can be transmitted automatically when a parity error is detected during reception.	An error signal can be transmitted automatically when a parity error is detected during reception.
		Data can be retransmitted automatically when an error signal is received during transmission.	Data can be retransmitted automatically when an error signal is received during transmission.
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^{2}C mode	Communication format	I^{2}C bus format	I^{2}C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer speed	Fast mode is supported.	Fast mode is supported.
	Noise canceler	The signal paths from input on the SSCLn and SSDAn pins incorporate on-chip digital noise filters, and the noise cancellation bandwidth is adjustable.	The signal paths from input on the SSCLn and SSDAn pins incorporate on-chip digital noise filters, and the noise cancellation bandwidth is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Error detection	Overrun error	Overrun error
	SS input pin function	Applying a high-level signal to the SSn# pin causes the output pins to enter the high-impedance state.	Applying a high-level signal to the SSn# pin causes the output pins to enter the high-impedance state.
	Clock settings	Selectable among four clock phase and clock polarity settings.	Selectable among four clock phase and clock polarity settings.
Extended serial mode	Start frame transmission	• Output of the break field low width and generation of an interrupt on detection • Detection of bus collisions and the generation of interrupts on detection	• Output of the break field low width and generation of an interrupt on detection • Detection of bus collisions and the generation of interrupts on detection
	Start frame reception	• Detection of the break field low width and generation of an interrupt on detection • Comparison of data in control fields 0 and 1 and generation of an interrupt when the two match • Two kinds of data for comparison (primary and secondary) can be set in control field 1. • A priority interrupt bit can be set in control field 1. • Support for handling of start frames that do not include a break field • Support for handling of start frames that do not include control field 0 • Function for measuring bit rates	• Detection of the break field low width and generation of an interrupt on detection • Comparison of data in control fields 0 and 1 and generation of an interrupt when the two match • Two kinds of data for comparison (primary and secondary) can be set in control field 1. • A priority interrupt bit can be set in control field 1. • Support for handling of start frames that do not include a break field • Support for handling of start frames that do not include control field 0 • Function for measuring bit rates

Item		**RX220 (SCIf)**	**RX130 (SCIh)**
Extended serial mode	I/O control functions	• Selectable polarity for TXDX12 and RXDX12 signals • Ability to enable digital filter function for RXDX12 • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Selectable timing for the sampling of data received through RXDX12 • Signals received on RXDX12 can be passed through to SCIg when the extended serial mode control section is off.	• Selectable polarity for TXDX12 and RXDX12 signals • Ability to enable digital filter function for RXDX12 • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Selectable timing for the sampling of data received through RXDX12 • Signals received on RXDX12 can be passed through to SCIg when the extended serial mode control section is off.
	Timer function	Usable as a reloading timer	Usable as a reloading timer
Bit rate modulation function		—	On-chip baud rate generator output correction can reduce errors.

Table 2.40 Comparative Listing of Serial Communication Interface Registers

Register	Bit	RX220(SCIe, SCIf)	RX130(SCIg, SCIh)
RDRH	—	—	Receive data register H
RDRL	—	—	Receive data register L
RDRHL	—	—	Receive data register HL
TDRH	—	—	Transmit data register H
TDRL	—	—	Transmit data register L
TDRHL	—	—	Transmit data register HL
SMR	CHR	Character length bit (Valid only in asynchronous mode) 0: Transmission/reception data length of 8 bits 1: Transmission/reception data length of 7 bits	Character length bit (Valid only in asynchronous mode) Select together with the SCMR.CHR1 bit. CHR1 CHR 0 0: Transmission/reception data length of 9 bits 0 1: Transmission/reception data length of 9 bits 1 0: Transmission/reception data length of 8 bits (initial value) 1 1: Transmission/reception data length of 7 bits
SSR	RDRF	—	Receive Data Full Flag
	TDRE	—	Transmit Data Empty Flag
SCMR	SMIF	Smart Card Interface Mode Select 0: Serial communications interface mode 1: Smart card interface mode	Smart Card Interface Mode Select 0: Non-smart card interface mode (Asynchronous mode, clock synchronous mode, simple SPI mode, or simple I2C mode) 1: Smart card interface mode
	CHR1	—	Character length bit 1
MDDR	—	—	Modulation duty register
SEMR	BRME	—	Bit rate modulation enable bit
	BGDM	—	Baud rate generator double-speed mode select bit
CR2	BCCS[1:0]	Bus collision detection clock select bits b5 b4 0 0: SCI base clock 0 1: SCI base clock frequency divided by 2 1 0: SCI base clock frequency divided by 4 1 1: Setting prohibited	Bus collision detection clock select bits When SEMR.BGDM bit is cleared to 0 or SEMR.BGDM bit is set to 1 and SMR.CKS[1:0] bits are set to value other than 00b b5 b4 0 0: SCI base clock 0 1: SCI base clock frequency divided by 2 1 0: SCI base clock frequency divided by 4 1 1: Setting prohibited When SEMR.BGDM bit is set to 1 and SMR.CKS[1:0] bits are set to

			00b b5 b4 0 0: SCI base clock frequency divided by 2 0 1: SCI base clock frequency divided by 4 1 0: Setting prohibited 1 1: Setting prohibited

2.18 I2C Bus Interface

Table 2.41 shows a comparative listing of the I^{2}C bus interface registers.

Table 2.41 Comparative Listing of Serial Communication Interface Registers

Register	Bit	RX220 (RIIC)	RX130 (RIICa)
ICMR2	TMWE	Timeout internal counter write enable bit	—
TMOCNT	—	Timeout internal counter	—

2.19 Serial Peripheral Interface

Table 2.42 shows a comparative overview of the serial peripheral interface specifications, and Table 2.43 shows a comparative listing of the serial peripheral interface registers.

Table 2.42 Comparative Overview of Serial Peripheral Interface

Item	RX220 (RSPI)	RX130 (RSPIa)
Number of channels	1 channel	1 channel
RSPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communication through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Serial communication is available in master and slave mode. • Switching of the polarity of RSPCK is supported. • Switching of the phase of RSPCK is supported.	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communication through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK is supported. • Switching of the phase of RSPCK is supported.
Data format	• Selectable between MSB-first and LSB-first. • Transfer bit length is selectable among 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (with each frame consisting of up to 32 bits).	• Selectable between MSB-first and LSB-first. • Transfer bit length is selectable among 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (with each frame consisting of up to 32 bits).

Item	**RX220 (RSPI)**	**RX130 (RSPIa)**
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the maximum division ratio is 4,096). • In slave mode, the externally input clock is used as the serial clock (the maximum frequency is PCLK divided by 8). Width at high level: 4 cycles of PCLK; width at low level: 4 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from 2 to 4096). • In slave mode, the minimum PCLK clock divided by 8 can be input as RSPCK (the maximum frequency of RSPCK is PCLK divided by 8). Width at high level: 4 cycles of PCLK; width at low level: 4 cycles of PCLK
Buffer configuration	• The transmit and receive buffers have a double buffer configuration. • The transmit and receive buffers are each 128 bits in size.	• The transmit and receive buffers have a double buffer configuration. • The transmit and receive buffers are each 128 bits in size.
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection	• Mode fault error detection • Overrun error detection • Parity error detection
SSL control function	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin is input, and SSLA1 to SSLA3 pins are either output or unused. • In slave mode: SSLA0 pin is input, and SSLA1 to SSLA3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • SSL polarity-change function	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin is input, and SSLA1 to SSLA3 pins are either output or unused. • In slave mode: SSLA0 pin is input, and SSLA1 to SSLA3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • SSL polarity-change function

Item	RX220 (RSPI)	RX130 (RSPIa)
Control in master transfer	• Transfers of up to eight commands can be performed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, LSB/MSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • The MOSI signal value when SSL is negated can be specified.	• Transfers of up to eight commands can be performed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, LSB/MSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • The MOSI signal value when SSL is negated can be specified. • RSPCK auto-stop function
Interrupt sources	maskable interrupt sources: • RSPI receive interrupt (receive buffer full) • RSPI transmit interrupt (transmit buffer empty) • RSPI error interrupt (mode fault, overrun, parity error) • RSPI idle interrupt (RSPI idle)	Interrupt sources: • Receive buffer full interrupt • transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, parity error) • RSPI idle interrupt (RSPI idle)
Event link function (output)	The five events can be output to the event link controller: • Receive buffer run event output • Transmit buffer empty event output • Mode fault, overrun, or parity error event output • RSPI idle event output • Transmit end event output	—
Other functions	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode function	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode function
Low power consumption function	It is possible to specify the module stop state.	It is possible to specify the module stop state.

Table 2.43 Comparative Listing of Serial Peripheral Interface Registers

Register	Bit	RX220 (RSPI)	RX130 (RSPIa)
SPCR2	SCKASE	—	RSPCK auto-stop function enable bit
SPSR	SPTEF	—	Transmit Buffer Empty Flag
	SPRF	—	Receive Buffer Full Flag

2.20 12-Bit A/D Converter

Table 2.44 shows a comparative overview of the 12-bit A/D converter specifications, and Table 2.45 shows a comparative listing of the 12-bit A/D converter registers.

Table 2.44 Comparative Overview of 12-Bit A/D Converter

Item	RX220 (S12ADb)	RX130 (S12ADE)
Number of units	1 unit	1 unit
Input channels	16 channels	24 channels
Extended analog function	Internal reference voltage	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	1.56 μs per channel (when operating with A/D conversion clock ADCLK = 32 MHz)	1.4 μs per channel (when operating with A/D conversion clock ADCLK = 32 MHz)
A/D conversion clock	Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the division ratio is one of the following: PCLK: ADCLK division ratio = 1:1, 1:2, 1:4, 1:8, 2:1, 4:1 ADCLK is set using the clock generation circuit.	Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency ratio is one of the following: PCLK: ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.
Data register	• For analog input: 16 data registers • One data register for each unit for A/D conversion data multiplexing in double trigger mode • For internal reference voltage: One data register • 1 register per unit for self-diagnostics • The results of A/D conversion are stored in 12-bit A/D data registers. • In addition mode, A/D conversion results are added and stored in A/D data registers as 14-bit data. Duplication of A/D conversion data • A/D conversion data of one selected analog input channel is stored in A/D data register y when conversion is started by the first trigger and into the duplication register when started by the second trigger.	• For analog input: 24 data registers • One data register for each unit for A/D conversion data multiplexing in double trigger mode • For temperature sensor: One data register • For internal reference voltage: One data register • 1 register per unit for self-diagnostics • The results of A/D conversion are stored in 12-bit A/D data registers. • Output of A/D conversion results at 12-bit precision • The value obtained by adding up A/D-converted results is stored as a value (number of conversion accuracy bits + 2 bits/4 bits) in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes) • The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.

Item	**RX220 (S12ADb)**	**RX130 (S12ADE)**
Data register	• Duplication is available only in double trigger mode in single scan mode or group scan mode.	
Operating mode	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up To 16 user-selected channels. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: — A/D conversion is performed repeatedly on the analog inputs of up to 16 user-selected channels. • Group scan mode: — Up to 16 channels of analog input are divided between group A and group B, and A/D conversion is performed only once on all the channels in the selected group. — The scanning start conditions can be selected independently for group A and group B allowing conversion to start at a different time for each group.	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 24 user-selected channels. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: — A/D conversion is performed repeatedly on the analog inputs of up to 24 user-selected channels. • Group scan mode: — Up to 24 channels of analog input are divided between group A and group B, and A/D conversion is performed only once on all the channels in the selected group. — The scanning start conditions (synchronous triggers) can be selected independently for group A and group B allowing conversion to start at a different time for each group. • Group scan mode (with group A priority control selected): — If a group A trigger is input when A/D conversion on group B is in progress, scanning of group B is stopped and scanning of group A starts. — Restart of A/D conversion on group B (rescan) after completion of A/D conversion on group A can be enabled.
A/D conversion start conditions	• Software trigger • Synchronous trigger Conversion start is triggered by the MTU and ELC. • Asynchronous trigger A/D conversion can be triggered by the ADTRG0# pin.	• Software trigger • Synchronous trigger Conversion start is triggered by the multi-function timer pulse unit (MTU) and event link controller (ELC). • Asynchronous trigger A/D conversion can be started by the external trigger ADTRG0# pin.

Item	RX220 (S12ADb)	RX130 (S12ADE)
Functions	• Sample-and-hold function • Variable sampling state count • Self-diagnostic function for 12-bit A/D converter • Selectable A/D-converted value adding mode • Analog input disconnection detection function • Double trigger mode (duplication of A/D conversion data)	• Sample-and-hold function • Variable sampling state count • Self-diagnostic function for 12-bit A/D converter • Selectable A/D-converted value adding mode or averaging mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • A/D data register auto-clear function • Compare function (window A, window B) • Ring buffers (16) for compare function
Interrupt sources	• In modes other than double trigger mode and group scan mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of a single scan. • In double trigger mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of a double scan. • In group scan mode, a scan end interrupt request (S12ADI0) can be generated on completion of a group A scan. On completion of a group B scan a dedicated group B scan end interrupt request (GBADI) can be generated. • When double trigger mode is selected in group scan mode, a scan end interrupt request (S12ADI0) can be generated on completion of two scans of group A. On completion of a group B scan a dedicated scan end interrupt request (GBADI) can be generated. • The DMA controller (DMAC) or data transfer controller (DTC) can be activated by the S12ADI0 or GBADI interrupt.	• In modes other than double trigger mode and group scan mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of a single scan. • In double trigger mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of a double scan. • In group scan mode, a scan end interrupt request (S12ADI0) can be generated on completion of a group A scan. On completion of a group B scan a dedicated group B scan end interrupt request (GBADI) can be generated. • When double trigger mode is selected in group scan mode, a scan end interrupt request (S12ADI0) can be generated on completion of two scans of group A. On completion of a group B scan a dedicated scan end interrupt request (GBADI) can be generated. • The data transfer controller (DTC) can be activated by the S12ADI0 or GBADI interrupt.

Item	RX220 (S12ADb)	RX130 (S12ADE)
Event link function	• In group scan mode an ELC event can be generated on completion of scans other than group B scan. • Scanning can be started by a trigger from the ELC.	• In group scan mode an ELC event can be generated on completion of scans other than group B scan. • An ELC event can be generated on completion of group B scan in group scan mode. • An ELC event can be generated at end of all scans. • Scanning can be started by a trigger from the ELC. • An ELC event can be generated according to the window compare function event conditions in single scan mode.
Low power consumption function	It is possible to specify the module stop state.	It is possible to specify the module stop state.

Table 2.45 Comparative Listing of 12-Bit A/D Converter Registers

Register	Bit	RX220 (S12ADb)	RX130 (S12ADE)
ADDRy	—	A/D data register y (y = 0 to 15)	A/D data register y (y = 0 to 7, 16 to 21, 24 to 26)
ADTSDR	—	—	A/D temperature sensor register
ADCSR	ADHSC	—	A/D conversion operation select bit
ADANSA	—	A/D channel select register A	—
ADANSB	—	A/D channel select register B	—
ADANSA0	—	—	A/D channel select register A0
ADANSA1	—	—	A/D channel select register A1
ADANSB0	—	—	A/D channel select register B0
ADANSB1	—	—	A/D channel select register B1
ADADS	—	A/D-converted value addition mode select register	—
ADADS0	—	—	A/D-converted value addition/averaging channel select register 0
ADADS1	—	—	A/D-converted value addition/averaging channel select register 1
ADADC	ADC	Addition count select bits (b0, b1)	Addition count select bits (b0 to b2)
	AVEE	—	Average mode enable bit
ADSTRGR	TRSA	A/D conversion start trigger select bit (b8 to b11)	A/D conversion start trigger select bit (b8 to b13)
	TRSB	A/D conversion start trigger for group B select bit (b0 to b3)	A/D conversion start trigger for group B select bit (b0 to b5)
ADEXICR	TSSAD	—	Temperature sensor output A/D-converted value addition/averaging mode select bit
	TSSA	—	Temperature sensor output A/D conversion select bit
	OCS	Internal reference voltage A/D-converted select bit	—

Register	Bit	RX220 (S12ADb)	RX130 (S12ADE)
	OCSA	—	Internal reference voltage A/D-converted select bit
ADSSTR0	—	A/D sampling state register 0 Corresponding Channels: AN000 / self-diagnosis	A/D sampling state register 0 Corresponding Channels: AN000
ADSSTRL	—	A/D sampling state register L Corresponding Channels: AN008 to AN015	A/D sampling state register L Corresponding Channels: AN016 to AN031
ADSSTRT	—	—	A/D sampling state register T Corresponding Channels: Temperature sensor output
ADELCCR	—	—	A/D event link control register
ADGSPCR	—	—	A/D group scan priority control register
ADCMPCR	—	—	A/D compare function control register
ADCMPANSR0	—	—	A/D compare function window A channel select register 0
ADCMPANSR1	—	—	A/D compare function window A channel select register 1
ADCMPANSER	—	—	A/D compare function window A extended input select register
ADCMPLR0	—	—	A/D compare function window A compare condition setting register 0
ADCMPLR1	—	—	A/D compare function window A compare condition setting register 1
ADCMPLER	—	—	A/D compare function window A extended input compare condition setting register
ADCMPDR0	—	—	A/D compare function window A lower-side level setting register
ADCMPDR1	—	—	A/D compare function window A upper-side level setting register
ADCMPSR0	—	—	A/D compare function window A channel status register 0
ADCMPSR1	—	—	A/D compare function window A channel status register 1
ADCMPSER	—	—	A/D compare function window A extended input channel status register
ADHVREFCNT	—	—	A/D high-potential/low-potential reference voltage control register
ADWINMON	—	—	A/D compare function window A/B status monitor register
ADCMPBNSR	—	—	A/D compare function window B channel select register
ADWINLLB	—	—	A/D compare function window B lower-side level setting register
ADWINULB	—	—	A/D compare function window B upper-side level setting register

Register	Bit	RX220 (S12ADb)	RX130 (S12ADE)
ADCMPBSR	—	—	A/D compare function window B channel status register
ADBUFn (n = 0 to 15)	—	—	A/D data storage buffer register n
ADBUFEN	—	—	A/D data storage buffer enable register
ADBUFPTR	—	—	A/D data storage buffer pointer register

2.21 Comparator

Table 2.46 shows a comparative overview of the comparator, and Table 2.47 shows a comparative listing of comparator registers.

Table 2.46 Comparative Overview of Comparator

Item	RX220(CMPA)	RX130(CMPBa)
Analog input voltage	Input voltage to the CMPAn pin (n = 1, 2)	Input voltage to the CMPBn pin (n = 0, 1)
Reference input voltage	Input voltage to the CVREFA pin	Input voltage to the CVREFBn pin (n = 0, 1) or internal reference voltage
Comparison result monitor	LVDnMON bit in the LVDnSR register (n = 1, 2)	Read from the CPBFLG.CPBnOUT flag (n = 0, 1)
Comparison result output	Comparison result can be output from a port by going through the event link controller (ELC).	The comparison result can be output to the CMPOBn pin (n = 0, 1).
Interrupt request generation timing	Input voltage to the CMPA1 pin has risen above or fallen below the CVREFA pin reference input voltage, or either of the two.	When comparator B0 comparison result changes When comparator B1 comparison result changes
Event generation timing to ELC	Input voltage to the CMPA1 pin has risen above or fallen below the CVREFA pin reference input voltage, or either of the two.	When comparator B0 comparison result changes When comparator B0 or comparator B1 comparison result changes
Selectable function	• Digital filter function Whether the digital filter is applied or not, and the sampling frequency can be selected.	• Digital filter function Whether the digital filter is applied or not, and the sampling frequency can be selected. • Window function Whether the window function is enabled or disabled (low-side reference (VRFL)) < CMPBn (n = 0, 1) < high-side reference (VRFH)) can be selected. • Reference input voltage CVREFBn pin input or internal reference voltage (generated internally) can be selected (n = 0, 1). • Comparator B response speed High-speed mode/low-speed mode can be selected.
Low power consumption function	—	Module stop state can be set.

Table 2.47 Comparative Listing of Comparator Registers

Register	Bit	RX220(CMPA)	RX130(CMPBa)
LVD1CR1	—	Voltage Monitoring 1 Circuit/Comparator A1 Control Register 1	—
LVD1SR	—	Voltage Monitoring 1 Circuit/Comparator A1 Status Register	—
LVD2CR1	—	Voltage Monitoring 2 Circuit/Comparator A2 Control Register 1	—
LVD2SR	—	Voltage Monitoring 2 Circuit/Comparator A2 Status Register	—
LVCMPCR	—	Voltage Monitoring Circuit/Comparator A Control Register	—
LVD1CR0	—	Voltage Monitoring 1 Circuit/Comparator A1 Control Register 0	—
LVD2CR0	—	Voltage Monitoring 2 Circuit/Comparator A2 Control Register 0	—
CPBCNT1	—	—	Comparator B Control Register 1
CPBCNT2	—	—	Comparator B Control Register 2
CPBFLG	—	—	Comparator B Flag Register
CPBINT	—	—	Comparator B Interrupt Control Register
CPBF	—	—	Comparator B Filter Select Register
CPBMD	—	—	Comparator B Mode Select Register
CPBREF	—	—	Comparator B Reference Input Voltage Select Register
CPBOCR	—	—	Comparator B Output Control Register

2.22 RAM

Table 2.48 shows a comparative overview of the RAM.

Table 2.48 Comparative Overview of RAM

Item	RX220	RX130
RAM capacity	16 KB, 8 KB, or 4 KB	48 KB, 32 KB, 16 KB or 10 KB
RAM address	0000 0000h to 0000 3FFFh (16 KB) 0000 0000h to 0000 1FFFh (8 KB) 0000 0000h to 0000 0FFFh (4 KB)	0000 0000h to 0000 BFFFh (48 KB) 0000 0000h to 0000 7FFFh (32 KB) 0000 0000h to 0000 3FFFh (16 KB) 0000 0000h to 0000 27FFh (10 KB)
Access	• Single-cycle access is possible for both reading and writing. • The on-chip RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing. • The on-chip RAM can be enabled or disabled.
Low power consumption function	It is possible to specify the module stop state.	It is possible to specify the module stop state.

2.23 Flash Memory (ROM)

Table 2.49 shows a comparative listing of the flash memory specifications and Table 2.50 shows a comparative listing of the flash memory registers.

Table 2.49 Comparative Listing of Flash Memory Specifications

Item	RX220	RX130
Memory space	User area: Maximum 256 KB Data area: 8 KB User boot area: 16 KB	User area: Maximum 512 KB Data area: 8 KB
Value after erase	ROM: FFh E2 data flash: Undefined value	ROM: FFh E2 data flash: FFh
Programming/erasing method	• Unit of programming User area: 2, 8, or 128 bytes Data area: 2 or 8 bytes User boot area: 2, 8, or 128 bytes • Unit of erasing User area: Block units Data area: 128 bytes User boot area: 16 KB	• Unit of programming User area: 4 bytes Data area: 1 byte • Unit of erasing User area: Block units Data area: Block units
On-board programming	• Boot mode SCI1 is used for programming. FINE is used for programming. • User boot mode • Single-chip mode	• Boot mode SCI1 is used for programming. FINE is used for programming. • Single-chip mode
Interrupt	FIFERR and FRDYI	FRDYI
Protect function	Protection based on settings to flash memory–related I/O registers Protection based on lock bits (user area only)	Protection based on settings to flash memory–related I/O registers Area protection
Start-up program protection function	Not supported	Supported
ROM (flash memory for code storage) characteristics	• Reprogramming/erase cycles 10,000 (min.) • Data retention time Up to 1,000 programming/erase cycles: 30 years (min.) Up to 10,000 programming/erase cycles: 1 year (min.)	• Reprogramming/erase cycles 1,000 (min.) • Data retention time Up to 1,000 programming/erase cycles: 20 years (min.)
E2 data flash (flash memory for data storage) characteristics	• Reprogramming/erase cycles 100,000 (min.) • Data retention time Up to 100,000 programming/erase cycles: 30 years (min.)	• Reprogramming/erase cycles 100,000 (min.), 1,000,000 (typ.) • Data retention time Up to 10,000 programming/erase cycles: 20 years (min.) Up to 100,000 programming/erase cycles: 5 years (min.) Up to 1,000,000 programming/erase cycles: 1 year (typ.)

Table 2.50 Comparative Listing of Flash Memory Registers

Register	Bit	RX220	RX130
FWEPROR	—	Flash write erase protection register	—
FMODR	—	Flash mode register	—
FASTAT	—	Flash access status register	—
FAEINT	—	Flash access error interrupt enable register	—
FSTATR0	PRGSPD	Programming suspend status bit	—
	ERSSPD	Erasure suspend status bit	—
	SUSRDY	Suspend ready bit	—
	ERSERR	Erasure error bit	—
	FRDY	Flash ready bit	—
	ERERR	—	Erase error flag
	BCERR	—	Blank check error flag
	EILGLERR	—	Extra area illegal command error flag
FSTATR1	FLOCKST	Lock bit status bit	—
	FCUERR	FCU error bit	—
	DRRDY	—	Data read ready flag
	FRDY	—	Flash ready flag
	EXRDY	—	Extra area ready flag
FRDYIE	—	Flash ready interrupt enable register	—
FPROTR	—	Flash protection register	—
FRESETR	FRESET	Flash reset bit 0: FCU is not reset. 1: FCU is reset.	Flash reset bit 0: Reset of flash control circuit is canceled. 1: Reset of flash control circuit is reset.
	FRKEY[7:0]	Key code	—
FCMDR	—	FCU command register	—
FCPSR	—	FCU processing switching register	—
FPESTAT	—	Flash P/E status register	—
PCKAR	—	Peripheral clock notification register	—
DFLRE0	—	E2 data flash read enable register 0	—
DFLWE0	—	E2 data flash programming/erasure enable register 0	—
DFLBCCNT	—	E2 data flash blank check control register	—
DFLBCSTAT	—	E2 data flash blank check status register	—
DFLCTL	—	—	E2 data flash control register
FPR	—	—	Protection unlock register
FPSR	—	—	Protection unlock status register
FPMCR	—	—	Flash P/E mode control register
FISR	—	—	Flash initial settings register
FASR	—	—	Flash area select register
FCR	—	—	Flash control register
FEXCR	—	—	Flash extra area control register
FSARH	—	—	Flash processing start address register H

Register	Bit	RX220	RX130
FSARL	—	—	Flash processing start address register L
FEARH	—	—	Flash processing end address register H
FEARL	—	—	Flash processing end address register L
FRBH	—	—	Flash read buffer register H
FRBL	—	—	Flash read buffer register L
FWBH	—	—	Flash write buffer register H
FWBL	—	—	Flash write buffer register L
FEAMH	—	—	Flash error address monitor register H
FEAML	—	—	Flash error address monitor register L
FSCMR	—	—	Flash start-up setting monitor register
FAWSMR	—	—	Flash access window start address monitor register
FAWEMR	—	—	Flash access window end address monitor register
UIDRn (n = 0 to 31)	—	—	Unique ID register n

2.24 Flash Memory (E2 Data Flash)

Table 2.51 shows a comparative overview of the flash memory (E2 Data flash) specifications.

Table 2.51 Comparative Overview of Flash Memory (E2 Data Flash) Specifications

Item	RX220	RX130
Memory capacity	8 Kbytes	8 Kbytes
Value after erasure	Undefined	FFh
Block configuration	Block: 128 bytes	Block: 1 Kbytes
Number of blocks	64	8

2.25 Package (LFQFP48/64/100 only)

There are some differences in the outline drawing of the LFQFP48, LFQFP64, LFQFP100 package, so please be careful when designing the board.

For details, refer to Design Guide for Migration between RX Family: Differences in Package External form (R01AN4591EJ).

Table 2.52 Comparison of package codes

Item	RX220	RX130
48 pin LFQFP	PLQP0048KB-A	PLQP0048KB-B
64 pin LFQFP	PLQP0064KB-A	PLQP0064KB-C
100 pin LFQFP	PLQP0100KB-A	PLQP0100KB-B

3. Comparison of Pin Functions

The pin functions are compared below, and a comparative listing of power supply, clock, and system control pins is provided. Items present on only one group are shown in blue. Items with identical specifications on both groups are shown in **black**.

3.1 100-Pin Package

Table 3.1lists the pin functions on products with the 100-pin package.

Table 3.1 Comparison of Pin Functions on 100-Pin Package Products

Pin No.	I/O Port	RX220	RX130
1	P06*1	(Non-Connection)	P06
2	P03	P03	DA0
3	P04*1	(Non-Connection)	P04
4	PJ3	MTIOC3C,CTS6#,RTS6#,SS6#	MTIOC3C,CTS6#,RTS6#,SS6#
5	—	VCL	VCL
6	PJ1	MTIOC3A	MTIOC3A
7	—	MD,FINED	MD,FINED
8	—	XCIN	XCIN
9	—	XCOUT	XCOUT
10	—	RES#	RES#
11	P37	XTAL	XTAL
12	—	VSS	VSS
13	P36	EXTAL	EXTAL
14	—	VCC	VCC
15	P35	NMI	NMI
16	P34	MTIOC0A,TMCI3,POE2#,SCK6,IRQ4	MTIOC0A,TMCI3,POE2#,SCK6,IRQ4
17	P33	MTIOC0D,TMRI3,POE3#,RXD6,SMISO6,SSCL6,IRQ3	MTIOC0D,TMRI3,POE3#,RXD6,SMISO6,SSCL6,IRQ3
18	P32	MTIOC0C,TMO3,TXD6,SMOSI6,SSDA6,IRQ2,RTCOUT	MTIOC0C,TMO3,TXD6,SMOSI6,SSDA6,TS0,IRQ2,RTCOUT
19	P31	MTIOC4D,TMCI2,CTS1#,RTS1#,SS1#,IRQ1	MTIOC4D,TMCI2,CTS1#,RTS1#,SS1#,TS1,IRQ1
20	P30	MTIOC4B,TMRI3,POE8#,RXD1,SMISO1,SSCL1,IRQ0	MTIOC4B,POE8#,TMRI3,RXD1,SMISO1,SSCL1,TS2,IRQ0
21	P27	MTIOC2B,TMCI3,SCK1	MTIOC2B,TMCI3,SCK1,TS3
22	P26	MTIOC2A,TMO1,TXD1,SMOSI1,SSDA1	MTIOC2A,TMO1,TXD1,SMOSI1,SSDA1,TS4
23	P25	MTIOC4C,MTCLKB,ADTRG0#	MTIOC4C,MTCLKB,ADTRG0#
24	P24	MTIOC4A,MTCLKA,TMRI1	MTIOC4A,MTCLKA,TMRI1
25	P23	MTIOC3D,MTCLKD	MTIOC3D,MTCLKD,CTS0#,RTS0#,SS0#
26	P22	MTIOC3B,MTCLKC,TMO0	MTIOC3B,MTCLKC,TMO0,SCK0
27	P21	MTIOC1B,TMCI0	MTIOC1B,TMCI0,RXD0,SMISO0,SSCL0
28	P20	MTIOC1A,TMRI0	MTIOC1A,TMRI0,TXD0,SMOSI0,SSDA0
29	P17	MTIOC3A,MTIOC3B,TMO1,POE8#,SCK1,MISOA,SDA,IRQ7, (5V tolerant)	MTIOC3A,MTIOC3B,TMO1,POE8#,SCK1,MISOA,SDA0,IRQ7, (5V tolerant)
30	P16	MTIOC3C,MTIOC3D,TMO2,TXD1,SMOSI1,SSDA1,MOSIA,SCL,IRQ6,RTCOUT,ADTRG0#, (5V tolerant)	MTIOC3C,MTIOC3D,TMO2,TXD1,SMOSI1,SSDA1,MOSIA,SCL0,IRQ6,RTCOUT,ADTRG0#, (5V tolerant)
31	P15	MTIOC0B,MTCLKB,TMCI2,RXD1,SMISO1,SSCL1,IRQ5	MTIOC0B,MTCLKB,TMCI2,RXD1,SMISO1,SSCL1,TS5,IRQ5

Pin No.	I/O Port	RX220	RX130
32	P14	MTIOC3A,MTCLKA,TMRI2,CTS1#,RTS1#,SS1#,IRQ4	MTIOC3A,MTCLKA,TMRI2,CTS1#,RTS1#,SS1#,TS6,IRQ4
33	P13	MTIOC0B,TMO3,SDA,IRQ3, (5V tolerant)	MTIOC0B,TMO3,SDA0,IRQ3, (5V tolerant)
34	P12	TMCI1,SCL,IRQ2, (5V tolerant)	TMCI1,SCL0,IRQ2, (5V tolerant)
35	PH3	TMCI0	TMCI0,TS7
36	PH2	TMRI0,IRQ1	TMRI0,TS8,IRQ1
37	PH1	TMO0,IRQ0	TMO0,TS9,IRQ0
38	PH0	CACREF	TS10,CACREF
39	P55	MTIOC4D,TMO3	MTIOC4D,TMO3,TS11
40	P54	MTIOC4B,TMCI1	MTIOC4B,TMCI1,TS12
41	P53	P53	P53
42	P52	P52	PMC1
43	P51	P51	PMC0
44	P50	P50	P50
45	PC7	MTIOC3A,TMO2,MTCLKB,MISOA,CACREF	MTIOC3A,TMO2,MTCLKB,TXD8,SMOSI8,SSDA8,MISOA,TS13,CACREF
46	PC6	MTIOC3C,MTCLKA,TMCI2,MOSIA	MTIOC3C,MTCLKA,TMCI2,RXD8,SMISO8,SSCL8,MOSIA,TS14
47	PC5	MTIOC3B,MTCLKD,TMRI2,RSPCKA	MTIOC3B,MTCLKD,TMRI2,SCK8,RSPCKA,TS15
48	PC4	MTIOC3D,MTCLKC,TMCI1,POE0#,SCK5,SSLA0	MTIOC3D,MTCLKC,TMCI1,POE0#,SCK5,CTS8#,RTS8#,SS8#,SSLA0,TSCAP
49	PC3	MTIOC4D,TXD5,SMOSI5,SSDA5,IRTXD5	MTIOC4D,TXD5,SMOSI5,SSDA5,TS16
50	PC2	MTIOC4B,RXD5,SMISO5,SSCL5,IRRXD5,SSLA3	MTIOC4B,RXD5,SMISO5,SSCL5,SSLA3,TS17
51	PC1	MTIOC3A,SCK5,SSLA2	MTIOC3A,SCK5,SSLA2
52	PC0	MTIOC3C,CTS5#,RTS5#,SS5#,SSLA1	MTIOC3C,CTS5#,RTS5#,SS5#,SSLA1
53	PB7	MTIOC3B,TXD9,SMOSI9,SSDA9	MTIOC3B,TXD9,SMOSI9,SSDA9,TS18
54	PB6	MTIOC3D,RXD9,SMISO9,SSCL9	MTIOC3D,RXD9,SMISO9,SSCL9,TS19
55	PB5	MTIOC2A,MTIOC1B,TMRI1,POE1#,SCK9	MTIOC2A,MTIOC1B,TMRI1,POE1#,SCK9,TS20
56	PB4	CTS9#,RTS9#,SS9#	CTS9#,RTS9#,SS9#,TS21
57	PB3	MTIOC0A,MTIOC4A,TMO0,POE3#,SCK6	MTIOC0A,MTIOC4A,TMO0,POE3#,SCK6,TS22
58	PB2	CTS6#,RTS6#,SS6#	CTS6#,RTS6#,SS6#,TS23
59	PB1	MTIOC0C,MTIOC4C,TMCI0,TXD6,SMOSI6,SSDA6,IRQ4	MTIOC0C,MTIOC4C,TMCI0,TXD6,SMOSI6,SSDA6,TS24,IRQ4,CMPOB1
60	—	VCC	VCC
61	PB0	MTIC5W,RXD6,SMISO6,SSCL6,RSPCKA	MTIC5W,RXD6,SMISO6,SSCL6,RSPCKA,TS25
62	—	VSS	VSS
63	PA7	MISOA	MISOA
64	PA6	MTIC5V,MTCLKB,TMCI3,POE2#,CTS5#,RTS5#,SS5#,MOSIA	MTIC5V,MTCLKB,TMCI3,POE2#,CTS5#,RTS5#,SS5#,MOSIA,TS26
65	PA5	RSPCKA	RSPCKA,TS27
66	PA4	MTIC5U,MTCLKA,TMRI0,TXD5,SMOSI5,SSDA5,IRTXD5,SSLA0,IRQ5	MTIC5U,MTCLKA,TMRI0,TXD5,SMOSI5,SSDA5,SSLA0,TS28,IRQ5,CVREFB1
67	PA3	MTIOC0D,MTCLKD,RXD5,SMISO5,SSCL5,IRRXD5,IRQ6	MTIOC0D,MTCLKD,RXD5,SMISO5,SSCL5,TS29,IRQ6,CMPB1

Pin No.	I/O Port	RX220	RX130
68	PA2	RXD5,SMISO5,SSCL5,IRRXD5,SSLA3	RXD5,SMISO5,SSCL5,SSLA3,TS30
69	PA1	MTIOC0B,MTCLKC,SCK5,SSLA2,CVREFA	MTIOC0B,MTCLKC,SCK5,SSLA2,TS31
70	PA0	MTIOC4A,SSLA1,CACREF	MTIOC4A,SSLA1,TS32,CACREF
71	PE7	IRQ7,AN015	IRQ7,AN023
72	PE6	IRQ6,AN014	IRQ6,AN022
73	PE5	MTIOC4C,MTIOC2B,IRQ5,AN013	MTIOC4C,MTIOC2B,IRQ5,AN021,CMPOB0
74	PE4	MTIOC4D,MTIOC1A,AN012,CMPA2	MTIOC4D,MTIOC1A,TS33,AN020,CMPA2,CLKOUT
75	PE3	MTIOC4B,POE8#,CTS12#,RTS12#,SS12#,AN011,CMPA1	MTIOC4B,POE8#,CTS12#,RTS12#,SS12#,TS34,AN019,CLKOUT
76	PE2	MTIOC4A,RXD12,RXDX12,SMISO12,SSCL12,IRQ7,AN010	MTIOC4A,RXD12,RXDX12,SMISO12,SSCL12,TS35,IRQ7,AN018,CVREFB0
77	PE1	MTIOC4C,TXD12,TXDX12,SIOX12,SMOSI12,SSDA12,AN009	MTIOC4C,TXD12,TXDX12,SIOX12,SMOSI12,SSDA12,AN017,CMPB0
78	PE0	SCK12,AN008	SCK12,AN016
79	PD7	MTIC5U,POE0#,IRQ7	MTIC5U,POE0#,IRQ7,AN031
80	PD6	MTIC5V,POE1#,IRQ6	MTIC5V,POE1#,IRQ6,AN030
81	PD5	MTIC5W,POE2#,IRQ5	MTIC5W,POE2#,IRQ5,AN029
82	PD4	POE3#,IRQ4	POE3#,IRQ4,AN028
83	PD3	POE8#,IRQ3	POE8#,IRQ3,AN027
84	PD2	MTIOC4D,IRQ2	MTIOC4D,SCK6,IRQ2,AN026
85	PD1	MTIOC4B,IRQ1	MTIOC4B,RXD6,SMISO6,SSCL6,IRQ1,AN025
86	PD0	IRQ0	TXD6,SMOSI6,SSDA6,IRQ0,AN024
87	P47	AN007	AN007
88	P46	AN006	AN006
89	P45	AN005	AN005
90	P44	AN004	AN004
91	P43	AN003	AN003
92	P42	AN002	AN002
93	P41	AN001	AN001
94	PJ7*1	VREFL0	VREFL0
95	P40	AN000	AN000
96	PJ6*1	VREFH0	VREFH0
97	—	AVCC0	AVCC0
98	P07	ADTRG0#	ADTRG0#
99	—	AVSS0	AVSS0
100	P05	P05	DA1

Note 1. I/O port implemented on the RX130 only. Not implemented on the RX220.

3.2 64-Pin Package

Table 3.2 lists the pin functions on products with the 64-pin package.

Table 3.2 Comparison of Pin Functions on 64-Pin Package Products

Pin No.	I/O Port	RX220	RX130
1	P03		DA0
2	—	VCL	VCL
3	—	MD, FINED	MD, FINED
4	—	XCIN	XCIN
5	—	XCOUT	XCOUT
6	—	RES#	RES#
7	P37	XTAL	XTAL
8	—	VSS	VSS
9	P36	EXTAL	EXTAL
10	—	VCC	VCC
11	P35	NMI	NMI
12	P32	MTIOC0C, TMO3, RTCOUT, TXD6, SMOSI6, SSDA6, IRQ2	MTIOC0C, TMO3, RTCOUT, TXD6, SMOSI6, SSDA6, IRQ2, TS0
13	P31	MTIOC4D, TMCI2, CTS1#, RTS1#, SS1#, IRQ1	MTIOC4D, TMCI2, CTS1#, RTS1#, SS1#, IRQ1, TS1
14	P30	MTIOC4B, TMRI3, POE8#, RXD1, SMISO1, SSCL1, IRQ0	MTIOC4B, TMRI3, POE8#, RXD1, SMISO1, SSCL1, IRQ0, TS2
15	P27	MTIOC2B, TMCI3, SCK1	MTIOC2B, TMCI3, SCK1, TS3
16	P26	MTIOC2A, TMO1, TXD1, SMOSI1, SSDA1	MTIOC2A, TMO1, TXD1, SMOSI1, SSDA1, TS4
17	P17	MTIOC3A, MTIOC3B, TMO1, POE8#, SCK1, MISOA, SDA, IRQ7, (5V tolerant)	MTIOC3A, MTIOC3B, TMO1, POE8#, SCK1, MISOA, SDA, IRQ7, (5V tolerant)
18	P16	MTIOC3C, MTIOC3D, TMO2, TXD1, SMOSI1, SSDA1, MOSIA, SCL, IRQ6, RTCOUT, ADTRG0#, (5V tolerant)	MTIOC3C, MTIOC3D, TMO2, TXD1, SMOSI1, SSDA1, MOSIA, SCL, IRQ6, RTCOUT, ADTRG0#, (5V tolerant)
19	P15	MTIOC0B, MTCLKB, TMCI2, RXD1, SMISO1, SSCL1, IRQ5	MTIOC0B, MTCLKB, TMCI2, RXD1, SMISO1, SSCL1, IRQ5, TS5
20	P14	MTIOC3A, MTCLKA, TMRI2, CTS1#, RTS1#, SS1#, IRQ4	MTIOC3A, MTCLKA, TMRI2, CTS1#, RTS1#, SS1#, IRQ4, TS6
21	PH3	TMCI0	TMCI0, TS7
22	PH2	TMRI0, IRQ1	TMRI0, IRQ1, TS8
23	PH1	TMO0, IRQ0	TMO0, IRQ0, TS9
24	PH0	CACREF	CACREF, TS10
25	P55	MTIOC4D, TMO3	MTIOC4D, TMO3, TS11
26	P54	MTIOC4B, TMCI1	MTIOC4B, TMCI1, TS12
27	PC7	MTIOC3A, TMO2, MTCLKB, MISOA, CACREF	MTIOC3A, TMO2, MTCLKB, MISOA, CACREF, TS13
28	PC6	MTIOC3C, MTCLKA, TMCI2, MOSIA	MTIOC3C, MTCLKA, TMCI2, MOSIA, TS14
29	PC5	MTIOC3B, MTCLKD, TMRI2, RSPCKA	MTIOC3B, MTCLKD, TMRI2, RSPCKA, TS15
30	PC4	MTIOC3D, MTCLKC, TMCI1, POE0#, SCK5, SSLA0	MTIOC3D, MTCLKC, TMCI1, POE0#, SCK5, SSLA0, TSCAP
31	PC3	MTIOC4D, TXD5, SMOSI5, SSDA5, IRTXD5	MTIOC4D, TXD5, SMOSI5, SSDA5, TS16
32	PC2	MTIOC4B, RXD5, SMISO5, SSCL5, IRRXD5, SSLA3	MTIOC4B, RXD5, SMISO5, SSCL5, SSLA3, TS17

Pin No.	I/O Port	RX220	RX130
33	PB7/ PC1	MTIOC3B, TXD9, SMOSI9, SSDA9	MTIOC3B, TS18
34	PB6/ PC0	MTIOC3D, RXD9, SMISO9, SSCL9	MTIOC3D, TS19
35	PB5	MTIOC2A, MTIOC1B, TMRI1, POE1#, SCK9	MTIOC2A, MTIOC1B, TMRI1, POE1#, TS20
36	PB3	MTIOC0A, MTIOC4A, TMO0, POE3#, SCK6	MTIOC0A, MTIOC4A, TMO0, POE3#, SCK6, TS22
37	PB1	MTIOC0C, MTIOC4C, TMCI0, TXD6, SMOSI6, SSDA6, IRQ4	MTIOC0C, MTIOC4C, TMCI0, TXD6, SMOSI6, SSDA6, IRQ4, TS24, CMPOB1
38	—	VCC	VCC
39	PB0	MTIC5W, RXD6, SMISO6, SSCL6, RSPCKA	MTIC5W, RXD6, SMISO6, SSCL6, RSPCKA, TS25
40	—	VSS	VSS
41	PA6	MTIC5V, MTCLKB, TMCI3, POE2#, CTS5#, RTS5#, SS5#, MOSIA	MTIC5V, MTCLKB, TMCI3, POE2#, CTS5#, RTS5#, SS5#, MOSIA, TS26
42	PA4	MTIC5U, MTCLKA, TMRI0, TXD5, SMOSI5, SSDA5, IRTXD5, SSLA0, IRQ5	MTIC5U, MTCLKA, TMRI0, TXD5, SMOSI5, SSDA5, SSLA0, IRQ5, TS28, CVREFB1
43	PA3	MTIOC0D, MTCLKD, RXD5, SMISO5, SSCL5, IRRXD5, IRQ6	MTIOC0D, MTCLKD, RXD5, SMISO5, SSCL5, IRQ6, TS29, CMPB1
44	PA1	MTIOC0B, MTCLKC, SCK5, SSLA2, CVREFA	MTIOC0B, MTCLKC, SCK5, SSLA2, TS31
45	PA0	MTIOC4A, SSLA1, CACREF	MTIOC4A, SSLA1, CACREF, TS32
46	PE5	MTIOC4C, MTIOC2B, IRQ5, AN013	MTIOC4C, MTIOC2B, IRQ5, AN021, CMPOB0
47	PE4	MTIOC4D, MTIOC1A, AN012, CMPA2	MTIOC4D, MTIOC1A, AN020, CMPA2, CLKOUT, TS33
48	PE3	MTIOC4B, POE8#, CTS12#, RTS12#, SS12#, AN011, CMPA1	MTIOC4B, POE8#, CTS12#, RTS12#, SS12#, AN019, CLKOUT, TS34
49	PE2	MTIOC4A, RXD12, RXDX12, SMISO12, SSCL12, IRQ7, AN010	MTIOC4A, RXD12, RXDX12, SMISO12, SSCL12, IRQ7, AN018, CVREFB0, TS35
50	PE1	MTIOC4C, TXD12, TXDX12, SIOX12, SMOSI12, SSDA12, AN009	MTIOC4C, TXD12, TXDX12, SIOX12, SMOSI12, SSDA12, AN017, CMPB0
51	PE0	SCK12, AN008	SCK12, AN016
52	P47*1	(Non-Connection)	AN007
53	P46	AN006	AN006
54	P45*1	(Non-Connection)	AN005
55	P44	AN004	AN004
56	P43	AN003	AN003
57	P42	AN002	AN002
58	P41	AN001	AN001
59	PJ7*1	VREFL0	VREFL0
60	P40	AN000	AN000
61	PJ6*1	VREFH0	VREFH0
62	—	AVCC0	AVCC0
63	P05	—	DA1
64	—	AVSS0	AVSS0

Note 1. I/O port implemented on the RX130 only. Not implemented on the RX220.

3.3 48-Pin Package

Table 3.3 lists the pin functions on products with the 48-pin package.

Table 3.3 Comparison of Pin Functions on 48-Pin Package Products

Pin No.	I/O Port	RX220	RX130
1	—	VCL	VCL
2	—	MD, FINED	MD, FINED
3	—	RES#	RES#
4	P37	XTAL	XTAL
5	—	VSS	VSS
6	P36	EXTAL	EXTAL
7	—	VCC	VCC
8	P35	NMI	NMI
9	P31	MTIOC4D, TMCI2, CTS1#, RTS1#, SS1#, IRQ1	MTIOC4D, TMCI2, CTS1#, RTS1#, SS1#, IRQ1, TS1
10	P30	MTIOC4B, TMRI3, POE8#, RXD1, SMISO1, SSCL1, IRQ0	MTIOC4B, TMRI3, POE8#, RXD1, SMISO1, SSCL1, IRQ0, TS2
11	P27	MTIOC2B, TMCI3, SCK1	MTIOC2B, TMCI3, SCK1, TS3
12	P26	MTIOC2A, TMO1, TXD1, SMOSI1, SSDA1	MTIOC2A, TMO1, TXD1, SMOSI1, SSDA1, TS4
13	P17	MTIOC3A, MTIOC3B, TMO1, POE8#, SCK1, MISOA, SDA, IRQ7, (5V tolerant)	MTIOC3A, MTIOC3B, TMO1, POE8#, SCK1, MISOA, SDA, IRQ7, (5V tolerant)
14	P16	MTIOC3C, MTIOC3D, TMO2, TXD1, SMOSI1, SSDA1, MOSIA, SCL, IRQ6, ADTRG0#, (5V tolerant)	MTIOC3C, MTIOC3D, TMO2, TXD1, SMOSI1, SSDA1, MOSIA, SCL, IRQ6, ADTRG0#, (5V tolerant)
15	P15	MTIOC0B, MTCLKB, TMCI2, RXD1, SMISO1, SSCL1, IRQ5	MTIOC0B, MTCLKB, TMCI2, RXD1, SMISO1, SSCL1, IRQ5, TS5
16	P14	MTIOC3A, MTCLKA, TMRI2, CTS1#, RTS1#, SS1#, IRQ4	MTIOC3A, MTCLKA, TMRI2, CTS1#, RTS1#, SS1#, IRQ4, TS6
17	PH3	TMCI0	TMCI0, TS7
18	PH2	TMRI0, IRQ1	TMRI0, IRQ1, TS8
19	PH1	TMO0, IRQ0	TMO0, IRQ0, TS9
20	PH0	CACREF	CACREF, TS10
21	PC7	MTIOC3A, TMO2, MTCLKB, MISOA, CACREF	MTIOC3A, TMO2, MTCLKB, MISOA, CACREF, TS13
22	PC6	MTIOC3C, MTCLKA, TMCI2, MOSIA	MTIOC3C, MTCLKA, TMCI2, MOSIA, TS14
23	PC5	MTIOC3B, MTCLKD, TMRI2, RSPCKA	MTIOC3B, MTCLKD, TMRI2, RSPCKA, TS15
24	PC4	MTIOC3D, MTCLKC, TMCI1, POE0#, SCK5, SSLA0	MTIOC3D, MTCLKC, TMCI1, POE0#, SCK5, SSLA0, TSCAP
25	PB5/ PC3	MTIOC2A, MTIOC1B, TMRI1, POE1#	MTIOC2A, MTIOC1B, TMRI1, POE1#, TS20
26	PB3/ PC2	MTIOC0A, MTIOC4A, TMO0, POE3#, SCK6	MTIOC0A, MTIOC4A, TMO0, POE3#, SCK6, TS22
27	PB1/ PC1	MTIOC0C, MTIOC4C, TMCI0, TXD6, SMOSI6, SSDA6, IRQ4	MTIOC0C, MTIOC4C, TMCI0, TXD6, SMOSI6, SSDA6, IRQ4, CMPOB1, TS24
28		VCC	VCC
29	PB0/ PC0	MTIC5W, RXD6, SMISO6, SSCL6, RSPCKA	MTIC5W, RXD6, SMISO6, SSCL6, RSPCKA, TS25
30	—	VSS	VSS

Pin No.	I/O Port	RX220	RX130
31	PA6	MTIC5V, MTCLKB, TMCI3, POE2#, CTS5#, RTS5#, SS5#, MOSIA	MTIC5V, MTCLKB, TMCI3, POE2#, CTS5#, RTS5#, SS5#, MOSIA, TS26
32	PA4	MTIC5U, MTCLKA, TMRI0, TXD5, SMOSI5, SSDA5, IRTXD5, SSLA0, IRQ5	MTIC5U, MTCLKA, TMRI0, TXD5, SMOSI5, SSDA5, SSLA0, IRQ5, TS28, CVREFB1
33	PA3	MTIOC0D, MTCLKD, RXD5, SMISO5, SSCL5, IRRXD5, IRQ6	MTIOC0D, MTCLKD, RXD5, SMISO5, SSCL5, IRQ6, TS29, CMPB1
34	PA1	MTIOC0B, MTCLKC, SCK5, SSLA2, CVREFA	MTIOC0B, MTCLKC, SCK5, SSLA2, TS31
35	PE4	MTIOC4D, MTIOC1A, AN012, CMPA2	MTIOC4D, MTIOC1A, AN020, CMPA2, CLKOUT, TS33
36	PE3	MTIOC4B, POE8#, CTS12#, RTS12#, AN011, CMPA1	MTIOC4B, POE8#, CTS12#, RTS12#, AN019, CLKOUT, TS34
37	PE2	MTIOC4A, RXD12, RXDX12, SSCL12, IRQ7, AN010	MTIOC4A, RXD12, RXDX12, SSCL12, IRQ7, AN018, CVREFB0, TS35
38	PE1	MTIOC4C, TXD12, TXDX12, SIOX12, SSDA12, AN009	MTIOC4C, TXD12, TXDX12, SIOX12, SSDA12, AN017, CMPB0
39	P47*1	(Non-Connection)	AN007
40	P46	AN006	AN006
41	P45*1	(Non-Connection)	AN005
42	P42	AN002	AN002
43	P41	AN001	AN001
44	PJ7*1	VREFL0	VREFL0
45	P40	AN000	AN000
46	PJ6*1	VREFH0	VREFH0
47	—	AVCC0	AVCC0
48	—	AVSS0	AVSS0

Note 1. I/O port implemented on the RX130 only. Not implemented on the RX220.

4. Notes on Migration

When migrating from the RX220 Group to the RX130 Group, a few points need to be considered with regard to hardware and software.

The points related to hardware are covered in 4.1, Important Points Regarding Pin Design, and the points related to software are covered in 4.2, Important Points Regarding Function Settings.

4.1 Important Points Regarding Pin Design

The RX220 Group and RX130 Group are pin compatible to enable easy migration, but some pins need to be handled differently because the product series are different.

4.1.1 Power Supply Pin

The upper limit of the operating frequency range differs between the RX220 Group and RX130 Group, depending on the voltage (Vcc) applied to the power supply pin. Make sure to use the power supply voltage that is appropriate for the operating frequency.

Table 4.1 Power Supply Voltage and Operating Frequency

MCU	Power Supply Voltage/Operating Frequency		
RX220	1.62 V to 2.7 V / 8 MHz		2.7 V to 5.5 V / 32 MHz
RX130	1.8 V to 2.4 V / 8 MHz	2.4 V to 2.7 V / 16 MHz	

4.1.2 Main Clock Oscillator

When VCC ≥ 2.4 V, the connectable main clock frequency range of the RX130 Group is the same as that for the RX220 Group (1 MHz to 20 MHz). However, when VCC < 2.4 V, the main clock frequency of the RX130 Group is limited to a range of 1 MHz to 8 MHz.

4.1.3 VCL Pin (External Capacitor)

To stabilize the internal power supply, connect a smoothing capacitor to the VCL pin. For the RX220 Group use a smoothing capacitor rated at 0.1 µF, and for the RX130 Group use a smoothing capacitor rated at 4.7 µF.

4.1.4 Mode Setting Pin

On the RX220 Group the MD pin and PC7 pin are used to specify the mode after a reset, but on the RX130 Group only the MD pin is used for this purpose.

4.1.5 General-Purpose I/O Ports

Care must be exercised on the RX220 Group with ports P40 to P47, and on the RX130 Group with ports P03 to P07, P40 to P47, PJ6, and PJ7, because these I/O ports are dependent on AVCC. When they will not be used, these pins should be set as inputs and individually connected to AVCC via a resistor (pull-up), or they should be individually connected to VSS via a resistor (pull-down). Alternatively, they can be set as outputs and left open.

A pin that is set as an output and left open will be set as an input immediately after a reset, and the pin’s voltage level will be unstable for the period it is set as an input. This can cause in increase in the power supply current.

4.1.6 Analog Input Pins

It is necessary to change references to the eight channels assigned to pins AN008 to AN015 on the RX220 Group to channels among the nine assigned to pins AN016 to AN021 and AN024 to AN026 on the RX130 Group.

Refer to 4.2.5, 12-Bit A/D Converter, regarding software related to analog inputs.

4.1.7 Analog Pins for Comparator A1

The PE3/CMPA1 pin and comparator A function of the RX220 Group are not implemented on the RX130 Group. The PE4/CMPA2 pin can be used as a detection target for the voltage detection 2 voltage detection circuit, but the functionality of comparator A2 differs from that of comparator A.

Change references to the PE3/CMPA1 pin of comparator A1 on the RX220 Group to the PA3/CMPB1 pin of comparator B on the RX130 Group.

4.2 Important Points Regarding Function Settings

Software that runs on the RX220 Group is highly compatible with RX130 Group software. Nevertheless, careful evaluation is needed to accommodate differences in certain aspects, such as operation timing and electrical characteristics.

Some important points regarding function settings in software for the RX220 Group and RX130 Group are described below. See 2, Comparative Overview of Functions, for details of the points of difference between modules and functions. These points should be carefully evaluated when making use of this application note.

4.2.1 Option-Setting Memory

The settings details for the IWDT timeout period select bits (IWDTTOPS[1:0]) in option function select register 0 (OFS0) and the voltage detection 0 level select bits (VDSEL[1:0]) in option function select register 1 (OFS1) in the flash memory differ between the RX220 Group and RX130 Group. Make sure to change the settings to appropriate values.

See 2.3, Option-Setting Memory for the points of difference. For details, refer to User’s Manual: Hardware in 5, Reference Documents.

4.2.2 User Boot Mode

The RX220 Group has a user boot mode, but UB code A, UB code B, and user boot mode are not implemented on the RX130 Group.

As a substitute for user boot mode, on the RX130 Group it is possible to use the startup program protection function to program and read the user and data areas of the flash memory via a user-defined interface. For details, refer to the Startup Program Protection Function section in User’s Manual: Hardware, listed in 5, Reference Documents.

4.2.3 Clock Generator Circuit

The RX130 Group has a PLL circuit, but no PLL circuit is implemented on the RX220 Group. On the RX130 Group the PLL circuit supports selection of multiplication factors from 4× to 8× (in increments of 0.5×) to generate a PLL oscillation frequency of 24 MHz to 32 MHz (VCC ≥ 2.4V), without frequency division. To use the PLL circuit, change these settings as appropriate.

In addition, the on-chip oscillator generation frequencies of the RX130 Group differ from those of the RX220 Group. The different generation frequencies are listed below.

Table 4.2 On-Chip Oscillator and Operating Frequency

On-Chip Oscillator	RX220	RX130
High-speed on-chip oscillator (HOCO)	32 MHz, 36.864 MHz, 40 MHz, or 50 MHz	32 MHz
Low-speed on-chip oscillator (LOCO)	125 kHz	4 MHz
IWDT-dedicated on-chip oscillator	125 kHz	15 kHz

For points of difference, see 2.5, Clock Generation Circuit. For details, refer to User's Manual: Hardware in 5, Reference Documents.

4.2.4 Low Power Consumption Functions

Change references to the all-module clock stop mode of the RX220 Group to deep sleep mode on the RX130 Group. Deep sleep mode provides power consumption equivalent to all-module clock stop mode.

Change the references to the operating power control modes to the following three modes:

- High-speed operating mode
- Middle-speed operating mode
- Low-speed operating mode

For points of difference, see 2.7, Low Power Consumption Functions. For details, refer to User's Manual: Hardware in 5, Reference Documents.

4.2.5 12-Bit A/D Converter

The functions of the 12-bit A/D converter have been enhanced on the RX130 Group, and the number of I/O registers used has increased. Also, change references in software to the eight channels assigned to pins AN008 to AN015 on the RX220 Group to channels among the nine assigned to pins AN016 to AN021 and AN024 to AN026 on the RX130 Group.

For points of difference, see 2.20, 12-Bit A/D Converter. For details, refer to the 12-Bit A/D Converter (S12ADE) section in User's Manual: Hardware, listed in 5, Reference Documents.

4.2.6 Comparator A

Comparator A is not implemented on the RX130 Group. Change references to comparator A of the RX220 Group to comparator B (comparator B0 or B1) on the RX130 Group.

For details, refer to User's Manual: Hardware in 5, Reference Documents.

4.2.7 Flash Memory

The flash memory on the RX130 Group has shorter programming and read times, resulting in increased production efficiency, lower power consumption, and reduced production costs for products incorporating it. To realize these benefits, software used for self-programming in single-chip mode on the RX220 Group will require appropriate modifications.

For points of difference related to the flash memory, see 2.23, Flash Memory. For details, refer to User's Manual: Hardware in 5, Reference Documents.

5. Reference Documents

User’s Manual: Hardware

RX220 Group, User’s Manual: Hardware Rev.1.10 (R01UH0292EJ0110)
(The latest version can be downloaded from the Renesas Electronics website.)

RX130 Group User’s Manual: Hardware Rev.3.00 (R01UH0560EJ0300)
(The latest version can be downloaded from the Renesas Electronics website.)

Application Note

Design Guide for Migration between RX Family: Differences in Package External (R01AN4591EJ)
(The latest version can be downloaded from the Renesas Electronics website.)

On-Chip Debugging Emulator

E1/E20 Emulator, E2 Emulator Lite Additional Document for User’s Manual (RX User System Design) (R20UT0399EJ)

Technical Update/Technical News

(The technical updates issued after each referenced user manual are not reflected in this application note, so obtain latest version from the Renesas Electronics website.)

Revision History

Rev.	Date	Description	
		Page	**Summary**
1.00	Dec. 9, 2015	-	First edition issued
1.10	May. 8, 2019	Whole	Correspondence for 512KB and 100pin of RX130 Confirmed the contents of the description again (Addition of description mistake etc.)
		5	Add memory map comparison of address space
		7	Add area comparison of option setting memory
		18	Add Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode
		33	Add comparative listing of functions assigned to each multiplexed pin
		40	Added comparison of pin function control register
		68	Add differences in package external form

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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