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Renesas Electronics Corporation

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H8/300L Super Low Power Series

Multiplication of Signed 16-Bit Binary Numbers (SMUL)

Introduction

The software SMUL multiplies a signed 16-bit binary number to another signed 16-bit binary number and places the result, which is a signed 32-bit binary number, in general-purpose registers.

Target Device

H8/38024

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1. Arguments

Description		Memory area	Data length (bytes)
Input	Multiplicand	R1	2
	Multiplier	R0	2
Output	Result of multiplication	R1, R2	4

2. Changes to Internal Registers and Flags

R0	R1	R2	R3	R4	R5	R6H	R6L	R7
×	○	○	×	×	—	—	×	—

I	U	H	U	N	Z	V	C
—	×	×	×	×	×	×	×

Legend
—: No change
×: Undefined
○: Result

3. Specifications

Program memory (bytes)
52
Data memory (bytes)
0
Stack (bytes)
0
Clock cycle count
132
Reentrant
Possible
Relocation
Possible
Interrupt
Possible

4. Notes

The clock cycle count (132) in the specifications is the maximum cycle count.

5. Description

5.1 Details of functions

1. The following arguments are used with the software SMUL:
   a. Input arguments:
      R0: Sets a signed 16-bit binary multiplier.
      R1: Sets a signed 16-bit binary multiplicand.
   b. Output arguments:
      R1, R2: The result of multiplication (a signed 32-bit binary number) is placed here.
2. The following figure illustrates the execution of the software SMUL. When the input arguments are set as shown in (1), the result of multiplication is placed in R1 and R2 as shown in (2).

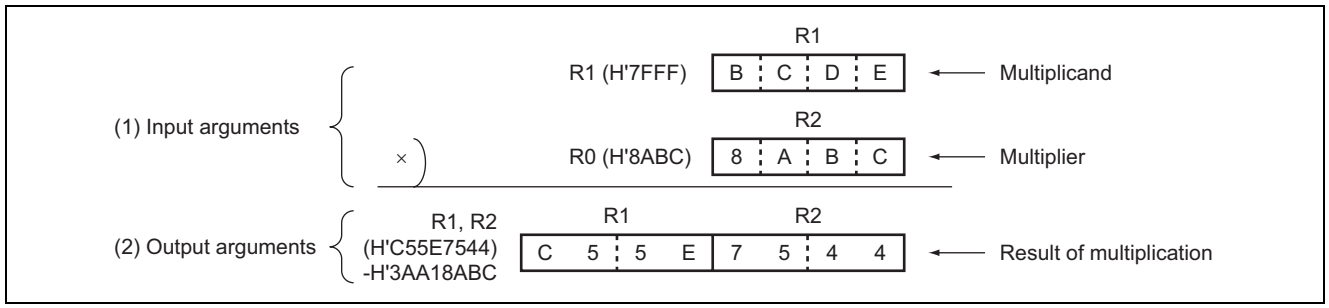


Figure 1 Example of Software SMUL Execution

5.2 Notes on usage

1. When the upper bits are not used as seen in figure 2, set them to 0; otherwise, a correct result cannot be obtained because multiplication is done on the numbers including indeterminate data placed in the upper bits (the upper bits here do not include the sign bit).

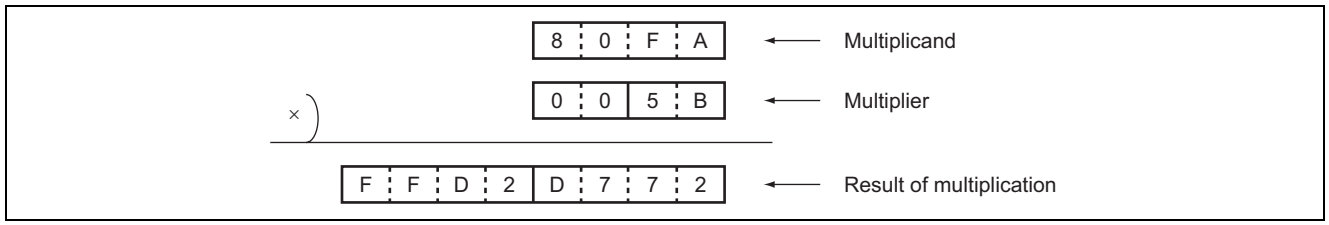


Figure 2 Example of Multiplication with Upper Bits Unused

2. After execution of the software SMUL, the multiplicand will be lost because the upper 2 bytes of the result are placed in R1. If the multiplicand is still needed after software SMUL execution, save it in memory in advance.

5.3 Description of data memory

The software SMUL does not use data memory.

5.4 Example of usage

Set a multiplicand and a multiplier in the input arguments and call the software SMUL as a subroutine.

```
WORK1    . RES. W    1    ---------  Reserves a data memory area in which the user program places
                                     a signed 16-bit binary multiplicand.

WORK2    . RES. W    1    ---------  Reserves a data memory area in which the user program places
                                     a 16-bit binary multiplier.

WORK3    . RES. W    2    ---------  Reserves a data memory area
                                     for storage of the result of multiplication.
             .
             .
             .
         MOV. W      @WORK1, R1   -------  Places in R1 the 16-bit binary multiplicand
                                           set by the user program.

         MOV. W      @WORK2, R0   -------  Places in R0 the 16-bit binary multiplier
                                           set by the user program.

         JSR         @SMUL        -------  Calls the software SMUL as a subroutine.

         MOV. W      R1, @WORK3   -------  Places the result (set in the output argument)
         MOV. W      R2, @WORK3+2          in the data memory of the user program.
             .
             .
             .
```

5.5 Operation

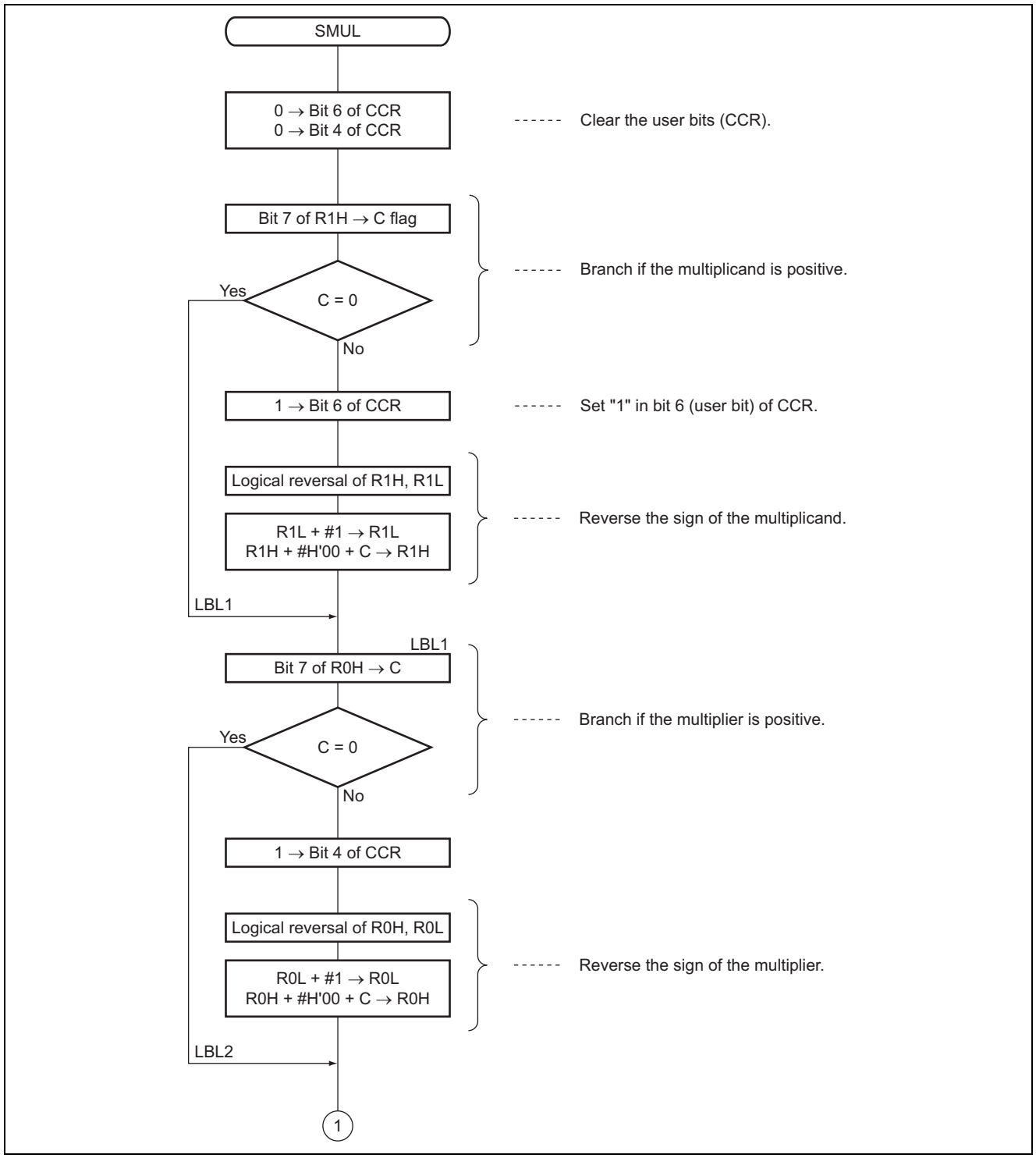
1. Subtraction of signed 16-bit binary numbers is done in one of the following manners depending on the signs of the multiplicand and multiplier:

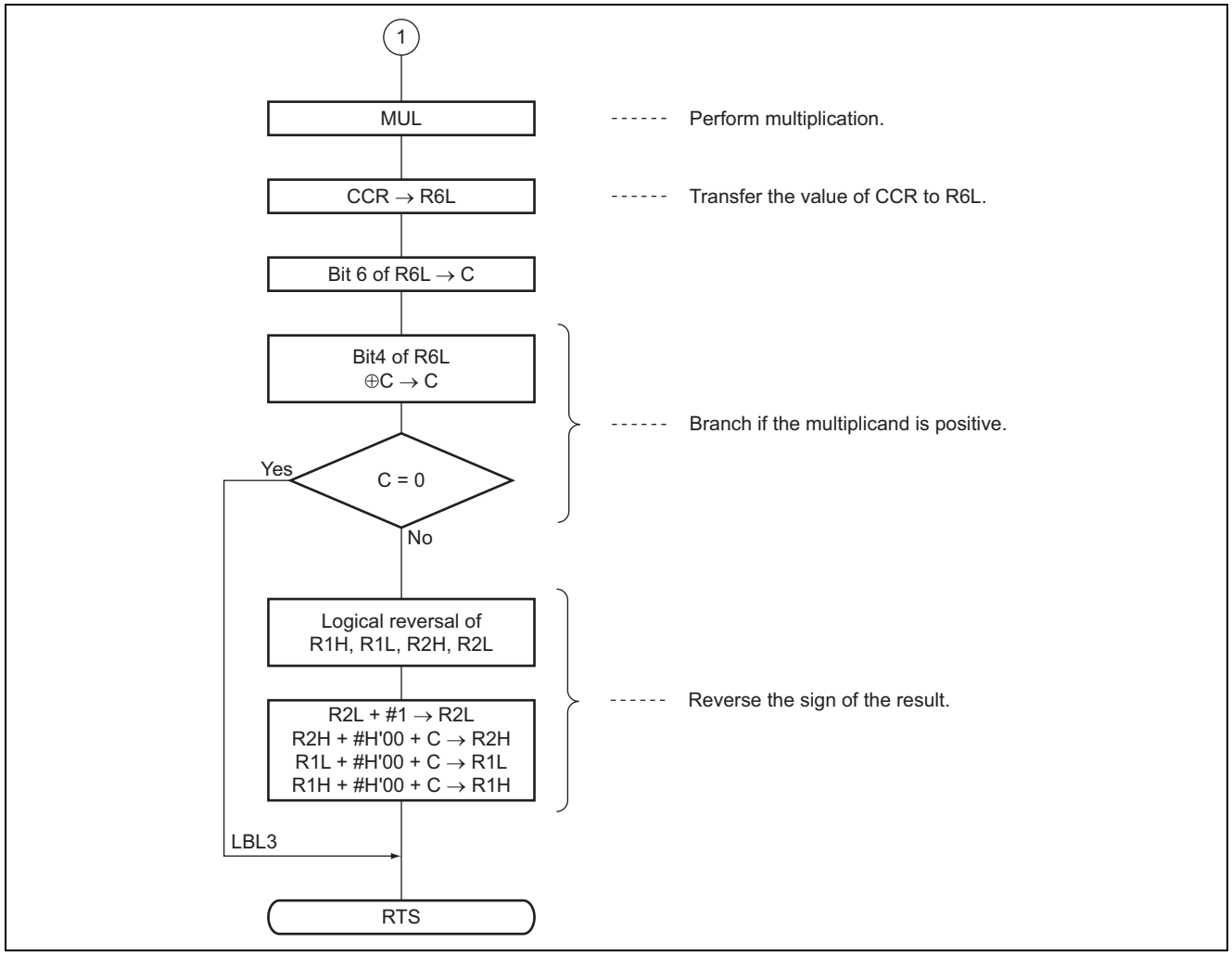
(Multiplicand)	(Multiplier)		(Process)
(+)	(+)	→	Multiplied directly.
(+)	(–)	→	Multiplied with the sign of the multiplier inverted.
(–)	(+)	→	Multiplied with the sign of the multiplicand inverted.
(–)	(–)	→	Multiplied with the signs of both multiplicand and multiplier inverted.

2. The multiplication steps are as follows:
   a. A multiplicand is placed in R1 and a multiplier in R0.
   b. The user bit (CCR) is cleared.
   c. If the multiplicand is negative, its sign is inverted. If the multiplier is negative, its sign bit is inverted. Bits 6 and 4 of the CCR (user bits) are used as the sign bits of the multiplicand and multiplier, respectively. If the multiplicand or multiplier is negative, "1" is set in the corresponding user bit.
   d. Multiplication is done with the software MUL.
   e. The CCR is transferred to R6L.
   f. The result is modified or unmodified depending on the signs of the multiplicand and multiplier, as follows:

(Multiplicand)	(Multiplier)	(Process)
(+)	(+)	→ The result is unmodified.
(+)	(-)	
(-)	(+)	→ The sign of the result is inverted.
(-)	(-)	

6. Flowchart


SMUL
0 → Bit 6 of CCR
0 → Bit 4 of CCR
Clear the user bits (CCR).
Bit 7 of R1H → C flag
C = 0
Yes
No
Branch if the multiplicand is positive.
1 → Bit 6 of CCR
Set "1" in bit 6 (user bit) of CCR.
Logical reversal of R1H, R1L
R1L + #1 → R1L
R1H + #H'00 + C → R1H
Reverse the sign of the multiplicand.
LBL1
LBL1
Bit 7 of R0H → C
C = 0
Yes
No
Branch if the multiplier is positive.
1 → Bit 4 of CCR
Logical reversal of R0H, R0L
R0L + #1 → R0L
R0H + #H'00 + C → R0H
Reverse the sign of the multiplier.
LBL2
1


1
MUL
CCR → R6L
Bit 6 of R6L → C
Bit4 of R6L
⊕C → C
Yes
C = 0
No
Logical reversal of
R1H, R1L, R2H, R2L
R2L + #1 → R2L
R2H + #H'00 + C → R2H
R1L + #H'00 + C → R1L
R1H + #H'00 + C → R1H
LBL3
RTS
------ Perform multiplication.
------ Transfer the value of CCR to R6L.
------ Branch if the multiplicand is positive.
------ Reverse the sign of the result.

7. Program List

```
*** H8/300 ASSEMBLER VER 1.0B ** 08/18/92 10:16:51
PROGRAM NAME =
 1                              ;*************************************************************
 2                              ;*
 3                              ;*      00 - NAME   :SIGNED 16 BIT BINARY MULTIPLICATION (SMUL)
 4                              ;*
 5                              ;*************************************************************
 6                              ;*
 7                              ;*      ENRTRY      :R1 (MULTIPLICAND)
 8                              ;*                   R0 (MULTIPLIER)
 9                              ;*
10                              ;*      RETURNS     :R1 (UPPER WORD OF RESULT)
11                              ;*                   R2 (LOWER WORD OF RESULT)
12                              ;*
13                              ;*************************************************************
14                              ;
15  SMUL_cod C    0000                      .SECTION              SMUL_code,CODE,ALIGN=2
16                                          .EXPORT  SMUL
17                              ;
18  SMUL_cod C          00000000  SMUL      .EQU $                ;Entry point
19  SMUL_cod C    0000  06AD                ANDC.B   #H'AD,CCR    ;Clear user bits
20  SMUL_cod C    0002  7771                BLD      #7,R1H       ;Load sign bit of multiplicand
21  SMUL_cod C    0004  4408                BCC      LBL1         ;Branch if C = 0
22  SMUL_cod C    0006  0440                ORC.B    #H'40,CCR    ;Bit set user bit (bit 6 of CCR)
23  SMUL_cod C    0008  1701                NOT      R1H          ;2's complement multiplicand
24  SMUL_cod C    000A  1709                NOT      R1L
25  SMUL_cod C    000C  0B01                ADDS.W   #1,R1
26  SMUL_cod C    000E            LBL1
27  SMUL_cod C    000E  7770                BLD      #7,R0H       ;Load sign bit of multiplier
28  SMUL_cod C    0010  4408                BCC      LBL2         ;Branch if C = 0
29  SMUL_cod C    0012  0410                ORC.B    #H'10,CCR    ;Bit set user bit (bit 4 of CCR)
30  SMUL_cod C    0014  1700                NOT      R0H          ;2's complement multiplier
31  SMUL_cod C    0016  1708                NOT      R0L
32  SMUL_cod C    0018  0B00                ADDS.W   #1,R0
33  SMUL_cod C    001A            LBL2
34  SMUL_cod C    001A  0C9A                MOV.B    R1L,R2L      ;
35  SMUL_cod C    001C  0C1C                MOV.B    R1H,R4L      ;
36  SMUL_cod C    001E  0C9B                MOV.B    R1L,R3L      ;
37  SMUL_cod C    0020  0C19                MOV.B    R1H,R1L      ;
38  SMUL_cod C    0022  5082                MULXU    R0L,R2       ;R0L * R2L -> R2
39  SMUL_cod C    0024  5084                MULXU    R0L,R4       ;R0L * R4L -> R4
40  SMUL_cod C    0026  5003                MULXU    R0H,R3       ;R0H * R3L -> R3
41  SMUL_cod C    0028  5001                MULXU    R0H,R1       ;R0H * R1L -> R1
42  SMUL_cod C    002A  08C2                ADD.B    R4L,R2H      ;R2H + R4L -> R2H
43  SMUL_cod C    002C  9400                ADDX.B   #H'00,R4H    ;R4H + #H'00 + C -> R4H
44  SMUL_cod C    002E  0839                ADD.B    R3H,R1L      ;R1L + R3L -> R1L
45  SMUL_cod C    0030  9100                ADDX.B   #H'00,R1H    ;R1H + #H'00 + C -> R1H
46  SMUL_cod C    0032  08B2                ADD.B    R3L,R2H      ;R2H + R3L -> R2H
47  SMUL_cod C    0034  0E49                ADDX.B   R4H,R1L      ;R1L + R4H + C -> R1L
48SMUL_cod C     0036  9100                ADDX.B   #H'00,R1H    ;R1H + #H'00 + C -> R1H
```

```
49                                  ;
50  SMUL_cod C    0038  020E              STC     CCR,R6L     ;CCR -> R6L
51  SMUL_cod C    003A  776E              BLD     #6,R6L      ;Load sign bit of multiplicand
52  SMUL_cod C    003C  754E              BXOR    #4,R6L      ;Bit exclusive OR sign bits
53  SMUL_cod C    003E  4410              BCC     LBL3        ;Branch if C = 0
54  SMUL_cod C    0040  1701              NOT     R1H         ;2's complement sign bits
55  SMUL_cod C    0042  1709              NOT     R1L         ;
56  SMUL_cod C    0044  1702              NOT     R2H         ;
57  SMUL_cod C    0046  170A              NOT     R2L         ;
58  SMUL_cod C    0048  8A01              ADD.B   #1,R2L      ;
59  SMUL_cod C    004A  9200              ADDX.B  #H'00,R2H   ;
60  SMUL_cod C    004C  9900              ADDX.B  #H'00,R1L   ;
61  SMUL_cod C    004E  9100              ADDX.B  #H'00,R1H   ;
62  SMUL_cod C    0050            LBL3
63  SMUL_cod C    0050  5470              RTS
64                                  ;
65                                  .END
*****TOTAL ERRORS 0
*****TOTAL WARNINGS 0
```

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