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# H8SX Series

## Multiple Bit Shift

### Introduction

As well as having an architecture that is upward-compatible with each CPU of the H8/300, H8/300H, and H8S series, so as to inherit a full complement of peripheral functions, the H8SX microcomputer series has a maximum operating frequency of 50 MHz and uses a 32-bit H8SX core CPU as well as an on-chip multiplier/divider to improve performance.

This H8SX series Application Note provides information you may be need during software and hardware design. This is a basic edition that provides operation examples that each use a single H8SX series on-chip peripheral function.

Although the operation of each program, circuit, and other aspects covered by this application note has been checked, make sure that you conduct your own operation checks before actually using the H8SX series.

### Contents

## 1. Overview

The H8SX series has an architecture that is upward-compatible with each CPU of the H8/300, H8/300H, and H8S series. Furthermore, in addition its instruction set has been enhanced to improve CPU performance. The enhancement of the instruction set has greatly improved coding efficiency compared to the conventional series. This improvement in the coding efficiency leads to benefits such as a reduction in the amount of ROM required to store programs, as well as the shortening of each instruction fetch cycle. This application note describes "multiple bit shift", which is an enhanced instruction set item.

## 2. Configuration

"Multiple bit shift" is described below. The conventional H8/300, H8/300H, and H8S series support only 1- or 2-bit shift instructions. With the H8SX series, however, 1-, 2-, 4-, 8-, and 16-bit shift instructions are supported as 2-byte code instructions. In addition, 32-bit shift instructions are added as 4-byte code instructions. For example, to perform a shift by 8 bits with the conventional H8S series, a 2-bit shift instruction is executed four times. With the H8SX series, an 8-bit shift instruction is executed once only. This is shown in Figure 1.

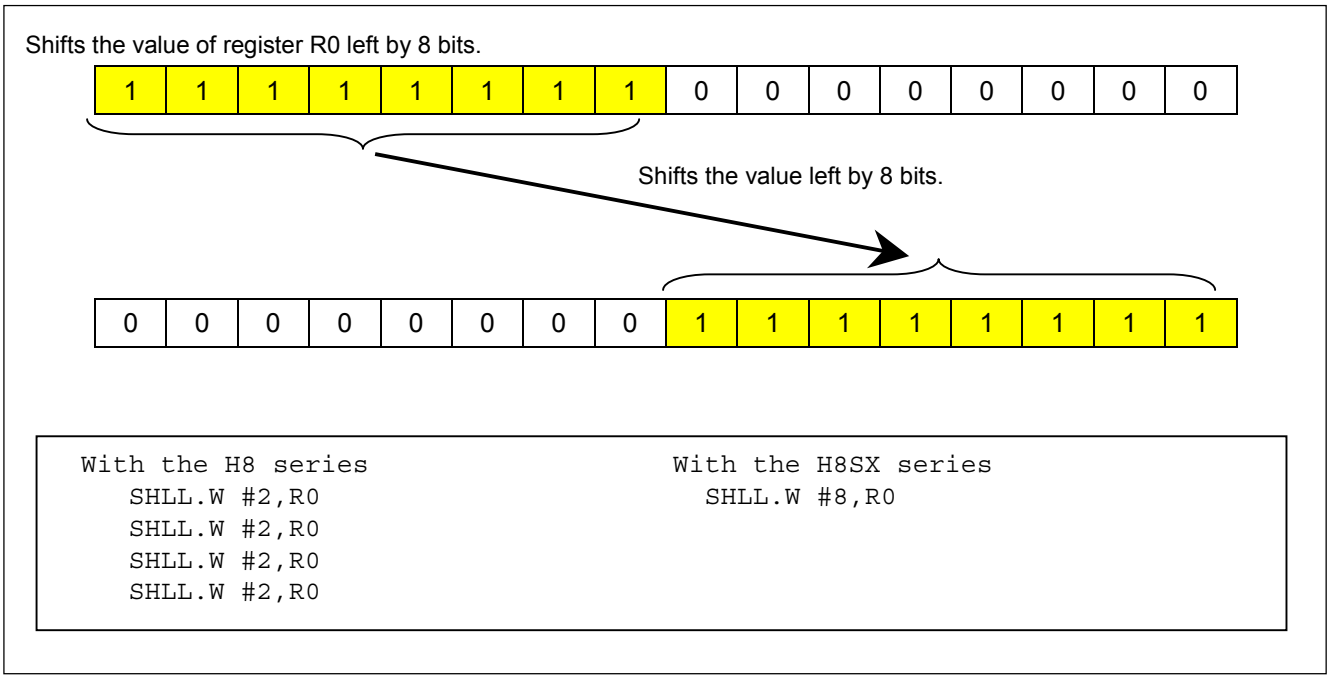


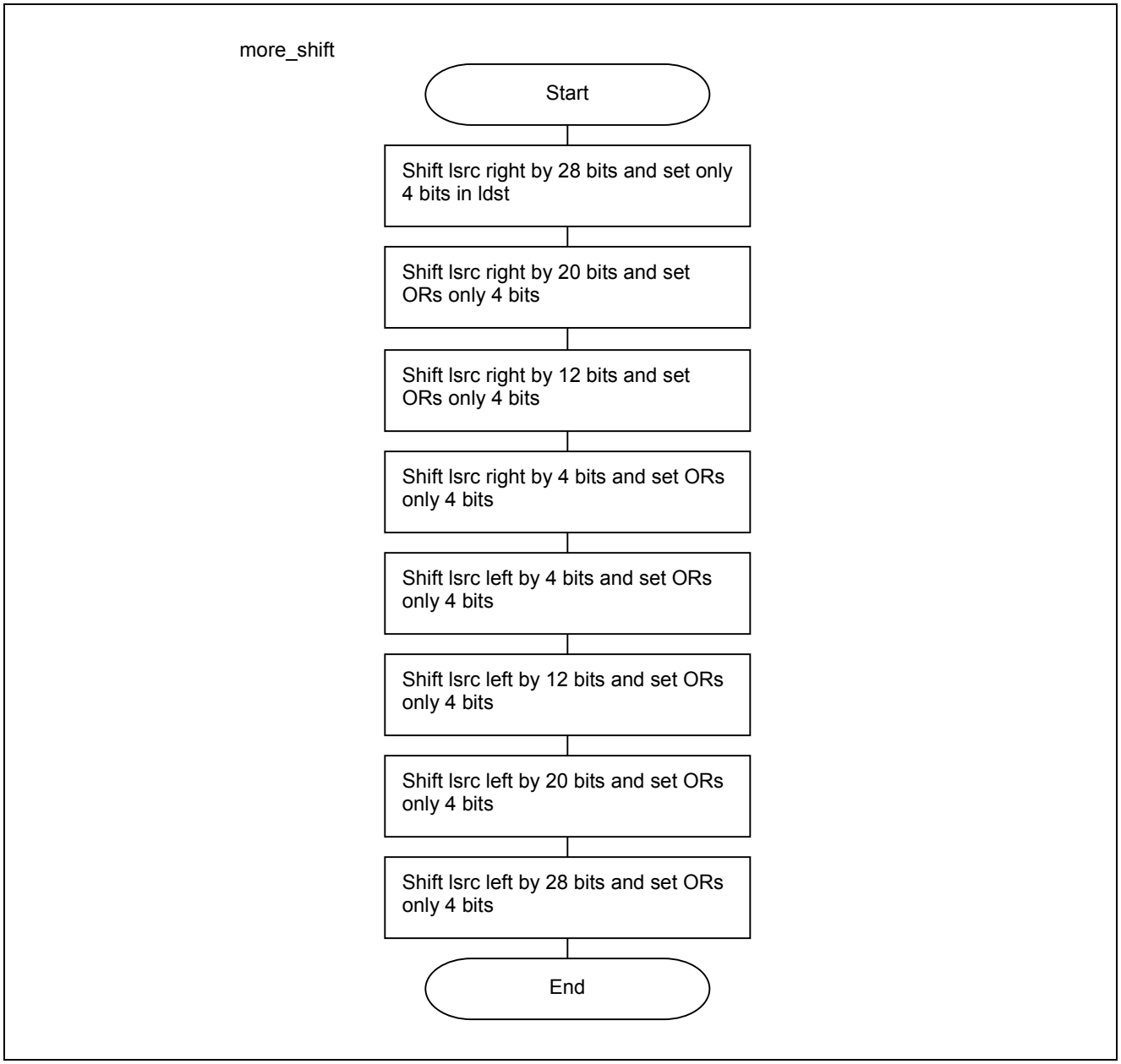

**Figure 1 Example of Shifting a Value Left by 8 Bits**

# 3. Sample Program

## 3.1 Flowchart

The sample program shown below is very simple, and will allow you to understand the description of "multiple bit shift", an enhanced instruction set item.

As a comparison with the H8S series, the results of compilation are shown. This example is for reference only because the instruction code length generated in the compilation of an application-level program greatly depends on the source program and the compile conditions. The flowchart for this sample program is shown below.



## 3.2 Program Listing

```
/************************************************************/
/* Include File                                             */
/************************************************************/
#include <machine.h>

/************************************************************/
/* Function Prototype                                       */
/************************************************************/
void more_shift(void);

/************************************************************/
/* RAM allocation                                           */
/************************************************************/
static unsigned long lsrc;       // Shift Data
static unsigned long ldst;       // Execute Shift Data
/************************************************************/
/* Function Definition(Main Program)                        */
/************************************************************/
void more_shift(void)
{
   lsrc = 0x12345678;             // Initialize lsrc
   ldst = 0;                      // Initialize ldst

   ldst  = (lsrc>>28)&0x0000000F; // 28bit Write Shift
   ldst |= (lsrc>>20)&0x000000F0; // 20bit Write Shift
   ldst |= (lsrc>>12)&0x00000F00; // 12bit Write Shift
   ldst |= (lsrc>>4 )&0x0000F000; // 4bit  Write Shift
   ldst |= (lsrc<<4 )&0x000F0000; // 4bit  Left  Shift
   ldst |= (lsrc<<12)&0x00F00000; // 12bit Left  Shift
   ldst |= (lsrc<<20)&0x0F000000; // 20bit Left  Shift
   ldst |= (lsrc<<28)&0xF0000000; // 28bit Left  Shift
}
```

## 3.3 Comparison of the H8S Series with the H8SX Series

The result of compilation (assembly code) with the H8S series is shown below.

```
P                                                  ; section
  00000000 _more_shift:                            ; function: more_shift
  00000000     PUSH.L      ER2
  00000004     MOV.L       #305419896,ER0
  0000000A     MOV.L       ER0,@__$lsrc:32
  00000012     SUB.L       ER0,ER0
  00000014     MOV.L       ER0,@__$ldst:32
  0000001C     MOV.L       @__$lsrc:32,ER0
  00000024     MOV.W       #28,R1
  00000028 L68:
  00000028     SHLR.L      #2,ER0
  0000002A     DEC.W       #2,R1
  0000002C     BGT         L68:8
```

```
0000002E     AND.L       #15,ER0
00000034     MOV.L       ER0,@__$ldst:32
0000003C     MOV.W       @__$lsrc:32,R0
00000042     SUB.W       E0,E0
00000044     SHLR.L      #2,ER0
00000046     SHLR.L      #2,ER0
00000048     AND.L       #240,ER0
0000004E     MOV.L       #__$ldst,ER1
00000054     MOV.L       @ER1,ER2
00000058     OR.L        ER0,ER2
0000005C     MOV.L       ER2,@ER1
00000060     MOV.L       @__$lsrc:32,ER0
00000068     MOV.W       #12,R1
0000006C L69:
0000006C     SHLR.L      #2,ER0
0000006E     DEC.W       #2,R1
00000070     BGT         L69:8
00000072     AND.L       #3840,ER0
00000078     MOV.L       #__$ldst,ER1
0000007E     MOV.L       @ER1,ER2
00000082     OR.L        ER0,ER2
00000086     MOV.L       ER2,@ER1
0000008A     MOV.L       @__$lsrc:32,ER0
00000092     SHLR.L      #2,ER0
00000094     SHLR.L      #2,ER0
00000096     AND.L       #61440,ER0
0000009C     MOV.L       @ER1,ER2
000000A0     OR.L        ER0,ER2
000000A4     MOV.L       ER2,@ER1
000000A8     MOV.L       @__$lsrc:32,ER0
000000B0     SHLL.L      #2,ER0
000000B2     SHLL.L      #2,ER0
000000B4     AND.L       #983040,ER0
000000BA     MOV.L       @ER1,ER2
000000BE     OR.L        ER0,ER2
000000C2     MOV.L       ER2,@ER1
000000C6     MOV.L       @__$lsrc:32,ER0
000000CE     MOV.W       #12,R1
000000D2 L70:
000000D2     SHLL.L      #2,ER0
000000D4     DEC.W       #2,R1
000000D6     BGT         L70:8
000000D8     AND.L       #15728640,ER0
000000DE     MOV.L       #__$ldst,ER1
000000E4     MOV.L       @ER1,ER2
000000E8     OR.L        ER0,ER2
000000EC     MOV.L       ER2,@ER1
000000F0     MOV.W       @__$lsrc+2:32,E0
000000F6     SUB.W       R0,R0
000000F8     SHLL.L      #2,ER0
000000FA     SHLL.L      #2,ER0
000000FC     AND.L       #251658240,ER0
00000102     MOV.L       @ER1,ER2
00000106     OR.L        ER0,ER2
```

```
   0000010A     MOV.L       ER2,@ER1
   0000010E     MOV.L       @__$lsrc:32,ER0
   00000116     MOV.W       #28,R1
   0000011A L71:
   0000011A     SHLL.L      #2,ER0
   0000011C     DEC.W       #2,R1
   0000011E     BGT         L71:8
   00000120     AND.L       #-268435456,ER0
   00000126     MOV.L       #__$ldst,ER1
   0000012C     MOV.L       @ER1,ER2
   00000130     OR.L        ER0,ER2
   00000134     MOV.L       ER2,@ER1
   00000138     POP.L       ER2
   0000013C     RTS

 B                                                  ; section
   00000000 __$lsrc                                 ; static: lsrc
   00000000     .RES.L      1
   00000004 __$ldst                                 ; static: ldst
   00000004     .RES.L      1
```

The result of compilation (assembly code) with the H8SX series is shown below.

```
 P                                                  ; section
   00000000 _more_shift:                            ; function: more_shift
   00000000     MOV.L       #305419896:32,@__$lsrc:32
   0000000C     MOV.L       #0:8,@__$ldst:32
   00000014     MOV.L       @__$lsrc:32,ER0
   0000001C     SHLR.L      #28:5,ER0
   00000020     AND.L       #15:16,ER0
   00000024     MOV.L       ER0,@__$ldst:32
   0000002C     MOV.L       @__$lsrc:32,ER0
   00000034     SHLR.L      #16,ER0
   00000036     SHLR.L      #4,ER0
   00000038     AND.L       #240:16,ER0
   0000003C     OR.L        ER0,@__$ldst:32
   00000044     MOV.L       @__$lsrc:32,ER0
   0000004C     SHLR.L      #8,ER0
   0000004E     SHLR.L      #4,ER0
   00000050     AND.L       #3840:16,ER0
   00000054     OR.L        ER0,@__$ldst:32
   0000005C     MOV.L       @__$lsrc:32,ER0
   00000064     SHLR.L      #4,ER0
   00000066     AND.L       #61440:16,ER0
   0000006A     OR.L        ER0,@__$ldst:32
   00000072     MOV.L       @__$lsrc:32,ER0
   0000007A     SHLL.L      #4,ER0
   0000007C     AND.L       #983040,ER0
   00000082     OR.L        ER0,@__$ldst:32
   0000008A     MOV.L       @__$lsrc:32,ER0
   00000092     SHLL.L      #8,ER0
   00000094     SHLL.L      #4,ER0
   00000096     AND.L       #15728640,ER0
   0000009C     OR.L        ER0,@__$ldst:32
```

```
   000000A4      MOV.L       @__$lsrc:32,ER0
   000000AC      SHLL.L      #16,ER0
   000000AE      SHLL.L      #4,ER0
   000000B0      AND.L       #251658240,ER0
   000000B6      OR.L        ER0,@__$ldst:32
   000000BE      MOV.L       @__$lsrc:32,ER0
   000000C6      SHLL.L      #28:5,ER0
   000000CA      AND.L       #-268435456,ER0
   000000D0      OR.L        ER0,@__$ldst:32
   000000D8      RTS

B                                                ; section
   00000000 __$lsrc                              ; static: lsrc
   00000000      .RES.L      1
   00000004 __$ldst                              ; static: ldst
   00000004      .RES.L      1
```

Table 1 lists the result of compilation with the H8S series, while Table 2 lists the result with the H8SX series.

**Table 1 Results of Compilation (H8S Series)**

| | | | Instruction length | | Execution state count | |
|---|---|---|---|---|---|---|
| **Shift count** | **H8S series** | | **In bytes** | **Total** | **State count** | **Total** |
| 28 | MOV.W | #28,R1 | 88 | 140 | 58 | 90 |
| | L68: | | | | | |
| | SHLR.L | #2,ER0 | | | | |
| | DEC.W | #2,R1 | | | | |
| | BGT | L68:8 | | | | |
| 20 | MOV.W | E0,R0 | 8 | | 4 | |
| | SUB.W | E0,E0 | | | | |
| | SHLR.L | #2,ER0 | | | | |
| | SHLR.L | #2,ER0 | | | | |
| 12 | MOV.W | #12,R1 | 40 | | 26 | |
| | L69: | | | | | |
| | SHLR.L | #2,ER0 | | | | |
| | DEC.W | #2,R1 | | | | |
| | BGT | L69:8 | | | | |
| 4 | SHLR.L | #2,ER0 | 4 | | 2 | |
| | SHLR.L | #2,ER0 | | | | |

**Table 2 Results of Compilation (H8SX Series)**

| | | | Instruction length | | Execution state count | |
|---|---|---|---|---|---|---|
| **Shift count** | **H8SX series** | | **In bytes** | **Total** | **State count** | **Total** |
| 28 | SHLR.L | #28:5,ER0 | 2 | 7 | 4 | 9 |
| 20 | SHLR.L | #16,ER0 | 2 | | 2 | |
| | SHLR.L | #4,ER0 | | | | |
| 12 | SHLR.L | #8,ER0 | 2 | | 2 | |
| | SHLR.L | #4,ER0 | | | | |
| 4 | SHLR.L | #4,ER0 | 1 | | 1 | |

## Revision Record

| | | Description | |
|---|---|---|---|
| Rev. | Date | Page | Summary |
| 1.00 | Sept.19.03 | — | First edition issued |
| | | | |
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