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SH7137 Group

MTU2: Output of Positive and Inverse PWM Signals in Three Phases (Reset-Synchronized PWM Mode)

Introduction

This application note describes an example of settings for the output of pulse width modulation (PWM) waveforms in three phases by using the multi-function timer pulse unit 2 (MTU2) in reset-synchronized PWM mode.

Target Device

SH7137

Contents

1. Preface

1.1 Specifications

This sample program employs channels 3 and 4 of MTU2 in reset-synchronized PWM mode for output of positive and inverse PWM waveforms three phases. Figure 1 shows an overview.

1. Channels 3 and 4 of MTU2 are set up to operate in reset-synchronized mode. The output pins for the positive PWM signals are TIOC3B, TIOC4A, and TIOC4B. The corresponding inverse signals are output on pins TIOC3D, TIOC4C, and TIOC4D. The high level is selected as the active level for PWM output.
2. The PWM carrier cycle is set to 400 µs.
3. PWM duty cycles in three phases are incremented or decremented by an interrupt signal generated every PWM cycle. The buffer function of registers is used to update the PWM duty cycle.
4. The level on the TIOC3A pin is toggled in synchronization with the PWM carrier cycle to produce a waveform.

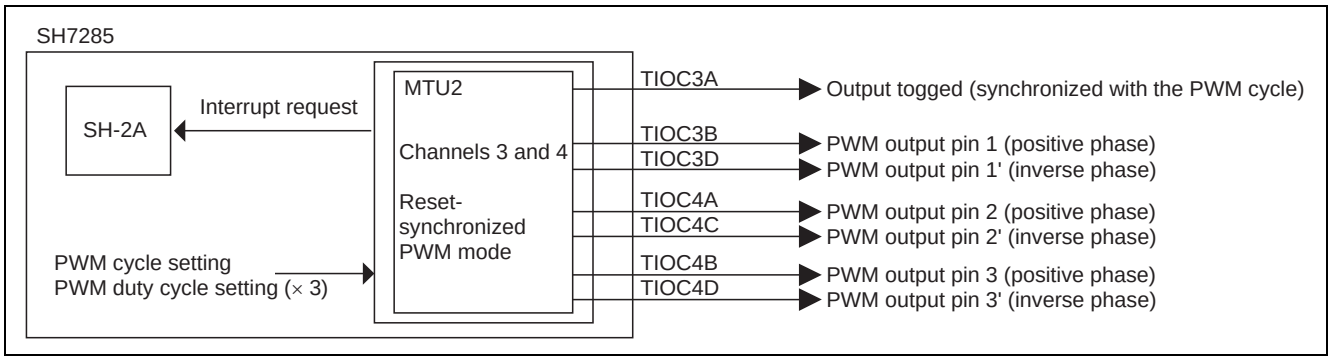


Figure 1 Three-Phase Output of PWM (Reset-Synchronized PWM Mode)

1.2 Module Used

Channels 3 and 4 of MTU2

1.3 Applicable Conditions

Table 1 Applicable Conditions

Item	Description
MCU	SH7137 [R5F7137]
Operating frequency	Internal clock: Iϕ = 80 MHz Bus clock: Bϕ = 40 MHz Peripheral clock: Pϕ = 40 MHz MTU2 clock: MPϕ = 40 MHz MTU2S clock: MIϕ = 80 MHz
MCU operating mode	Single-chip
C compiler	SuperH RISC engine C/C++ Compiler Ver.9.02.00 from Renesas Technology
C compiler options	Default settings of the C compiler

2. Description of the Sample Application

In this sample program, MTU2 is used in reset-synchronized PWM mode.

2.1 Operational Overview of Module Used

2.1.1 Multi-Function Timer Pulse Unit 2 (MTU2)

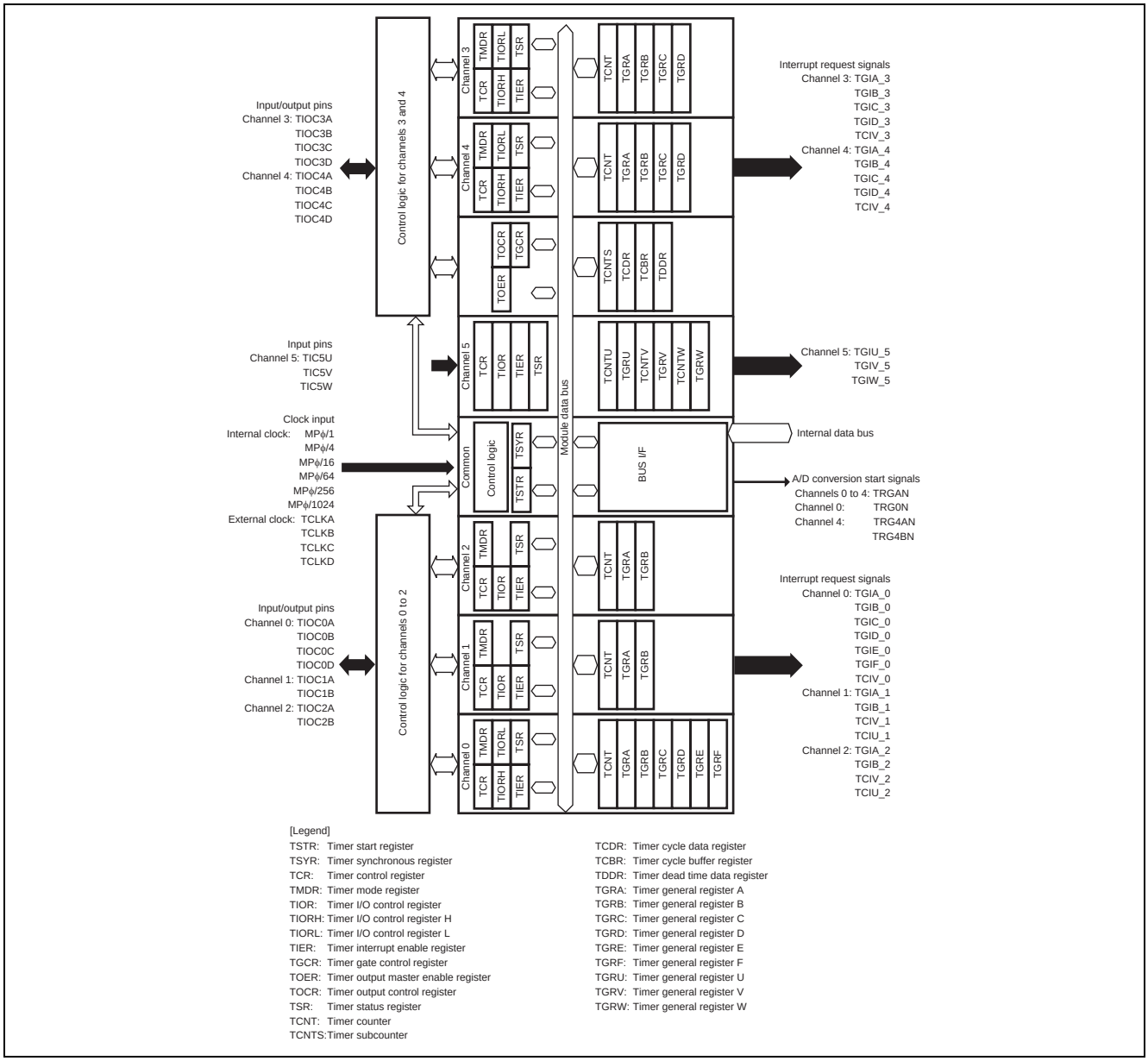
MTU2 is a multi-functional timer unit that has six 16-bit timer channels. Settings for compare-match function, input-capture function, etc. can be made for each channel. Settings for complementary PWM mode and reset-synchronized PWM mode are made for channels 3 and 4, enabling the control of six PWM output lines.

For details on MTU2, see the section on MTU2 in the *SH7137Group Hardware Manual* (REJ09B0402).

Table 2 gives an overview of MTU2 and figure 2 is a block diagram of MTU2.

Table 2 Overview of MTU2

Item	Description
Number of channels	16-bit timer × 6 channels (channels 0 to 5)
Counter clock	The clock signal for counter input can be selected from among 8 different input clock signals (except for channel 5, with only 4 different clock signals available).
Operation of channels 0 to 5	• Waveform output at compare match • Input capture function • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match and input capture • Input to and output from registers are synchronized with counter operation • PWM output in up to 12 phases in combination with synchronous operation
Triggers for A/D converter	• A/D converter start trigger can be generated. • In complementary PWM mode, interrupts at the crest and trough of the counter value and A/D converter start triggers can be skipped.
Buffered operation	• Settings for buffered operation of registers can be made to channels 0, 3, and 4.
Operating modes	• Settings for PWM mode can be made to channels 0 to 4. • Settings for phase counting mode can be set for each of channels 1 and 2 individually. • Waveform output in a total of six phases, including the positive and inverse signals for three phases, is possible in reset-synchronized PWM mode or complementary PWM mode.
Interrupt requests	• 28 different interrupt sources (interrupts generated by compare match, input capture, etc.)
Others	• Cascade-connection operation • High-speed access by internal 16-bit bus • Automatic transfer of register data is enabled. • Module standby mode can be set. • Dead time compensation counter is available in channel 5.



[Legend]

TSTR: Timer start register
TSYR: Timer synchronous register
TCR: Timer control register
TMDR: Timer mode register
TIOR: Timer I/O control register
TIORH: Timer I/O control register H
TIORL: Timer I/O control register L
TIER: Timer interrupt enable register
TGCR: Timer gate control register
TOER: Timer output master enable register
TOCR: Timer output control register
TSR: Timer status register
TCNT: Timer counter
TCNTS: Timer subcounter
TCDR: Timer cycle data register
TCBR: Timer cycle buffer register
TDDR: Timer dead time data register
TGRA: Timer general register A
TGRB: Timer general register B
TGRC: Timer general register C
TGRD: Timer general register D
TGRE: Timer general register E
TGRF: Timer general register F
TGRU: Timer general register U
TGRV: Timer general register V
TGRW: Timer general register W

Figure 2 Block Diagram of MTU2

2.1.2 Reset-Synchronized PWM Mode

In reset-synchronized PWM mode, channels 3 and 4 are used for the output of two sets (positive and inverse) of three-phase PWM waveforms, with each set sharing a common transition in one direction.

When set for reset-synchronized PWM mode, pins TIOC3B, TIOC4A, and TIOC4B function as output pins for the positive PWM signals, while pins TIOC3D, TIOC4C, and TIOC4D function as output pins for the corresponding inverse signals. Timer counter_3 (TCNT_3) functions as an up-counter. The counter is cleared when the value in TCNT_3 matches that in the TGRA_3 register (cycle), then counts up again from H'0000. Output levels on the PWM output pins are toggled on each compare-match with TGRB_3, TGRA_4, and TGRB_4, respectively, and each time the counter is cleared.

Figure 3 shows an example of the timing of operation in reset-synchronized PWM mode. In this example, the active level for output of positive and inverse PWM signals is high.

Table 3 is a list of the PWM output pins for use in reset-synchronized PWM mode, and table 4 gives descriptions of the functions of registers.

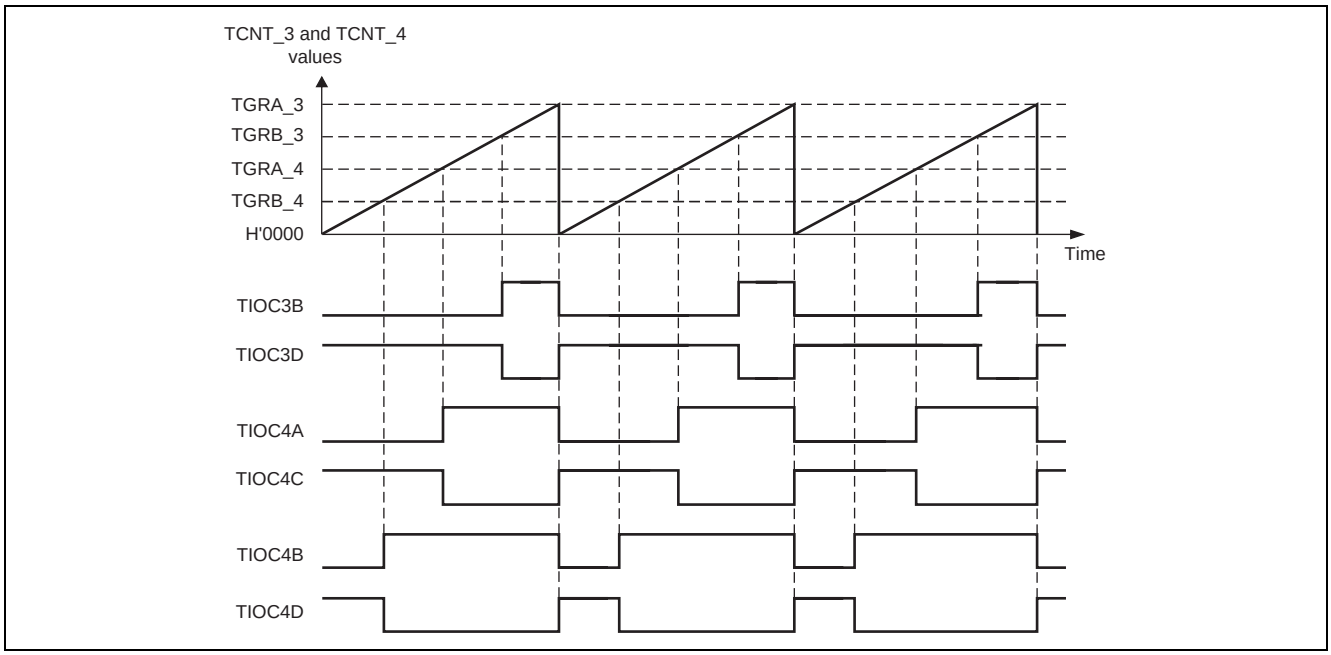


Figure 3 Sample Timing of Operation in Reset-Synchronized PWM Mode (In TOCR, OLSN = 1 and OLSP = 1)

Table 3 Output Pins in Reset-Synchronized PWM Mode

Channel	Output Pin	Description
Channel 3	TIOC3A	Output level is toggled in synchronization with the PWM cycle (if the pin is not used to output a toggled signal, it is available for use as an input or output port pin).
	TIOC3B	PWM output pin 1
	TIOC3D	PWM output pin 1' (inverse waveform corresponding to PWM output 1)
Channel 4	TIOC4A	PWM output pin 2
	TIOC4C	PWM output pin 2' (inverse waveform corresponding to PWM output 2)
	TIOC4B	PWM output pin 3
	TIOC4D	PWM output pin 3' (inverse waveform corresponding to PWM output 3)

Table 4 Registers Used in Reset-Synchronized PWM Mode

Register	Description
TCNT_3	Timer counter_3. The initial value is H'0000.
TCNT_4	Timer counter_4. The initial value is H'0000.
TGRA_3	Sets the period of counting by TCNT_3 (PWM cycle). When the PWM cycle is to be updated, the new value is set in a buffer register.
TGRB_3	Compare-match register. Sets a transition point for the PWM waveforms output from the TIOC3B and TIOC3D pins and thus determines the duty cycle. When the duty cycle is to be updated, the new value is set in a buffer register.
TGRA_4	Compare-match register. Sets a transition point for the PWM waveforms output from the TIOC4A and TIOC4C pins and thus determines the duty cycle. When the duty cycle is to be updated, the new value is set in a buffer register.
TGRB_4	Compare-match register. Sets a transition point for the PWM waveforms output from the TIOC4B and TIOC4D pins and thus determines the duty cycle. When the duty cycle is to be updated, the new value is set in a buffer register.
TGRC_3	Buffer register of TGRA_3 (if the buffering function is in use)
TGRD_3	Buffer register of TGRB_3 (if the buffering function is in use)
TGRC_4	Buffer register of TGRA_4 (if the buffering function is in use)
TGRD_4	Buffer register of TGRB_4 (if the buffering function is in use)

2.2 Operation of the Sample Program

2.2.1 Setting for Operation of the Sample Program

In this sample program, the output of PWM waveforms in three phases on channels 3 and 4 of MTU2 is obtained by selecting reset-synchronized PWM mode.

Table 5 gives the setting conditions for MTU2 in this sample program.

Table 5 Setting for Operation in Reset-Synchronized PWM Mode

Item	Description
Channels in use	3 and 4
Operating mode	Reset-synchronized PWM mode
Functions of pins	• TIOC3A pin: Output toggled in synchronization with the PWM cycle • TIOC3B pin: PWM output 1 (positive waveform) • TIOC3D pin: PWM output 1' (inverse waveform of PWM output 1) • TIOC4A pin: PWM output 2 (positive waveform) • TIOC4C pin: PWM output 2' (inverse waveform of PWM output 2) • TIOC4B pin: PWM output 3 (positive waveform) • TIOC4D pin: PWM output 3' (inverse waveform of PWM output 3)
Active level	• Output of positive signal: Active high • Output of inverse signal: Active high
Counter clock	10 MHz (Obtained by dividing Pϕ clock frequency by 4)
PWM carrier cycle	400 μs (carrier frequency: 2.5 kHz)
PWM duty cycle	• Initial duty cycle for PWM outputs 1, 2, 3: 50% • PWM duty cycle value is updated every time the TGRA_3 interrupt is generated (setting is incremented or decremented).
Interrupt	• Compare match interrupt for TGRA_3 A TGRA_3 compare match is generated once per PWM-carrier cycle.

2.2.2 Description of Operation by the Sample Program

Figure 4 shows the operation of the sample program. Channels 3 and 4 of MTU2 are placed in reset-synchronized PWM mode. Buffered operation is selected for the registers used to set cycles and PWM duty cycles. Bits BFA and BFB in the TMDR_3 register are used to specify buffered operation. In this case, when the BFA and BFB bits are set to 1, TGRC_3 and TGRD_3 on channel 3 function as the buffer registers for TGRA_3 and TGRB_3, respectively. At the same time, TGRC_4 and TGRD_4 on channel 4 function as the buffer registers for TGRA_4 and TGRB_4, respectively.

Three-phase PWM duty cycles are updated by handling the TGRA_3 compare match interrupt which is generated every PWM carrier cycle. The values for updating the PWM duty cycles are set in buffer registers TGRD_3, TGRC_4, and TGRD_4. The value in each buffer register is transferred to the corresponding comparison register on the compare match from TRRA_3 that is generated every cycle. Buffered operation enables the updating of registers with the desired timing.

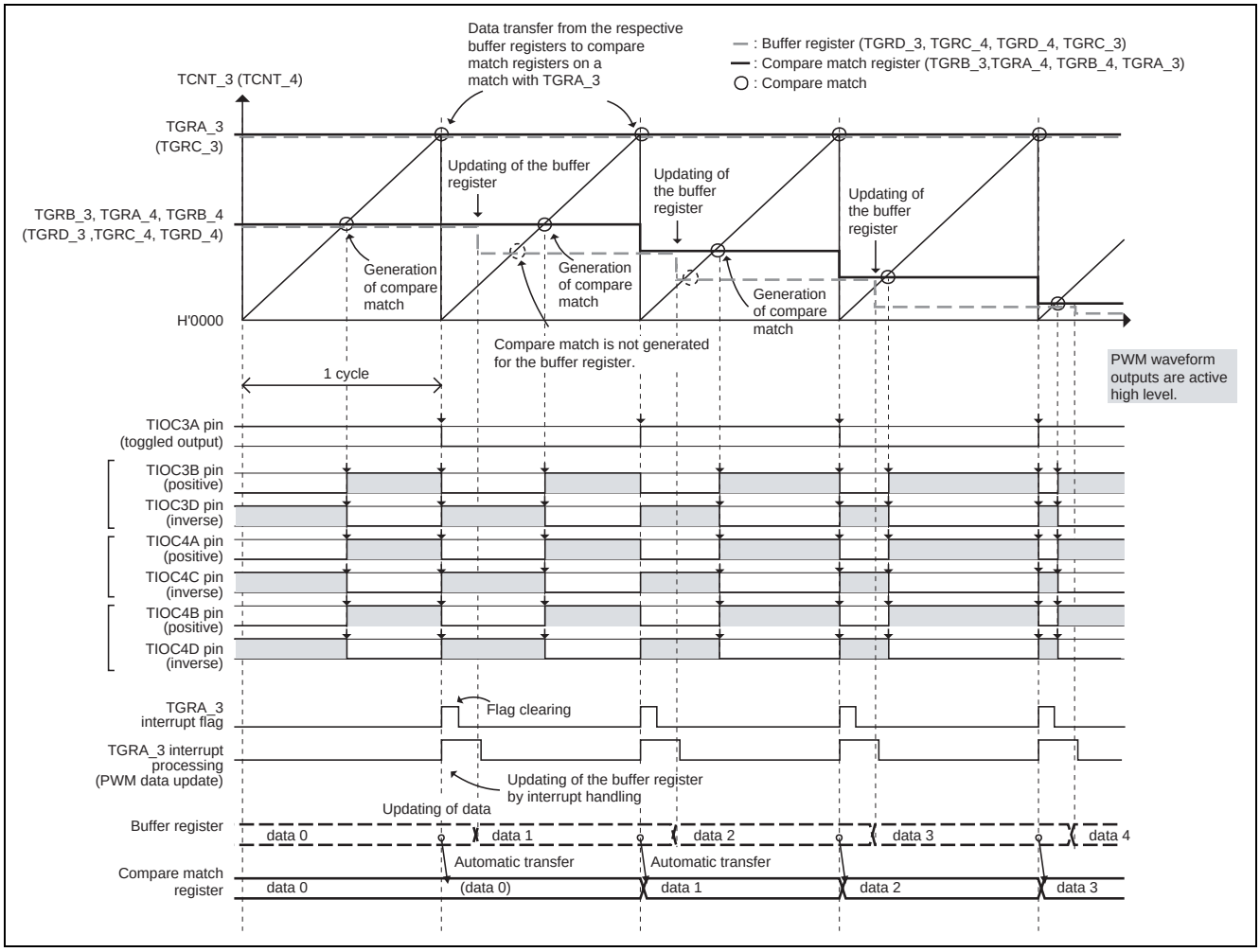


Figure 4 Operation (Buffered Operation) in Reset-Synchronized PWM Mode

1. Setting of Cycle Register
   When the setting has been made so that the counter is cleared on a match with cycle register TGRA_3, the TCNT timer counter is cleared on the last state in which the value of TCNT matches the value of TGR (the timing that TCNT updates the matched count value). Accordingly, the setting of the cycle register (TGRA_3 register) can be obtained from the following formula.

   Setting of the TGRA_3 register = (PWM period/count-by-one period) – 1
   PWM period: Setting for the desired period (cycle) of the PWM carrier
   Count-by-1 period: Period for the timer counter (TCNT) to count up by 1

   If the PWM carrier cycle is to be 400 μs, the following value is set in the cycle register (TGRA_3 register).

   Setting of the TGRA_3 register = 400 μs/100 ns – 1
   = D'3999

   Clock for counting by timer counter TCNT: 10 MHz (Pϕ/4: Pϕ is the on-chip peripheral clock)
   Count-by-1 period: 100 ns

2. Setting PWM duty cycle to 100% and 0%
   Figure 5 shows PWM output waveforms when duty register (TGRB_3) is set to H'0000 or the same as the value in period register (TGRA_3) in reset-synchronized PWM Mode.
   In the mode, as it is shown in figure 5, when the setting of PWM duty register TGRB_3 is H'0000, a PWM waveform is still output in the form of a pulse waveform over the period for the timer counter (TCNT) to count up by 1. When the setting of TGRB_3 is the same as or greater than the value of TGRA_3, the output level of the PWM waveform is toggled between the high and low level at the end of every cycle of counting.
   Changing the setting value in the duty register cannot fix the PWM output level to the high (PWM duty value: 100%) or the low (0%)
   If the output level is to be fixed to either the high or low level, set the pin function controller (PFC) to change the pin function specification from the timer pin (PWM output pin) function to the port output pin function, and then fix the level of the output signal.

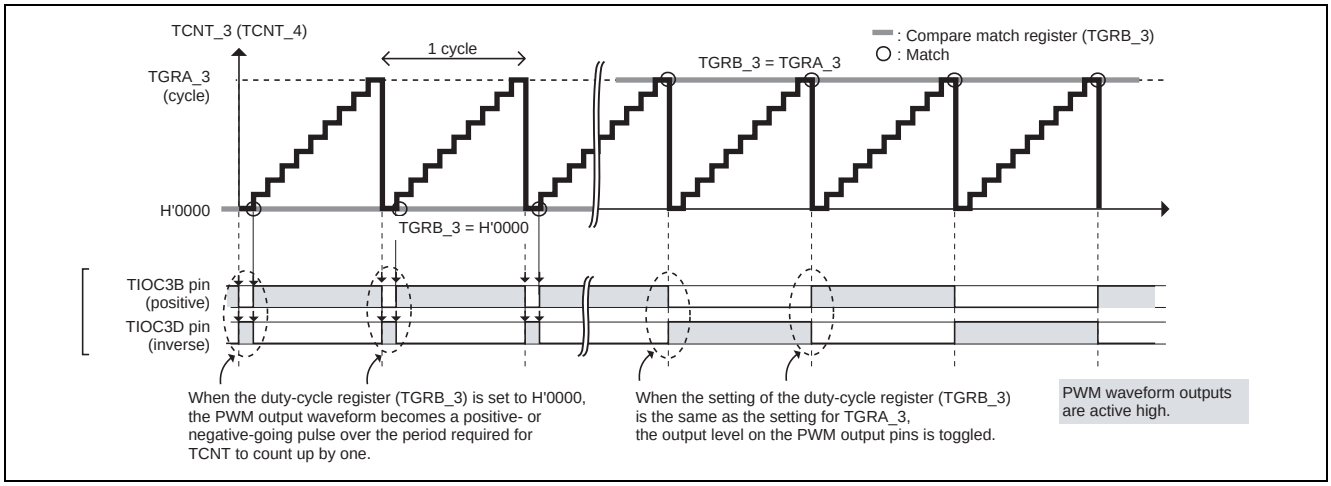


Figure 5 Settings of the Duty-Cycle Register and Corresponding PWM Output Waveforms

2.3 Configuration of the Sample Program

2.3.1 Description of Functions

Table 6 lists functions used in this sample program.

Table 6 Functions Used

Function Name	Label	Description
Main	main ()	Initializes other modules and makes setting for timers of MTU2
Standby setting	stbcr_init ()	Makes setting to release MTU2 from standby
Initialization of MTU2	mtu2_init ()	Initialized MTU2 (channels 3 and 4) Places channels 3 and 4 in reset-synchronized PWM mode
Initialization of PFC	pfc_init ()	Initializes the pin function controller (PFC) Selects the required MTU2-related pin functions, so that the pins function as timer pins
TGRA_3 interrupt	int_mtu2_tgia3()	Handles the TGRA_3 compare match interrupt from MTU2 (channel 3) Increments or decrements the setting to control the three-phase PWM duty cycle

2.3.2 Variable Usage

Table 7 gives a list of variables used in the sample program.

Table 7 Variable Usage

Label Name	Description	Name of Employing Module
C_cycle	Setting for the PWM carrier cycle (value set in the TGRC_3 register)	mtu2_init ()
Pul_pwm_duty1	PWM duty-cycle setting for the PWM1 output (pins TIOC3B and TIOC3D) (value set in the TGRD_3 register)	mtu2_init () int_mtu2_tgra3()
Pul_pwm_duty2	PWM duty-cycle setting for the PWM2 output (pins TIOC4A and TIOC4C) (value set in the TGRC_4 register)	
Pul_pwm_duty3	PWM duty-cycle setting for the PWM3 output (pins TIOC4B and TIOC4D) (value set in the TGRD_4 register)	

2.4 Procedure for Setting the Module Used

The following subsections describe the flow of processing by the sample program.

2.4.1 Main Function

Figure 6 shows the flow of processing by the main function.

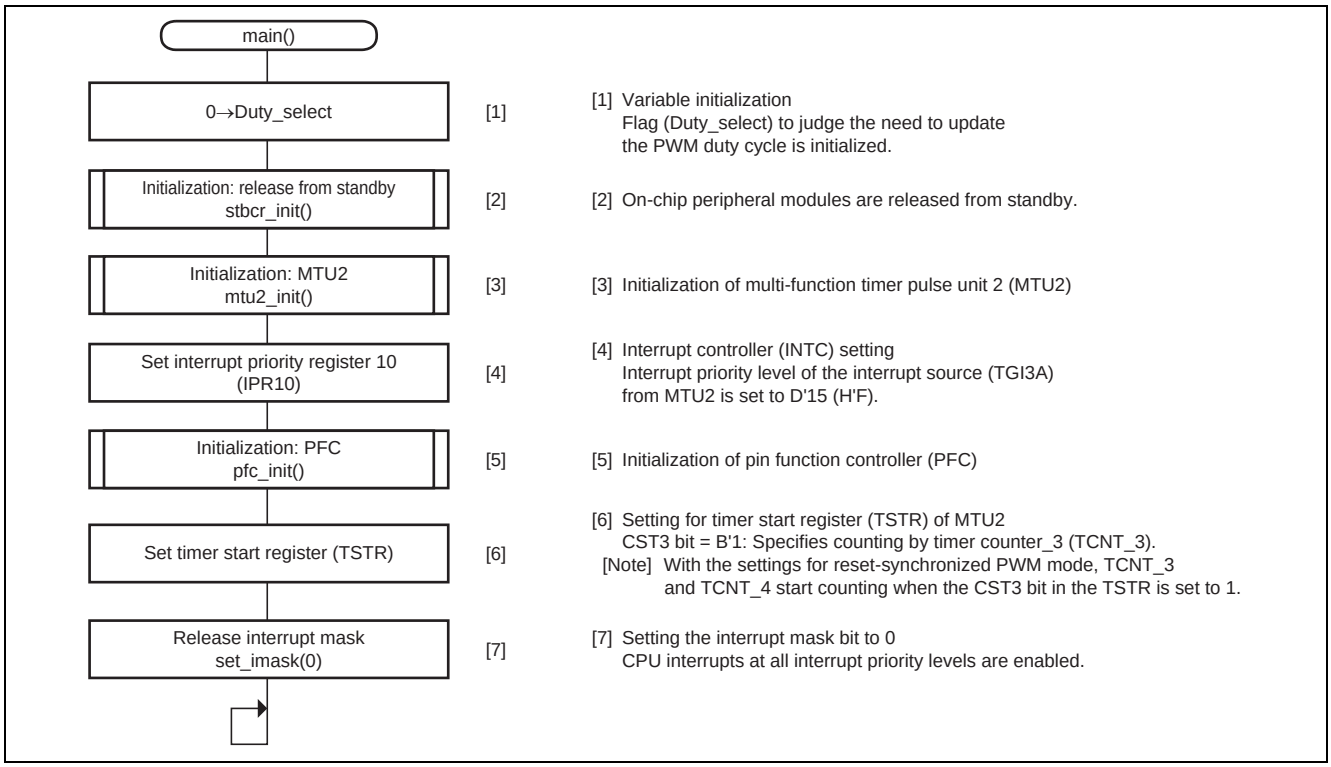


Figure 6 Processing by Function main

2.4.2 Setting to Release the Module from Standby

Figure 7 shows the flow of processing for release of the module from standby.

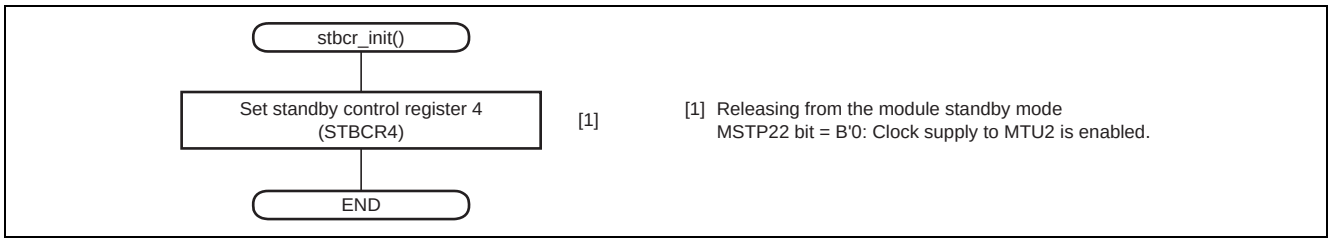
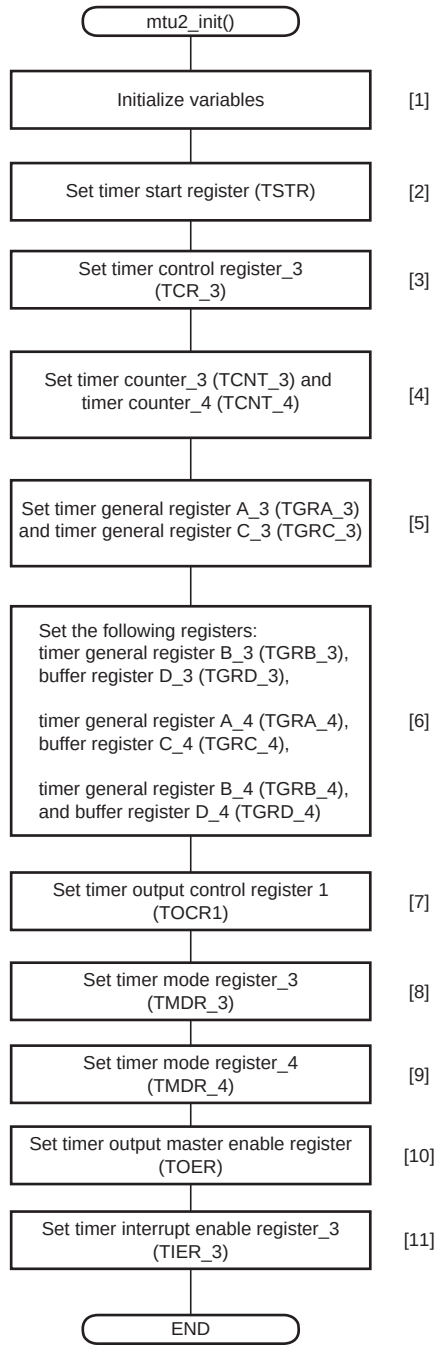


Figure 7 Setting for Release of the Module from Standby

2.4.3 Initialization of Multi-Function Timer Pulse Unit 2 (MTU2)

Figure 8 shows the flow for initialization of MTU2. Settings are made to set up reset-synchronized PWM mode on channels 3 and 4.



[1] Initialization of variables
C_cycle: Sets initial value of PWM carrier cycle.
Pul_pwm_duty1, 2, 3: Sets the initial values of duty cycle for PWM outputs 1, 2, and 3.

[2] Clear bits CST3 and CST4 in timer start register (TSTR) to 0 to halt counting by the timer counters (TCNT).

[3] Specification of clock source and source for clearing of timer counters
- CCLR[2:0] bits = B'001: Selects clearing of TCNT on a match with TGRA.
- CKEG[1:0] bits = B'00: TCNT counts rising edges.
- TPSC[2:0] bits = B'001: TCNT counts cycles of internal clock Pϕ/4.

[Note] When channel 3 is set to reset-synchronized PWM mode, settings made for timer control register_4 (TCR_4) of channel 4 are ineffective (operation is automatically in accord with the settings of channel 3).
No setting is made; the register is left at its initial value.

[4] Initialization of timer counters TCNT_3 and TCNT_4
H'0000 is set in the TCNT_3 and TCNT_4 registers.

[5] PWM carrier cycle (400 μs/2.5 kHz) is set in timer general register (TGRA_3).
Setting of TGRC_4 (buffer register for TGRA_3) is the same as the setting for TGRA_3.

[6] Initialization of three-phase PWM duty cycles
Initial values for PWM duty cycle are set in compare match registers (TGRB_3, TGRA_4, and TGRB_4) and buffer registers (TGRD_3, TGRC_4, and TGRD_4).
The same values are set in the compare match registers and buffer registers.
The setting should be within the range where a compare match with TCNT_3 will occur.
$X \leq$ TGRA_3 (X: Setting of duty cycle)

[Note] When X = TGRA_3 (cycle = duty cycle) is set, the output level of the PWM waveforms is toggled at the point where TCNT_3 = TGRA_3 = X.

[7] Setting to enable toggled output of PWM cycle and select the active PWM output level
- PSYE bit = B'1: Enables toggled output in synchronization with the PWM cycle.
- OLSN bit = B'1: Output of inverse signal is active at high level.
- OLSP bit = B'1: Output of positive signal is active at high level.

[8] Setting for operating modes
- BFB bit = B'1: TGRB and TGRD are set up for buffered operation.
- BFA bit = B'1: TGRA and TGRC are set up for buffered operation.
- MD[3:0] bits = B'1000: Reset-synchronized PWM mode

Mode setting should be made while TCNT_3 and TCNT_4 are halted.

[9] When channel 3 is set up for reset-synchronized PWM mode, settings for buffered operation and operating mode should not be made in TMDR_4.
The register is left at its initial value.

[10] Using timer output master enable register (TOER) to enable output on PWM output pins

[11] Setting to enable or disable interrupt requests
- TGIEA bit = B'1: Enables interrupt requests (TGIA_3) from channel 3.

Figure 8 Initialization of MTU2

2.4.4 Initialization of Pin Function Controller (PFC)

Figure 9 shows the flow for initialization of the PFC.

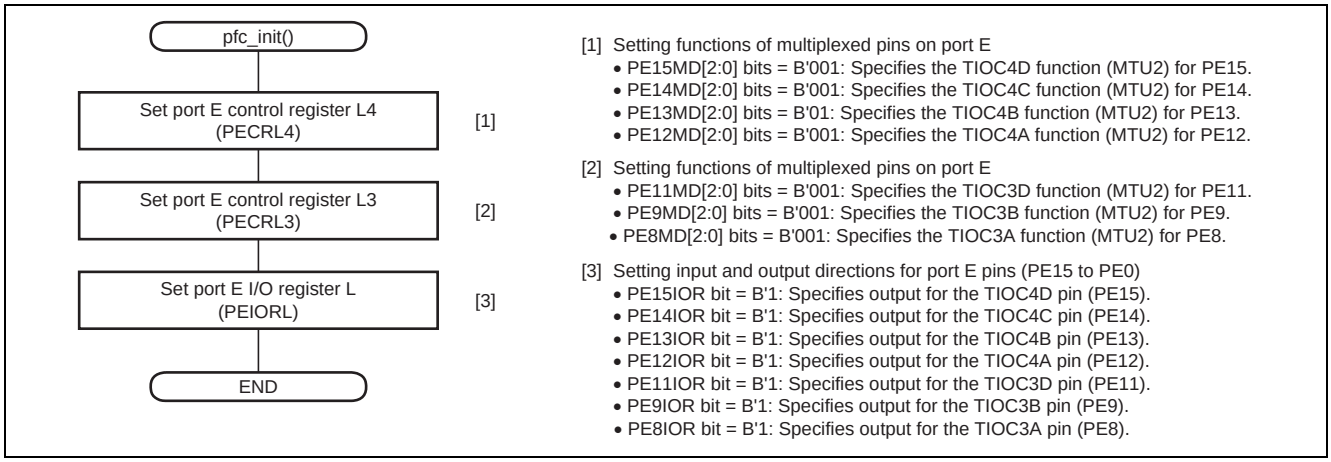


Figure 9 Initialization of PFC

2.4.5 Handling of the Compare Match Interrupt on Channel 3

Figure 10 shows the flow of handling for the compare match interrupt (TGRA_3) from MTU2 (channel 3). An interrupt is generated once per PWM carrier cycle.

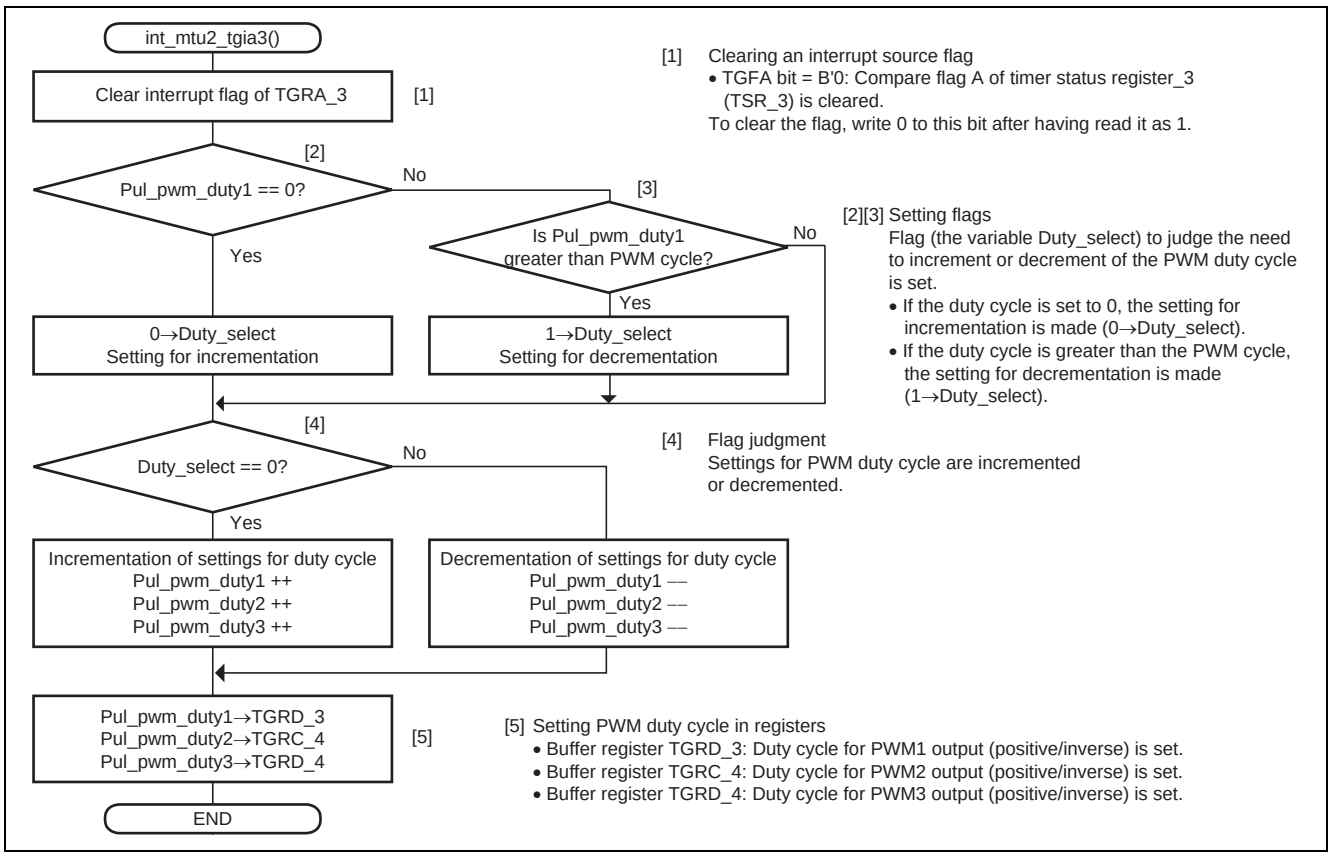


Figure 10 Handling the Compare Match (TGRA_3) Interrupt from Channel 3 of MTU2

2.5 Settings of Registers in the Sample Program

The following describes the settings of registers used in the sample program.

2.5.1 Clock Pulse Generator (CPG)

Table 8 gives a list of settings for registers for the clock pulse generator (CPG).

Table 8 Clock Pulse Generator

Register Name	Address	Setting	Description
Frequency control register (FRQCR)	H'FFFFE800	H'0241	Specifies division ratios for operating frequency • IFC[2:0] = B'000: ×1, internal clock (Iϕ) • BFC[2:0] = B'001: ×1/2, bus clock (Bϕ) • PFC[2:0] = B'001: ×1/2, peripheral clock (Pϕ) • MIFC[2:0] = B'000: ×1, MTU2S clock (MIϕ) • MPFC[2:0] = B'001: ×1/2, MTU2 clock (MPϕ)

2.5.2 Power-Down Modes

Table 9 gives register settings related to low-power modes.

Table 9 Power-Down Modes

Register Name	Address	Setting	Description
Standby control register 4 (STBCR4)	H'FFFE 0808	H'BF	Settings for the operation of various modules in power-down modes • MSTP23 = B'1: Clock supply to MTU2S halted. • MSTP22 = B'0: MTU2 runs. • MSTP21 = B'1: Clock supply to CMT halted. • MSTP20 = B'1: Clock supply to A/D_1 halted. • MSTP19 = B'1: Clock supply to AD_0 halted

2.5.3 Multi-Function Timer Pulse Unit 2 (MTU2)

Table 10 gives a list of settings for registers of multi-function timer pulse unit 2 (MTU2).

Table 10 Multi-Function Timer Pulse Unit 2 (MTU2)

Register Name	Address	Setting	Description
Timer control register_3 (TCR_3)	H'FFFFC200	H'21	Sets details of TCNT control • CCLR[2:0] = B'001: TCNT is cleared by TGRA compare match. • CKEG[1:0] = B'00: TCNT counts rising edge. • TPSC[2:0] = B'001: TCNT counts cycles of internal clock Pϕ/4.
Timer control register_4 (TCR_4)	H'FFFFC201	—	Sets details of TCNT control When channel 3 is set to reset-synchronized PWM mode, settings made for channel 4 are ineffective (operation is automatically in accord with the settings of channel 3). No setting is made. The register is left at its initial value.
Timer counter_3 (TCNT_3)	H'FFFFC210	H'0000	16-bit counter Initial value is set to 0.
Timer counter_4 (TCNT_4)	H'FFFFC212	H'0000	16-bit counter Initial value is set to 0.
Timer general register A_3 (TGRA_3)	H'FFFFC218	D'3999	Sets the upper limit of TCNT_3. Determines the PWM carrier cycle. During operation, the cycle is updated via a buffer register.
Timer general register C_3 (TGRC_3)	H'FFFFC224		Buffer register for TGRA_3 The initial setting of the buffer register for TGRA_3 is the same as the setting for TGRA_3.
Timer general register B_3 (TGRB_3)	H'FFFFC21A	D'1999	Comparison register for PWM output for 1. Determines the PWM duty cycle (initial output value). During operation, the PWM duty cycle is updated via a buffer register.
Timer general register D_3 (TGRD_3)	H'FFFFC226		Buffer register for TGRB_3 The initial value is the same as the value in TGRB_3.
Timer general register A_4 (TGRA_4)	H'FFFFC21C	D'1999	Comparison register for PWM output 2, Determines the PWM duty cycle in the initial state. During operation, the PWM duty cycle is updated via a buffer register.
Timer general register C_4 (TGRC_4)	H'FFFFC228		Buffer register for TGRA_4 The initial value is the same as the value in TGRA_4.
Timer general register B_4 (TGRB_4)	H'FFFFC21E	D'1999	Comparison register for PWM output 3. Determines the PWM duty cycle (initial output value). During operation, the PWM duty cycle is updated via a buffer register.
Timer general register D_4 (TGRD_4)	H'FFFFC22A		Buffer register for TGRB_4 The initial value is the same as the value in TGRB_4.

Register Name	Address	Setting	Description
Timer output control register 1 (TOCR1)	H'FFFFC20E	H'43	Sets output operation in reset-synchronized PWM mode. • PSYE = B'1: Toggled output in synchronization with PWM cycle is enabled. • TOCL = B'0: Writing to the TOCS, OLSN, and OLSP bits is enabled. • TOCS = B'0: Selects use of the TOCR1 setting. • OLSN = B'1: Selects levels for inverse output in reset-synchronized PWM mode. Initial output = low, active level = high • OLSP = B'1: Selects levels for output of positive signal in reset-synchronized PWM mode. Initial output = low, active level = high
Timer mode register_3 (TMDR_3)	H'FFFFC202	H'38	Sets operation mode (channel 3). • BFB = B'1: TGRB and TGRD are used together (buffered operation). • BFA = B'1: TGRA and TGRC are used together (buffered operation). • MD[3:0] = B'1000: Reset-synchronized PWM mode
Timer mode register_4 (TMDR_4)	H'FFFFC203	H'00 (Initial value)	Sets operation mode (channel 4). Note: When channel 3 is set to reset-synchronized PWM mode, settings made for channel 4 are ineffective (operation is automatically in accord with the settings of channel 3). No settings are made in this register, which is left at its initial value. Even if a setting is made for a buffer register, leave bits BFA and BFB in TMDR_4 at the value 0.
Timer output master enable register (TOER)	H'FFFFC20A	H'FF	Specifies enabling or disabling of output through the MTU2 output pins. • OE4D = B'1: MTU2 output on the TIOC4D pin is enabled. • OE4C = B'1: MTU2 output on the TIOC4C pin is enabled. • OE3D = B'1: MTU2 output on the TIOC3D pin is enabled. • OE4B = B'1: MTU2 output on the TIOC4B pin is enabled. • OE4A = B'1: MTU2 output on the TIOC4A pin is enabled. • OE3B = B'1: MTU2 output on the TIOC3B pin is enabled.
Timer interrupt enable register_3 (TIER_3)	H'FFFFC208	H'01	Specifies enabling or disabling of interrupt requests. TGIEA = B'1: Interrupt requests (TGIA) corresponding to setting of the TGFA bit are enabled.
Timer start register (TSTR)	H'FFFFC280	H'40	Selects operation or stoppage of TCNT for channels 0 to 4. • CST3 = B'1: TCNT_3 counts. Counting by TCNT_2 to TCNT_0 is stopped. Note: In reset-synchronized PWM mode, setting the CST3 bit in the TSTR to 1 starts counting by TCNT_3 on channel 3 and TCNT_4 on channel 4. Do not make the setting for counting by TCNT_4 on channel 4 (CST4 = B'1).

2.5.4 Interrupt Controller (INTC)

Table 11 gives a list of settings for registers of the interrupt controller (INTC).

Table 11 Interrupt Controller (INTC)

Register Name	Address	Setting	Description
Interrupt priority register E (IPRE)	H'FFFFE984	H'00F0	Selects interrupt priority (levels 0 to 15). • Bits 15 to 12 = B'0000: MTU2 (TGI2A and TGI2B) interrupt level = 0 • Bits 11 to 8 = B'0000: MTU2 (TCI2V and TCI2U) interrupt level = 0 • Bits 7 to 4 = B'1111: MTU3 (TGI3A to TGI3D) interrupt level = 15 • Bits 3 to 0 = B'0000: MTU3 (TCI3V) interrupt level = 0 The TGI3A interrupt is used in this sample program.

2.5.5 Pin Function Controller (PFC)

Table 12 gives a list of settings for registers of the pin function controller (PFC).

Table 12 Pin Function Controller (PFC)

Register Name	Address	Setting	Description
Port E control register L4 (PECRL4)	H'FFFFD310	H'1111	Specifies functions of multiplexed pins on port E. • PE15MD[2:0] = B'001: Specifies the TIOC4D I/O (MTU2) for: PE15. • PE14MD[2:0] = B'001: Specifies the TIOC4C I/O (MTU2) for PE14 • PE13MD[2:0] = B'01: Specifies the TIOC4B I/O (MTU2) for PE13. • PE12MD[2:0] = B'001: Specifies the TIOC4A I/O (MTU2) for PE12
Port E control register L3 (PECRL3)	H'FFFFD312	H'1011	Specifies functions of multiplexed pins on port E. • PE11MD[2:0] = B'001: Specifies the TIOC3D I/O (MTU2) for PE11. • PE10MD[2:0] = B'000: Specifies the PE10 I/O (port) for PE10. • PE9MD[2:0] = B'001 : Specifies the TIOC3B I/O (MTU2) for PE9. • PE8MD[2:0] = B'001 : Specifies the TIOC3A I/O (MTU2) for PE8.
Port E I/O register L (PEIORL)	H'FFFFD306	H'FB00	Specifies input and output directions for port E pins. • PE15IOR = B'1: Specifies the output for TIOC4D (PE15) pin. • PE14IOR = B'1: Specifies the output for TIOC4C (PE14) pin. • PE13IOR = B'1: Specifies output for the TIOC4B (PE13) pin. • PE12IOR = B'1: Specifies output for the TIOC4A (PE12) pin. • PE11IOR = B'1: Specifies output for the TIOC3D (PE11) pin. • PE10IOR = B'0: Specifies input for the PE10 (port). • PE9IOR = B'1: Specifies output for the TIOC3B (PE9) pin. • PE8IOR = B'1: Specifies output for the TIOC3A (PE8) pin. • PE7IOR to PE0IOR all set to B'0: PE7 to PE0 are input pins.

3. Documents for Reference

- Hardware Manual
  SH7137 Group Hardware Manual (REJ09B0402)
  The most up-to-date version of this document is available on the Renesas Technology Website.

- Software Manual
  SH-1/SH2/SH-DSP Software Manual (REJ09B0171)
  The most up-to-date version of this document is available on the Renesas Technology Website.

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