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April 1st, 2010
Renesas Electronics Corporation

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H8/300H Super Low Power Series

Measuring Voltage with ΔΣA/D Converter Generated by Internal Reference Voltage

Introduction

ΔΣA/D converter is used to measure the voltage input to the Ain1 pin. The internal input voltage provides the reference voltage for the ΔΣA/D converter. The data thus created after the conversion are saved to the internal RAM.

Target Device

H8/38086R

Contents

1. Specifications

- As is shown in figure 1, the ΔΣA/D converter of the H8/38086R is used to measure the voltage input to the Ain1 pin.
- The internal input voltage provides the reference voltage for the ΔΣA/D converter.
- The voltage to be measured is applied to the Ain1 pin. It is then A/D converted, and the data thus created are saved to the internal RAM. The A/D conversion is executed twice. The data created in the first round of conversion are discarded, and those from the second round are used. Also, the A/D-converted data read from the A/D Data Register (ADDR) are shifted 2 bits right and saved in the internal RAM as 14-bit data.
- The mode of operation is the wait mode. The oversampling frequency is ϕ. The A/D conversion is executed with the programmable-gain amplifier (PGA) bypassed.
- The operating mode is switched to sleep (high-speed) mode during A/D conversion since this minimizes the noise generated by the CPU. The A/D conversion end interrupt takes the chip out of sleep (high-speed) mode and places it in the active (high-speed) mode. The data generated by A/D conversion are then stored in the internal RAM. The module standby function is used to place internal peripheral functions other than the ΔΣA/D converter, such as SCI3, timer F, IIC2, the A/D converter, RTC, TPU, PWM, watchdog timer, and LCD internal peripheral module, on module standby.
- Ensure that the internal reference voltage has settled by waiting for about 0.8 ms before starting conversion.

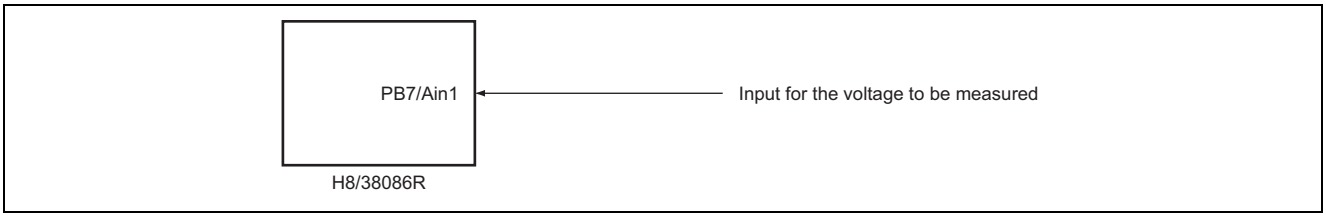


Figure 1 Voltage Measurement with the ΔΣA/D Converter (when Using the Internal Reference Voltage)

2. Measurement conditions

Figure 2 shows the measuring circuit in this sample task.

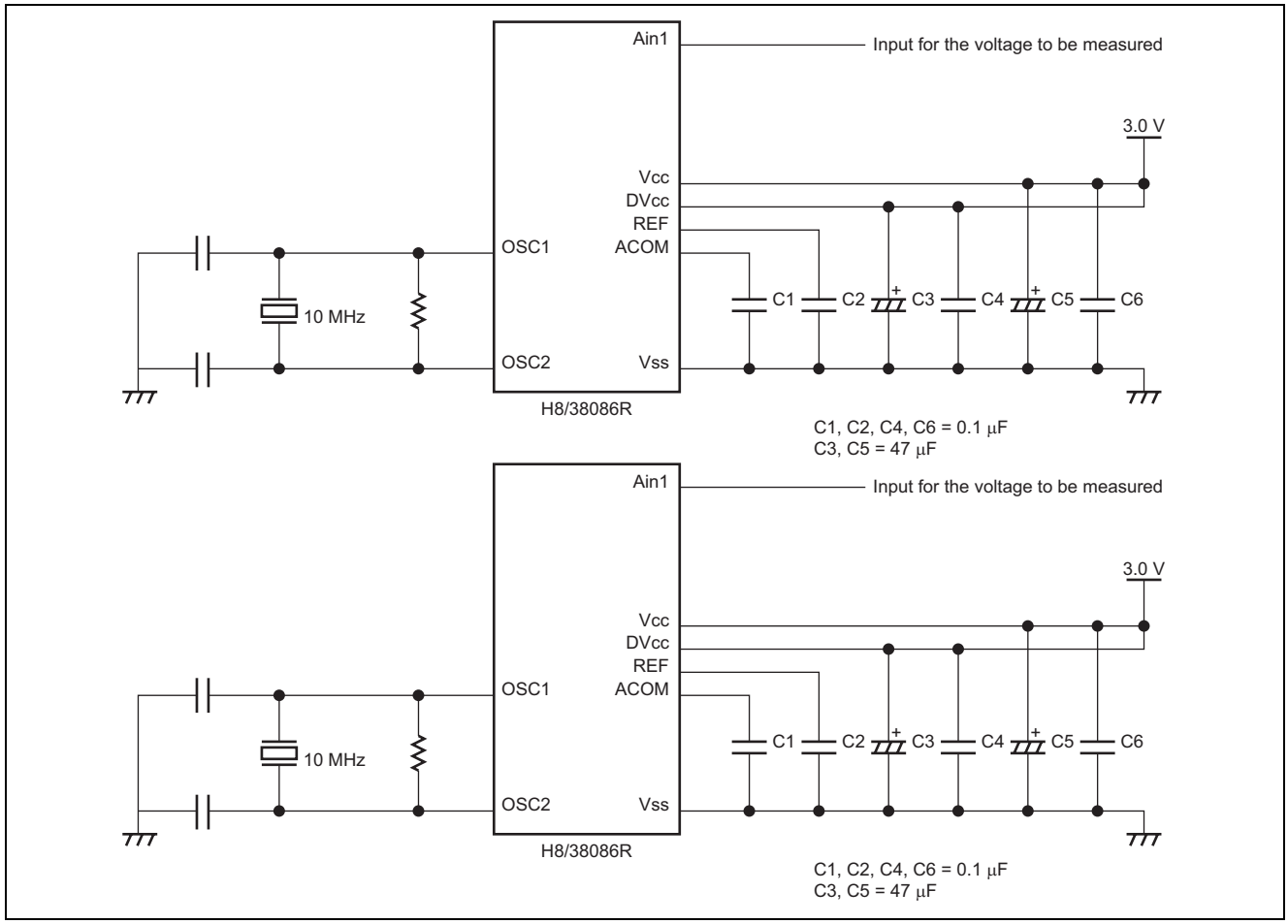


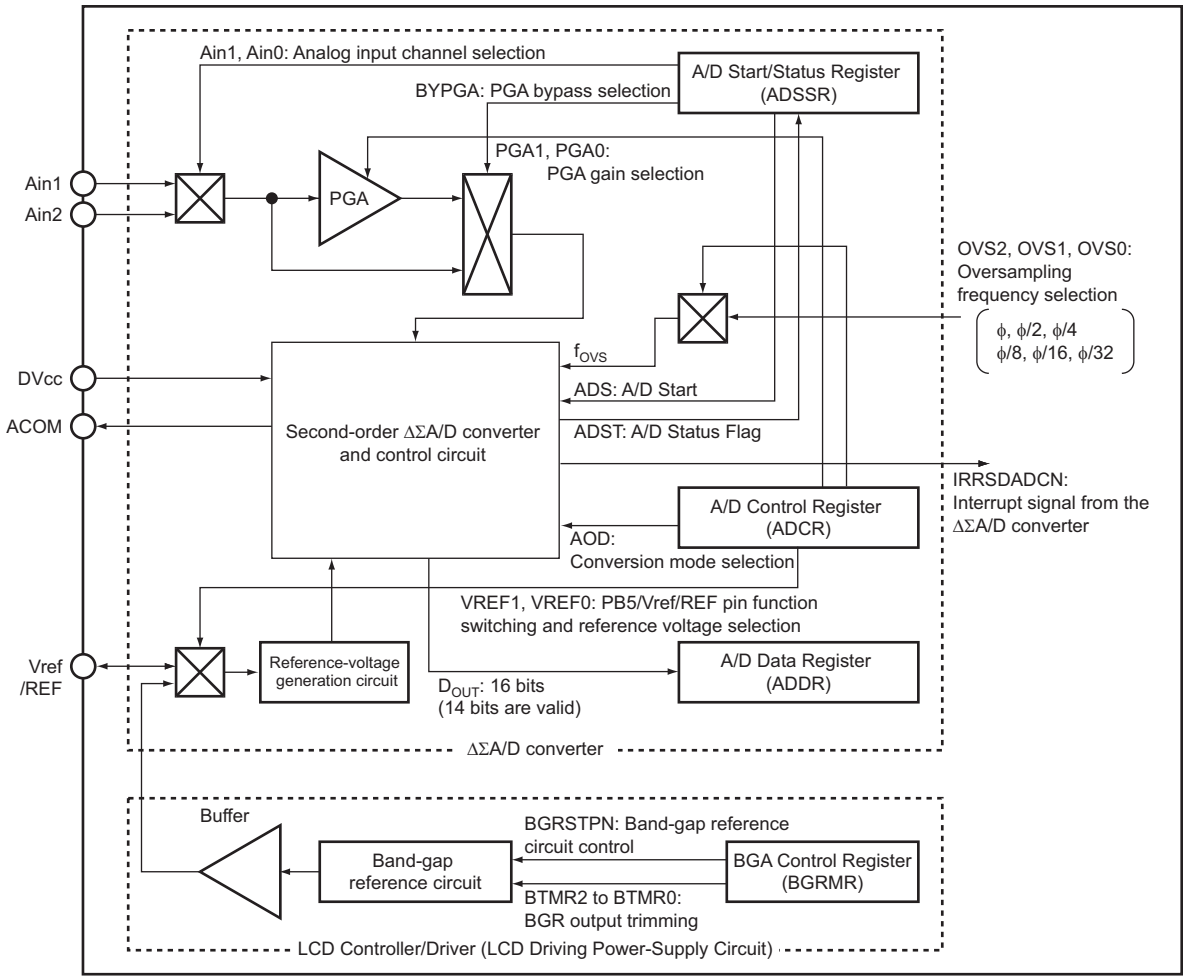
Figure 2 ΔΣA/D Converter Measuring Circuit (when Using the Internal Reference Voltage)

Conditions for voltage measurement with the ΔΣA/D converter using an external reference voltage are as follows.

- Vcc = 3.0 V
- DVcc = 3.0 V
- REF = internally input (about 1.2 V)
- System clock frequency (ϕ) = 10 MHz
- Oversampling frequency (fovs) = ϕ
- PGA = Bypass
- Conversion mode = wait mode
- Range of input voltage = 0.2 to approximately 1.2 V (REF)

3. Description of functions used

Figure 3 is a block diagram of the ΔΣA/D converter.



[Legend]
DVcc: ΔΣA/D Converter Analog Power-Supply Pin
Ain1: Analog Input Pin 1
Ain2: Analog Input Pin 2
Vref: Reference Voltage Pin
REF: Internal Reference Voltage Output Pin
ACOM: Analog Voltage Stabilization Pin

Figure 3 Block Diagram of the ΔΣA/D Converter

Functions of the ΔΣA/D converter are described below.

3.1 Features

- Resolution: 14 bits
- No. of input channels: 2
- Conversion type: Second-order ΔΣA/D converter, 320-times oversampling
- Conversion time: 32 µs per channel (in operation at 10 MHz)
- Interrupt source: One (A/D conversion end interrupt request)
- Module standby mode is available for placing this module on standby when it is not in use.

3.2 I/O pins

Table 1 is a list of the pins used for the ΔΣA/D converter

Table 1 Configuration of Pins for the ΔΣA/D Converter

Pin Name	Abbreviation	I/O	Function
Reference voltage pin	Vref	Input	Input for the external reference voltage
Internal reference voltage output pin	REF	Output	Output for the internal reference voltage
Analog voltage stabilization pin	ACOM	Output	For connection with a stabilizing capacitor (0.1 µF)
Analog input pin 1	Ain1	Input	Analog input pin
Analog input pin 2	Ain2	Input	
Analog power-supply pin for the ΔΣA/D converter	DVcc	Input	Power-supply pin

3.3 Description of registers

The ΔΣA/D converter has the following registers.

- A/D Data Register (ADDR)
  ADDR is a 16-bit read-only register that holds the results of A/D conversion. ADDR can be read by the CPU at any time, but values read from the ADDR during A/D conversion are undefined. On completion of A/D conversion, the 14-bit result of conversion is stored in the upper 14 bits in ADDR, and these data are retained until the next conversion operation starts. The initial value of ADDR is undefined.

- BGR Control Register (BGRMR)
  BGRMR controls the operation of the band-gap reference circuit (BGR) and adjusts the internal reference voltage output from the REF pin (BGR output voltage).

- A/D Control Register (ADCR)
  ADCR sets the conversion mode, PGA multiplication ratio, and reference voltage, and selects the PB5/Vref/REF pin function and oversampling frequency.

- A/D Start/Status Register (ADSSR)
  ADSSR contains the A/D conversion status flag, analog input channel selection bit, and bypass selection bit.

3.4 ΔΣA/D converter

The ΔΣA/D converter uses the ΔΣ modulator and converts the analog input voltage range specified by the Vref pin to digital data with 14-bit resolution. The ΔΣA/D converter is configured of two blocks, an analog block, the main part of which is a ΔΣ modulator, and a digital block, which consists of a digital filter control circuit.

In the analog block, voltages on the analog input pins (Ain1 and Ain2) are sampled at a frequency 320 times the conversion frequency (oversampling frequency) and then converted to a sequence of 1-bit digital values by the second-order ΔΣ modulator. The result of conversion is output as 14-bit data in unsigned binary code to the ADDR via the decimation filter in the digital block.

At this time, bit 13 in the ADDR is the MSB and bit 0 is the LSB.

3.5 Conversion modes of the ΔΣA/D converter

The ΔΣA/D converter has two modes, i.e. the wait mode and continuous mode.

3.5.1 Wait mode

In wait mode, A/D conversion is executed once for the specified one analog input channel as follows.

1. A/D conversion is started on the selected channel when the ADS bit in ADSSR is set to 1 by software.
2. The result is transferred to ADDR on completion of A/D conversion.
3. The IRRSAD flag in IRR2 is set to 1. If the value of the IENSAD bit in IENR2 is 1 at this time, an A/D conversion end interrupt request is generated.
4. The ADST bit remains set to 1 during A/D conversion. When A/D conversion ends, the ADST bit is automatically cleared to 0 and the A/D converter enters the wait state.

3.5.2 Continuous mode

In continuous mode, A/D conversion is executed continuously on the specified single analog input channel as follows.

1. A/D conversion is started on the selected channel when the MOD bit in ADCR is set to 1 by software.
2. The result is transferred to ADDR on completion of A/D conversion.
3. The IRRSAD flag in IRR2 is set to 1. If the value of the IENSAD bit in IENR2 is 1 at this time, an A/D conversion end interrupt request is generated.
4. Steps 2 and 3 are repeated. To stop conversion in continuous mode, the chip should be reset or placed in watch, subactive, subsleep, or standby mode, or the MOD bit in ADCR should be cleared to 0.

3.5.3 Operating modes of the ΔΣA/D converter

Table 2 shows the different operating modes of the ΔΣA/D converter

Table 2 Operating Modes of the ΔΣA/D Converter

Operating mode	Reset	Active	Sleep	Watch	Sub-active	Sub-sleep	Standby	Module standby
ADCR	Reset	Functions	Retained	Retained	Retained	Retained	Retained	Retained
ADSSR	Reset	Functions	Functions	Retained	Retained	Retained	Retained	Retained
ADDR	Retained*	Functions	Functions	Retained	Retained	Retained	Retained	Retained
BGRMR	Reset	Functions	Retained	Retained	Functions	Retained	Retained	Retained

Note: * Undefined during a power-on reset.

3.5.4 Assignment of pin functions

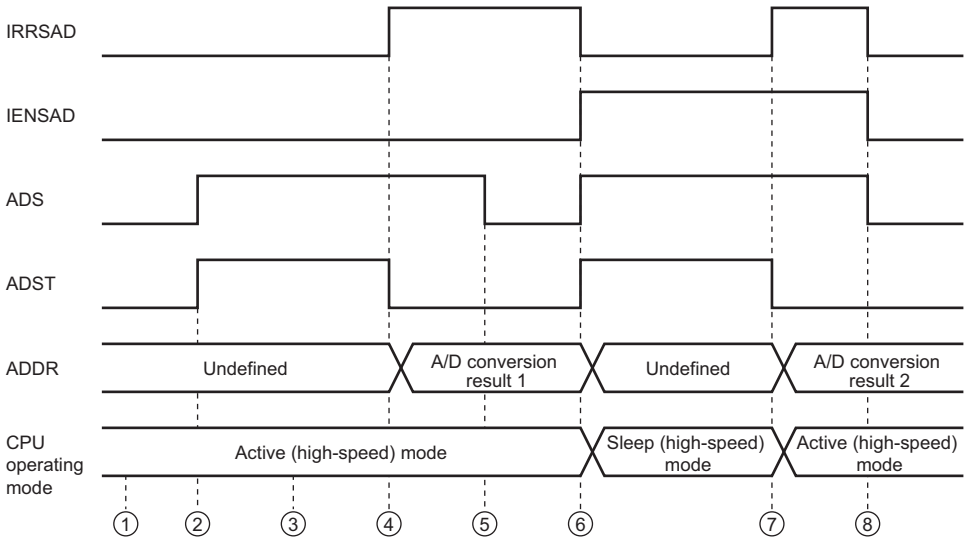
Table 3 shows the assignment of pin functions used in this sample task.

Table 3 Assignment of Pin Functions

Pin	Function
Vref/REF	As the REF output pin, output for the internal reference voltage (about 1.2 V)
DVcc	As the power-supply pin for the ΔΣA/D converter, input for 3.0 V dc
Ain1	As the analog input pin, input for the voltage to be measured
Ain2	Not used
ACOM	As the analog voltage stabilization pin, for connection to a 0.1-μF capacitor

4. Principle of operation

Figure 4 shows the principle of operation for ΔΣA/D conversion in the wait mode, i.e. the form used in this sample task. Polling by software is used to judge the completion of first round of A/D conversion. An interrupt is used to take the device out of sleep (high-speed) mode on completion of the second round of conversion.



① Initial settings of the ΣΔA/D converter

Software processing
1. Set ADCR to H'0C (conversion mode: wait mode, oversampling frequency: ϕ, PB5/Vref/REF pin function: REF output pin, reference voltage: internal reference voltage) 2. Set ADSSR to H'18 (analog input channel: Ain1, PGA bypass).

② Start the first round of A/D conversion.

Hardware processing
The ADST bit being set to 1 indicates that conversion is being executed by the ΔΣA/D converter.
Software processing
Set the ADS bit to 1 to start A/D conversion.

③ Wait for the end of the first round of A/D conversion.

Hardware processing
A/D conversion is being executed.
Software processing
Wait until the ADST bit is cleared to 0 (polling by software).

④ End of the first round of A/D conversion

Hardware processing
Bit ADST has been cleared to 0, and the result of conversion transferred to ADDR.

⑤ Read the result of the first round of A/D conversion.

Software processing
Clear the ADS bit to 0.

⑥ Start the second round of A/D conversion.

Hardware processing
1. The ADST bit being set to 1 indicates that conversion is being executed by the ΔΣA/D converter. 2. Switch to the sleep (high-speed) mode.
Software processing
1. Set the ADS bit to 1 to start A/D conversion 2. Clear the IRRSAD bit to 0 and set the IENSAD bit to 1 to enable the A/D conversion end interrupt 3. Issue a SLEEP instruction to place the chip in the sleep (high-speed) mode.

⑦ End of the second round of A/D conversion

Hardware processing
1. The ADST bit is cleared to 0, and the result of conversion is transferred to ADDR. 2. The A/D conversion end interrupt request switches the chip from the sleep (high-speed) mode to the active (high-speed) mode.

⑧ Read the result of the second round of A/D conversion (A/D conversion end interrupt processing).

Software processing
1. Clear the IRRSAD bit to 0 and the IENSAD bit to 0. Disable the A/D conversion end interrupt. 2. Clear the ADS bit to 0 and read the result of conversion from ADDR.

Figure 4 Principle of Operation for Voltage Measurement by the ΔΣA/D converter (When Using the Internal Reference Voltage)

5. Description of software

5.1 Description of internal I/O register usage

Internal I/O registers used in this sample task are described below.

- A/D Data Register (ADDR) Address: H'F062

Bit	Bit Name	Initial value	R/W	Description
15	ADD13	—	R	16-bit read-only register that holds the results of A/D conversion. The 14 bits of A/D-converted data are stored in the higher-order 14 bits. The ADDR value during A/D conversion is undefined.
14	ADD12	—	R	
13	ADD11	—	R	
12	ADD10	—	R	
11	ADD9	—	R	
10	ADD8	—	R	
9	ADD7	—	R	
8	ADD6	—	R	
7	ADD5	—	R	
6	ADD4	—	R	
5	ADD3	—	R	
4	ADD2	—	R	
3	ADD1	—	R	
2	ADD0	—	R	
1	—	—	—	—
0	—	—	—	

- A/D Control Register (ADCR) Address: H'F060

Bit	Bit Name	Initial value	R/W	Description
7	MOD	0	R/W	Conversion Mode Select Sets the conversion mode. While the MOD bit is set to 1, A/D conversion is executed regardless of the value of the ADS bit in ADSSR. 0: Wait mode 1: Continuous mode
6	OVS2	0	R/W	Oversampling Frequency Select
5	OSV1	0	R/W	Select the oversampling frequency.
4	OVS0	0	R/W	000: φ 001: φ/2 010: φ/4 011: φ/8 100: φ/16 101: φ/32 11x: Setting prohibited
3	VREF1	1	R/W	PB5/Vref/REF Pin Function Switch and Reference Voltage
2	VREF0	1	R/W	Select Specify whether the PB5/Vref/REF pin functions as a PB5 pin, Vref pin, or REF pin. In addition, these bits select the external reference voltage (Vref) or internal reference voltage (REF) as the reference voltage for the ΔΣA/D converter. If REF is to be selected, set these bits after setting the BGRSTPN bit in BGRMR to 1 so that the BGR operates. 00: Functions as a PB5 input pin 01: Functions as a Vref input pin, and the external reference voltage (Vref) is input to the reference generator 10: Functions as a REF output pin 11: Functions as a REF output pin, and the internal reference voltage (REF) is input to the reference generator When these bits are set to B'11, the REF voltage is input to the reference voltage generator in the ΔΣA/D converter at the same timing as the internal reference voltage (REF) is output from the REF pin. To operate the ΔΣA/D converter with the internal reference voltage (REF), set these bits to B'11.
1	PGA1	0	R/W	PGA Gain Select
0	PGA0	0	R/W	Set the analog input voltage multiplication ratio to a value from 1/3 to 4. 00: 1 01: 2 10: 4 11: 1/3

Note: x: Don't care

- A/D Start/Status Register (ADSSR) Address: H'F061

Bit	Bit Name	Initial value	R/W	Description
7	ADS	1	R/W	A/D Start When this bit is set to 1 in wait mode (the MOD bit in ADCR is cleared to 0), A/D conversion is started.
6	ADST	—	R	A/D Status Flag When this bit is read in wait mode (the MOD bit in ADCR is cleared to 0), A/D conversion status can be identified. 0: In the idle state 1: A/D conversion in progress
5	AIN1	0	R/W	Analog Input Channel Select Select the analog input channel. 00: Not selected 01: Ain1 10: Ain2 11: Not selected
4	AIN0	1	R/W	
3	BYPGA	1	R/W	PGA Bypass Select Selects whether the analog input is to the PGA or second-order ΔΣA/D converter. 0: To the PGA 1: To the second-order ΔΣA/D converter
2	—	—	—	Reserved These bits cannot be modified.
1	—	—	—	
0	—	—	—	

- Interrupt Enable Register 2 (IENR2) Address: H'FFF4

Bit	Bit Name	Initial value	R/W	Description
5	IENSAD	1	R/W	ΔΣA/D Converter Interrupt Request Enable The ΔΣA/D converter interrupt request is enabled when this bit is set to 1. 0: ΔΣA/D converter interrupt request is disabled. 1: ΔΣA/D converter interrupt request is enabled.

- Interrupt request register 2 (IRR2) Address: H'FFF7

Bit	Bit Name	Initial value	R/W	Description
5	IRRSAD	0	R/(W)*	ΔΣA/D Converter Interrupt Request Flag [Setting condition] Completion of ΔΣA/D conversion [Clearing condition] Writing of 0 to this bit

Note: * The only effective write value is 0, which clears the flag.

- System Control Register 1 (SYSCR1) Address: H'FFF0

Bit	Bit Name	Initial value	R/W	Description
7	SSBY	0	R/W	Software Standby Selects the mode to be entered after execution of the SLEEP instruction. 0: The transition is to sleep mode or subsleep mode. 1: The transition is to standby mode or watch mode.
3	LSON	0	R/W	Low-Speed On Flag Selects the system clock (ϕ) or subclock (ϕ_{SUB}) as the CPU operating clock on exit from watch mode. 0: The CPU operates from the system clock (ϕ) 1: The CPU operates from the subclock (ϕ_{SUB})

- System Control Register 2 (SYSCR2) Address: H'FFF1

Bit	Bit Name	Initial value	R/W	Description
3	DTON	0	R/W	Direct Transfer on Flag Along with bits SSBY, TMA3, and LSON in SYSCR1 and bit MSON in SYSCR2, selects the mode to be entered after execution of the SLEEP instruction.
2	MSON	0	R/W	Medium Speed on Flag After standby, watch, or sleep mode is cleared, this bit selects active (high-speed) or active (medium-speed) mode.

- Clock Halt Register 1 (CKSTPR1) Address: H'FFFA

Bit	Bit Name	Initial value	R/W	Description
7	S4CKSTP	1	R/W*1	SCI4 Module Standby SCI4 enters standby mode when this bit is cleared to 0. 0: SCI4 is placed in module standby mode 1: SCI4 is taken out of module standby mode.
6	S31CKSTP	0	R/W	SCI3_1 Module Standby*2 SCI3_1 enters standby mode when this bit is cleared to 0. 0: SCI3_1 is placed in module standby mode. 1: SCI3_1 is taken out of module standby mode.
5	S32CKSTP	0	R/W	SCI3_2 Module Standby*2 SCI3_2 enters standby mode when this bit is cleared to 0. 0: SCI3_2 is placed in module standby mode 1: SCI3_2 is taken out of module standby mode.
4	ADCKSTP	0	R/W	A/D Converter Module Standby The A/D converter enters standby mode when this bit is cleared to 0. 0: The A/D converter is placed in module standby mode. 1: The A/D converter is taken out of module standby mode.
3	DADCKSTP	1	R/W	ΔΣA/D Converter Module Standby The ΔΣA/D converter enters standby mode when this bit is cleared to 0. 0: The ΔΣA/D converter is placed in module standby mode. 1: The ΔΣA/D converter is taken out of module standby mode.
2	TFCKSTP	0	R/W	Timer F Module Standby Timer F enters standby mode when this bit is cleared to 0. 0: Timer F is placed in module standby mode. 1: Timer F is taken out of module standby mode.
1	FROMCKSTP	1	R/W	Flash Memory Module Standby The flash memory enters standby mode when this bit is cleared to 0. 0: The flash memory is placed in module standby mode. 1: The flash memory is taken out of module standby mode.
0	RTCCKTP	0	R/W	RTC Module Standby The RTC enters standby mode when this bit is cleared to 0. 0: The RTC is placed in module standby mode. 1: The RTC is taken out of module standby mode.

Notes: *1. In the mask-programmed ROM version, this is a reserved bit which is not readable or writable.
*2. When SCI3 is put on module standby, all registers of SCI3 enter the reset state.

- Clock Halt Register 2 (CKSTPR2) Address: H'FFFB

Bit	Bit Name	Initial value	R/W	Description
7	ADBCKSTP	1	R/W	Address Break Module Standby The address break module enters standby mode when this bit is cleared to 0. 0: The address break module is placed in module standby mode. 1: The address break module is taken out of module standby mode.
6	TPUCKSTP	0	R/W	TPU Module Standby The TPU enters standby mode when this bit is cleared to 0. 0: The TPU is placed in module standby mode 1: The TPU is taken out of module standby mode.
5	IICCKSTP	0	R/W	IIC2 Module Standby The IIC2 module enters standby mode when this bit is cleared to 0. 0: The IIC2 module is placed in module standby mode. 1: The IIC2 module is taken out of module standby mode.
4	PW2CKSTP	0	R/W	PWM2 Module Standby The PWM2 module enters standby mode when this bit is cleared to 0. 0: The PWM2 module is placed in module standby mode. 1: The PWM2 module is taken out of module standby mode.
3	AECCKSTP	0	R/W	Asynchronous Event Counter Module Standby The asynchronous event counter enters standby mode when this bit is cleared to 0. 0: The asynchronous event counter is placed in module standby mode. 1: The asynchronous event counter is taken out of module standby mode.
2	WDCKSTP	0	R/W*	Watchdog Timer Module Standby The watchdog timer enters standby mode when this bit is cleared to 0. 0: The watchdog timer is placed in module standby mode 1: The watchdog timer counter is taken out of module standby mode.
1	PW1CKSTP	0	R/W	PWM1 Module Standby The PWM1 module enters standby mode when this bit is cleared to 0. 0: The PWM1 module is placed in module standby mode. 1: The PWM1 module is taken out of module standby mode.

Bit	Bit Name	Initial value	R/W	Description
0	LDCKSTP	0	R/W	LCD Module Standby The LCD controller/driver enters standby mode when this bit is cleared to 0. 0: The LCD controller/driver is placed in module standby mode. 1: The LCD controller/driver is taken out of module standby mode.

Note: * This bit is valid when the WDON bit in TCSRWD1 is 0. If this bit is cleared to 0 while the WDON bit is set to 1 (i.e. while the watchdog timer is operating), the bit is cleared but the watchdog timer does not enter module standby mode; instead, it continues to operate. When the watchdog timer stops operating and the WDON bit is cleared to 0 by software, this bit is fully effective and the watchdog timer enters module standby mode.

- BGR control register (BGRMR) Address: H'FFA4

Bit	Bit Name	Initial value	R/W	Description
7	BGRSTPN*	1	R/W	Band-Gap Reference Circuit Control Makes the band-gap reference circuit operate or stop 0: Band-gap reference circuit stops 1: Band-gap reference circuit operates
6 to 3	—	—	—	Reserved These bits are always read as 1 and cannot be modified.
2	BTRM2	0	R/W	BGR Output Voltage Trimming Adjust the approximately 1.2-V BGR output voltage. 000: ±0 V 001: +0.14 V 010: +0.09 V 011: +0.04 V 100: –0.04 V 101: –0.09 V 110: –0.14 V 111: –0.18 V
1	BTRM1	0	R/W	
0	BTRM0	0	R/W	

Note: * When the BGRSTPN bit is 0 (when the band-gap reference circuit is halted), the 3-V constant-voltage power supply circuit of the LCD is halted.
The time from the point at which the BGRSTPN bit is set to 1 until the BGR output voltage is stabilized to approximately 1.2 V is approximately 70 µs.

- Timer Counter FH (TCFH) Address: H'FFB8

Bit	Bit Name	Initial value	R/W	Description
7	TCFH7	0	R/W	When CKSH2 in TCRF is set to 1, TCRF operates as an independent 8-bit counter. The TCFH input clock is selected by bits CKSH2 to CKSH0 in TCRF. Clearing of TCFH on a compare-match can be specified by bit CCLRH in TCSRF. When TCFH overflows (changes from H'FF to H'00), OVFH in TCSRF is set to 1. If OVIEH in TCSRF is 1 at this time, IRRTFH in IRR2 is set to 1; if IENTFH in IENR2 is also set to 1, an interrupt request is sent to the CPU.
6	TCFH6	0	R/W	
5	TCFH5	0	R/W	
4	TCFH4	0	R/W	
3	TCFH3	0	R/W	
2	TCFH2	0	R/W	
1	TCFH1	0	R/W	
0	TCFH0	0	R/W	

- Timer Control Register F (TCRF) Address: H'FFB6

Bit	Bit Name	Initial value	R/W	Description
6	CKSH2	1	W	Clock Select H
5	CKSH1	0	W	Select the input for counting by TCFH as a clock signal or overflow of TCFL.
4	CKSH0	0	W	000: 16-bit mode, counting of TCFL overflow signal cycles 001: 16-bit mode, counting of TCFL overflow signal cycles 010: 16-bit mode, counting of TCFL overflow signal cycles 011: Using prohibited 100: 8-bit mode, counting of ϕ/32 cycles 101: 8-bit mode, counting of ϕ/16 cycles 110: 8-bit mode, counting of ϕ/8 cycles 111: 8-bit mode, counting of ϕ_w/4 cycles

- Timer Control Status Register F (TCSRF) Address: H'FFB7

Bit	Bit Name	Initial value	R/W	Description
7	OVFH	0	R/W*	Timer Overflow Flag H [Setting condition] Overflow of TCFH (change from H'FF to H'00) [Clearing condition] Writing of 0 to this bit after having read it as 1

Note: * Only 0 can be written here, to clear the flag.

5.2 Description of modules

Table 4 gives descriptions of the modules used in this sample task.

Table 4 Description of modules

Module Name	Function
main ( )	Main Routine Initial settings of the ΔΣA/D converter. Waits for the end of the first round of ΔΣA/D conversion, enables the ΔΣA/D conversion end interrupt request, and places the chip in the sleep (high-speed) mode.
int_dsadc ( )	ΔΣA/D converter interrupt processing routine Clears the ΔΣA/D converter interrupt request flag, disables the ΔΣA/D converter interrupt request, and stores the result of A/D conversion in RAM.

5.3 RAM usage

Table 5 shows the description of RAM usage in this sample task.

Table 5 Description of RAM Usage

Label Name	Function	Data Size	Address	Module Name
ad_result	Shifts the results of ΔΣA/D conversion 2 bits right for treatment as 14-bit data.	unsigned short (2 bytes)	H'F780	main ( ) int_dsadc ( )

5.4 Link address settings

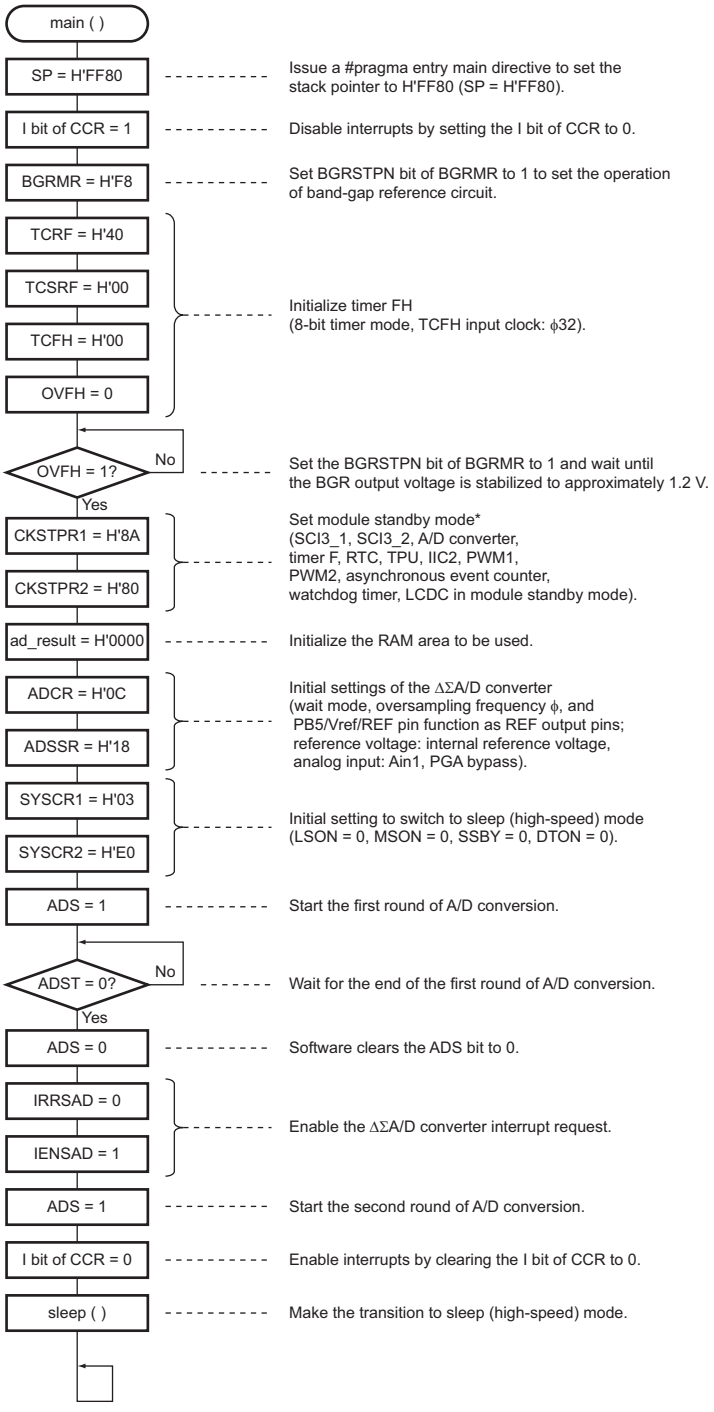
Table 6 shows the link addresses used in this sample task.

Table 6 Link Address Setting

Section Name	Address
CVECT	H'0000
P	H'0100
B	H'F780

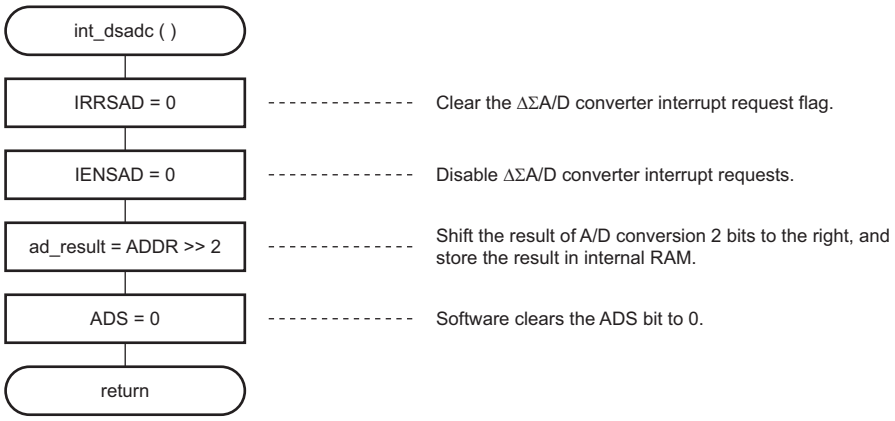
6. Flowcharts

6.1 Main routine



Note: * In this sample task, all internal peripheral modules other than SCI4, the flash memory, address break, and ΔΣA/D converter are placed in module standby mode. Write 1 rather than 0 to any bits of the clock stop register that correspond to other peripheral modules you might require.

6.2 ΔΣA/D converter interrupt processing routine



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