M16C/5LD, 5L, 5M, 6C Groups

Outputting a 16-Bit PWM Waveform Using Timer S in Single-Phase Waveform Output Mode

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Abstract

This document describes a method for outputting a 16-bit PWM waveform using timer S in single-phase waveform output mode with the M16C/5LD, 5L, 5M, and 6C Group microcomputers (MCUs).

Products

MCUs: M16C/5LD, 5L, 5M, 6C Groups

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Introduction

Timer S has an input capture/output compare function (IC/OC). The input capture (IC) is used for time measurement and the output compare (OC) is used for waveform generation. The IC/OC has one 16-bit free-running base timer and eight channels for timer measurement and waveform generation.

1.1 Waveform Generation Function

Waveforms are generated based on the values of the base timer and the G1POj register (j = 0 to 7). Table 1.1 lists the Waveform Generation Function Settings. Items marked with a check mark (✓) are described in this chapter.

Table 1.1 Waveform Generation Function Settings

Item	Setting	
Waveform generation function	✓	Single-phase waveform output mode
		Inverted waveform output mode
		Set/reset waveform output mode (SR waveform output mode)
Base timer reset source	✓	Base timer is reset when the base timer and G1BTRR register values match
		Base timer is reset when the base timer and G1PO0 register values match
		Base timer is reset when the input level to the $\overline{\text{INT1}}$ pin is low
Initial output level selection	✓	Output low as default level
		Output high as default level
Output level inversion selection	✓	Output level not inverted
		Output level inverted
Channels	✓	Channel 0
	✓	Channel 1
		Channel 2
		Channel 3
	✓	Channel 4
	✓	Channel 5
		Channel 6
		Channel 7
Interrupts	✓	IC/OC base timer interrupt
		IC/OC interrupt 0
		IC/OC interrupt 1
		IC/OC channel 0 interrupt
		IC/OC channel 1 interrupt
		IC/OC channel 2 interrupt
		IC/OC channel 3 interrupt

1.2 Single-Phase Waveform Output Mode

When the base timer and G1POj register values match, if the INV bit in the G1POCRj register is 0 (output level not inverted), the output level from the OUTC1_j pin becomes high (j = 0, 1, 4, 5). When the base timer becomes 0000h, the OUTC1_j pin outputs a low level. When using single-phase waveform output mode, set the base timer to increment mode.

The following is an explanation for setting the PWM period using the G1BTRR register, and setting the low width using the G1POj register (j = 0 to 7). PWM waveforms are output from the OUTC1_j pin corresponding to channel j. fBT1 is the operating clock for the base timer.

(1) PWM period setting

The base timer is reset when the base timer and G1BTRR register values match. At the same time, if the INV bit in the G1POCRj register is 0, the OUTC1_j pin outputs a low level. If the G1BTRR register setting value is n, the PWM period is as follows:

PWM period: $\frac{n + 2}{fBT1}$

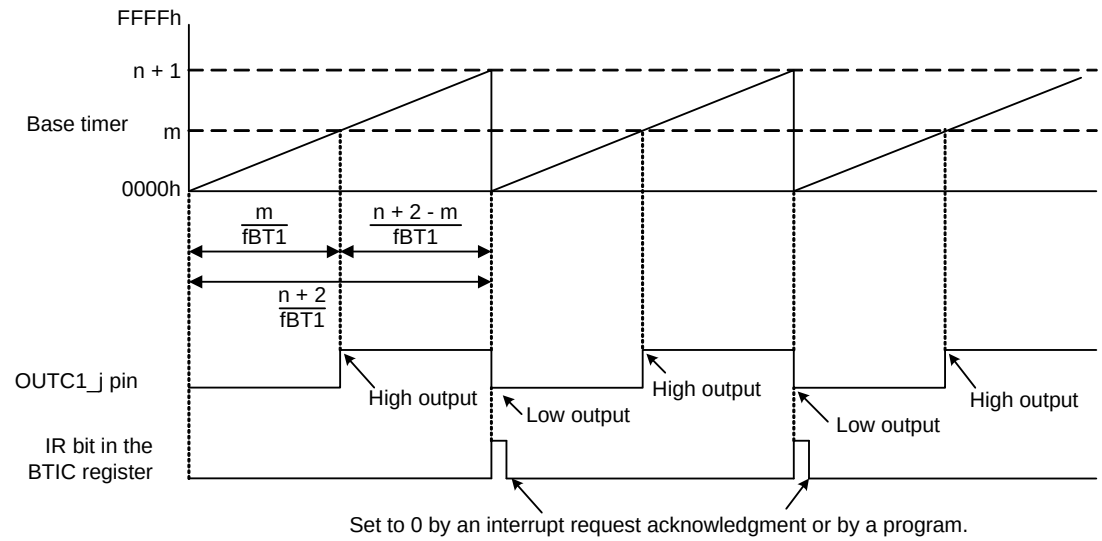
When changing the period, change the G1BT register in the interrupt handling without changing the G1BTRR register, or set the BTS bit in the G1BCR1 register to 0 before changing the G1BTRR register.

(2) Low width (initial output level width) setting

Set the low width in the G1POj register. If the G1POj register setting value is m, the PWM waveform low width is as follows:

Low width: $\frac{m}{fBT1}$

Figure 1.1 shows the operation of single-phase waveform output mode when the base timer is reset by the base timer and G1BTRR register values matching.



j = 0 to 7
m: G1POj register setting value
n: G1BTRR register setting value

The above diagram assumes the following:
- The RST4 bit in the G1BCR0 register is 1 (the base timer is reset when the base timer and G1BTRR register values match).
- The RST2 bit in the G1BCR1 register is 0 (the base timer is not reset when low is input to the $\overline{INT1}$ pin), and the RST1 bit is 0 (the base timer is not reset when the base timer and G1PO0 register values match).
- The IVL bit in the G1POCRj register is 0 (output low as default value), and the INV bit is 0 (output level not inverted).
- Bits IOj1 and IOj0 in registers G1IOR0 and G1IOR1 are 00b (outputs high or low, depending on the mode selected by bits MOD1 and MOD0 in the G1POCRj register).
- The EOCj bit in the G1OER register is 0 (output enabled).

Figure 1.1 Single-Phase Waveform Output Mode Operation

2. Software

2.1 Operation Overview

The OUTC1_k (P2_k) pin is used by timer S and outputs a PWM waveform (k = 0, 1, 4, 5). Every five times a base timer interrupt is generated, the G1POk register is rewritten in the base timer interrupt handler and the low width is changed.

Clock statistics are as follows:

- Main clock: 20 MHz
- Base timer operating clock (fBT1): 1 MHz

Figure 2.1 shows the Pin Output, and Table 2.1 lists the Low Width Setting Values.

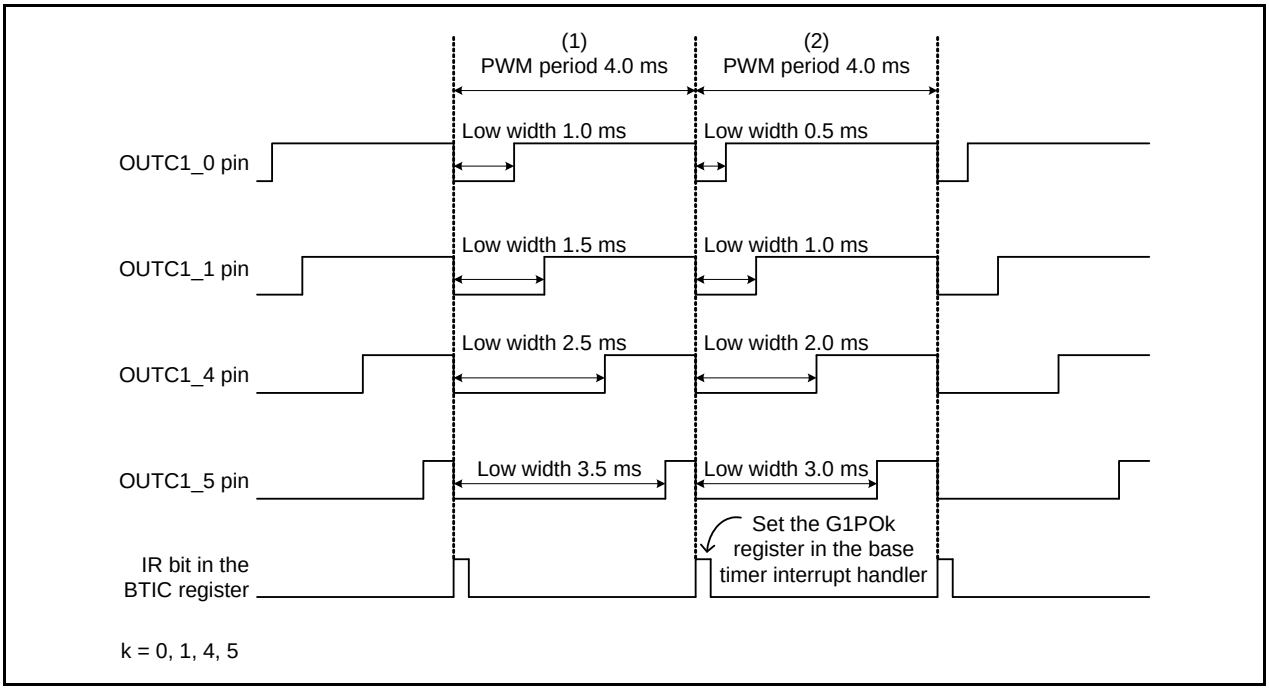


Figure 2.1 Pin Output

Table 2.1 Low Width Setting Values

Output Pin	Register	Low Width: $\frac{m}{fBT1}$	
		(1)	(2)
OUTC1_0 (P2_0)	G1PO0	1.0 ms (m = 1000)	0.5 ms (m = 500)
OUTC1_1 (P2_1)	G1PO1	1.5 ms (m = 1500)	1.0 ms (m = 1000)
OUTC1_4 (P2_4)	G1PO4	2.5 ms (m = 2500)	2.0 ms (m = 2000)
OUTC1_5 (P2_5)	G1PO5	3.5 ms (m = 3500)	3.0 ms (m = 3000)

2.2 Flowcharts

2.2.1 Main Processing

Figure 2.2 shows the Main Processing.

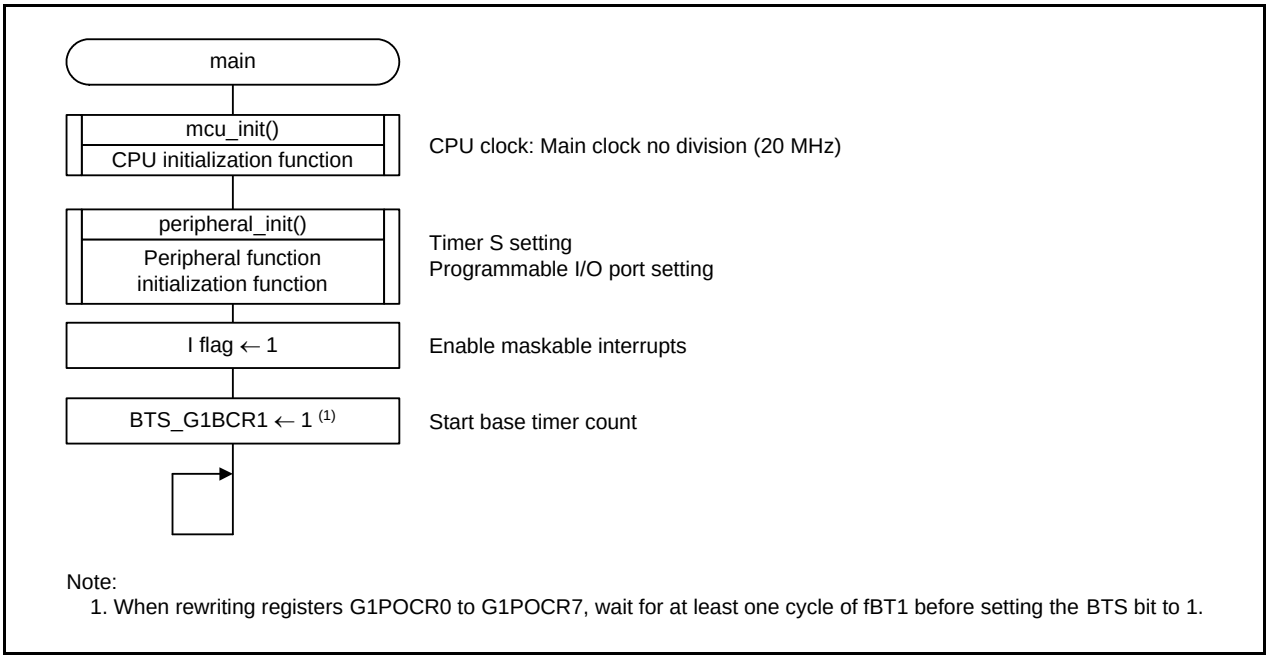
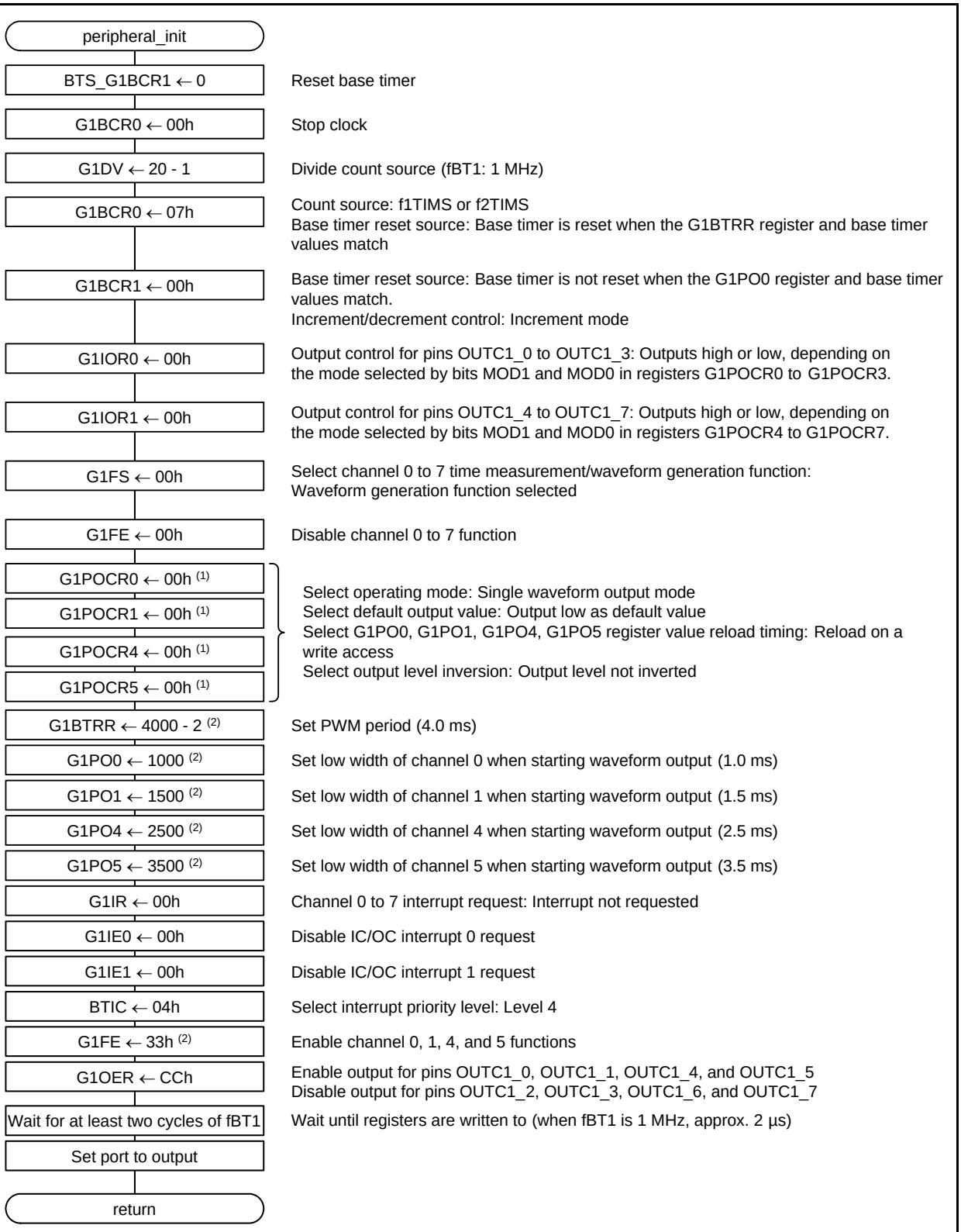


Figure 2.2 Main Processing

2.2.2 Peripheral Function Initialization Function

Figure 2.3 shows the Peripheral Function Initialization Function.



Notes:
1. When rewriting this register, after waiting for at least one cycle of fBT1, set the BTS bit to 1.
2. The values written to these registers are simultaneously reflected to the base timer count source (fBT1).

Figure 2.3 Peripheral Function Initialization Function

2.2.3 Base Timer Interrupt Handling Function

Figure 2.4 shows the Base Timer Interrupt Handling Function.

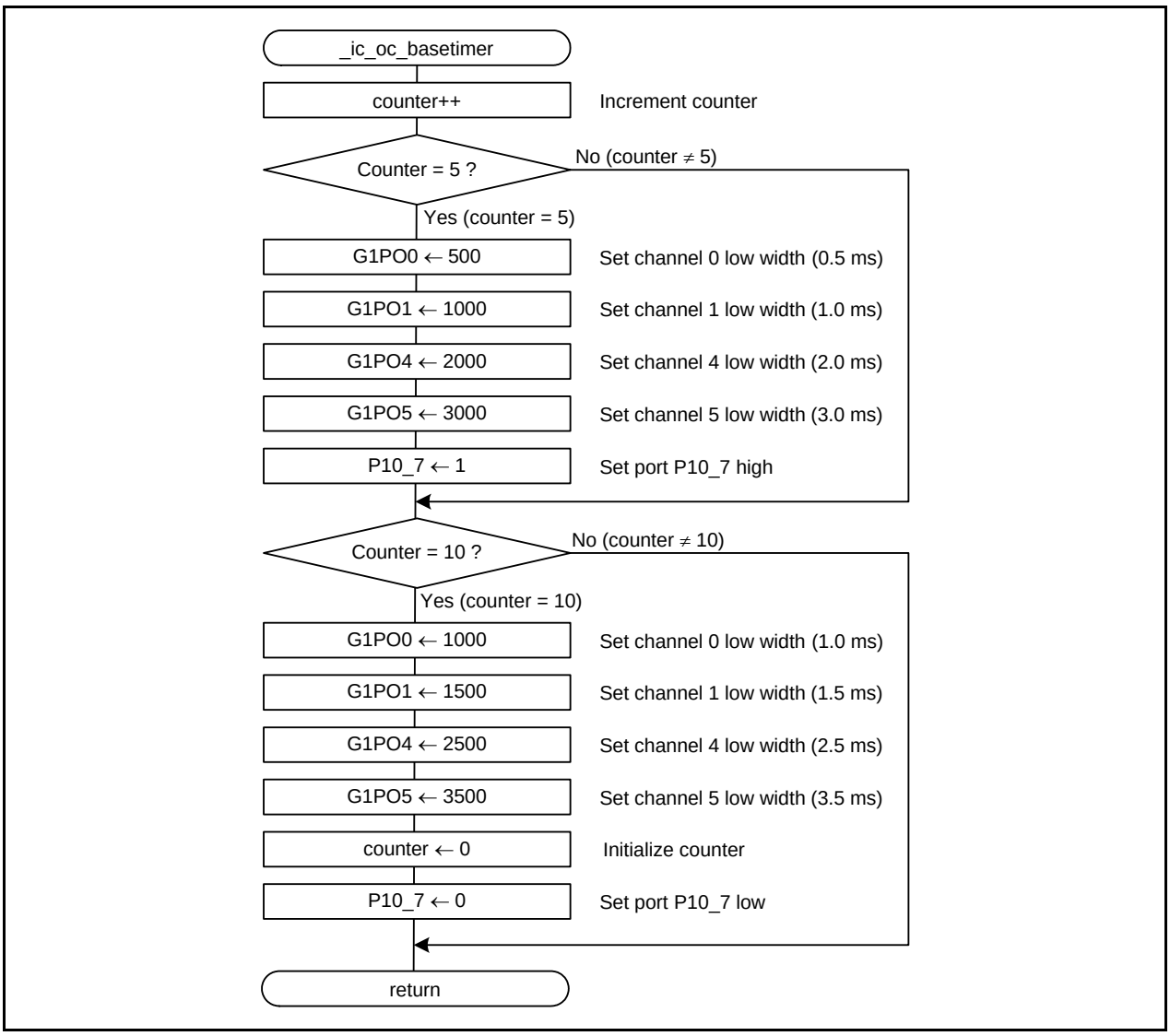


Figure 2.4 Base Timer Interrupt Handling Function

3. Application Example

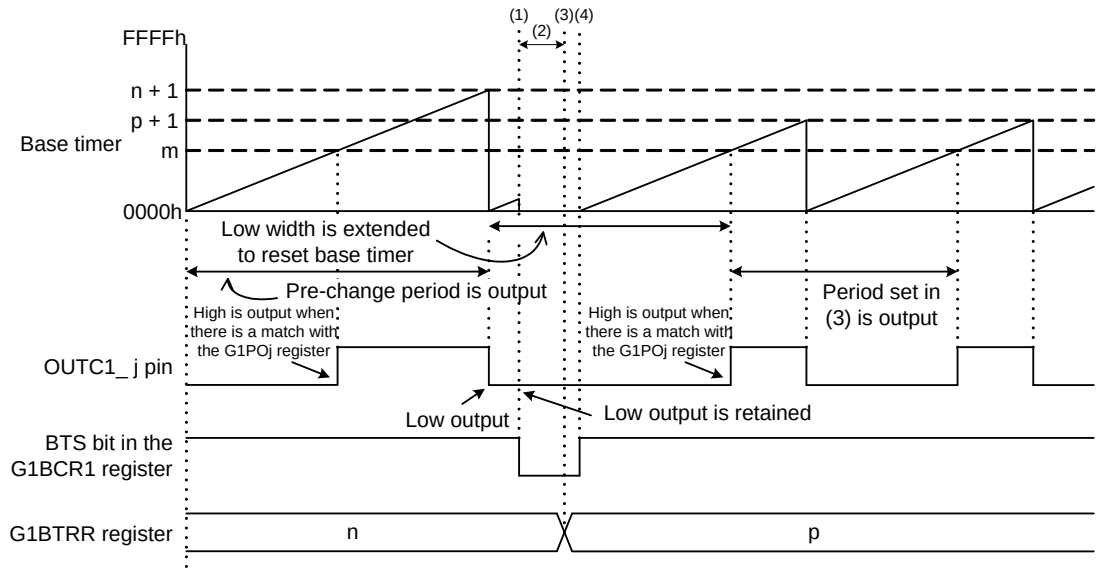
3.1 Changing the Period

The PWM output period can be set using the G1BTRR register when the RST4 bit in the G1BCR0 register is 1, or it can be set using the G1PO0 register when the RST1 bit in the G1BCR1 register is 1. When changing the period during a count operation, after setting the BTS bit in the G1BCR1 register to 0 (base timer reset), wait at least one cycle of fBT1, and rewrite the G1BTRR or G1PO0 register. The procedure is as follows:

(1) Set the BTS bit to 0. (1)
(2) Wait at least one cycle of fBT1.
(3) Rewrite the register where the period was set.
(4) Set the BTS bit to 1.

Note:
1. One cycle of fBT1 passes between setting the BTS bit to 0 and the count stopping.

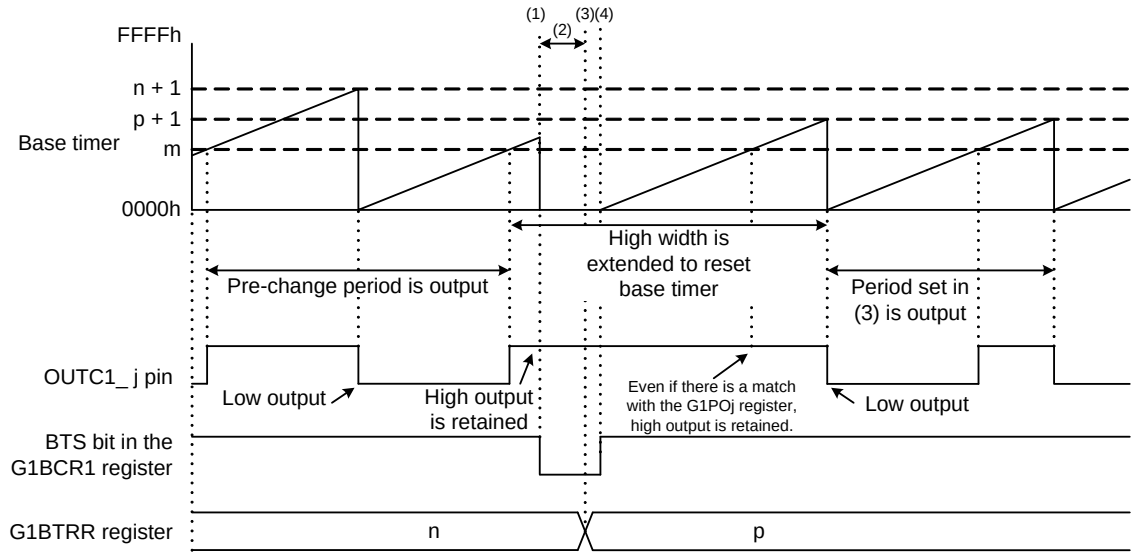
Figure 3.1 shows Output when Changing the Period While Outputting Low. Figure 3.2 shows Output when Changing the Period While Outputting High.



j = 0 to 7
m: G1POj register setting value
n and p: G1BTRR register setting values

The above diagram assumes the following:
- The RST4 bit in the G1BCR0 register is 1 (the base timer is reset when the base timer and G1BTRR register values match).
- The RST2 bit in the G1BCR1 register is 0 (the base timer is not reset when low is input to the $\overline{\text{INT1}}$ pin), and the RST1 bit is 0 (the base timer is not reset when the base timer and G1PO0 register values match).
- Bits MOD1 and MOD0 in the G1POCRj register are 00b (single waveform output mode), the IVL bit is 0 (output low as default value), and the INV bit is 0 (output level not inverted).
- Bits IOj1 and IOj0 in registers G1IOR0 and G1IOR1 are 00b (outputs high or low, depending on the mode selected by bits MOD1 and MOD0 in the G1POCRj register).
- The EOCj bit in the G1OER register is 0 (output enabled).

Figure 3.1 Output when Changing the Period While Outputting Low



j = 0 to 7
m: G1POj register setting value
n and p: G1BTRR register setting values

The above diagram assumes the following:

- The RST4 bit in the G1BCR0 register is 1 (the base timer is reset when the base timer and G1BTRR register values match).
- The RST2 bit in the G1BCR1 register is 0 (the base timer is not reset when low is input to the $\overline{\text{INT1}}$ pin), and the RST1 bit is 0 (the base timer is not reset when the base timer and G1PO0 register values match).
- Bits MOD1 and MOD0 in the G1POCRj register are 00b (single waveform output mode), the IVL bit is 0 (output low as default value), and the INV bit is 0 (output level not inverted).
- Bits IOj1 and IOj0 in registers G1IOR0 and G1IOR1 are 00b (outputs high or low, depending on the mode selected by bits MOD1 and MOD0 in the G1POCRj register).
- The EOCj bit in the G1OER register is 0 (output enabled).

Figure 3.2 Output when Changing the Period While Outputting High

4. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

5. Reference Documents

M16C/5LD, M16C/56D Group User's Manual: Hardware Rev.1.10
M16C/5L, M16C/56 Group User's Manual: Hardware Rev.1.00
M16C/5M, M16C/57 Group User's Manual: Hardware Rev.1.01
M16C/6C Group User's Manual: Hardware Rev.2.00
The latest versions can be downloaded from the Renesas Electronics website.

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C Compiler Manual
M16C Series, R8C Family C Compiler Package V.5.45
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Revision History	M16C/5LD, 5L, 5M, 6C Groups Outputting a 16-Bit PWM Waveform Using Timer S in Single-Phase Waveform Output Mode

Rev.	Date	Description	
		Page	Summary
1.00	Sep. 30, 2010	—	First edition issued
1.01	June 30, 2011	—	Added chapter 3

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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