M16C/63,64A,64C,65,65C,6C,5LD,56D,5L,56,5M,57 Groups

Operation of Serial I/O (Reception in Clock-Synchronous Serial I/O Mode)

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1. Abstract

In receiving data in clock-synchronous serial I/O mode, choose functions from those listed in Table 3.1. Operations of the marked items are described below. The examples are explained below using the M16C/65 Group.

2. Introduction

This application note is applied to the following MCUs:

MCU(s): M16C/63, 64A, 64C, 65, 65C, 6C, 5LD, 56D, 5L, 56, 5M, 57 Groups

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above groups. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Chosen Function

Table 3.1 Chosen Functions

Item	Set-up		Item	Set-up	
Transfer clock source		Internal clock (f1SIO/f2SIO/f8SIO/f32SIO)	Continuous receive mode	✓	Disabled
	✓	External clock (CLKi pin)			Enabled
$\overline{\text{RTS}}$ function	✓	$\overline{\text{RTS}}$ function enabled	Output transfer clock to multiple pins (1)	✓	Not selected
		$\overline{\text{RTS}}$ function disable			Selected
CLK polarity	✓	Input reception data at the rising edge of the transfer clock	Data logic select function	✓	No reverse
		Input reception data at the falling edge of the transfer clock			Reverse
Transfer clock	✓	LSB first	Separate $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ pins (2)	✓	Shared pin
		MSB first			Separated

Notes:
1. This can be selected only when UART1 is used in combination with the internal clock. When this function is selected, UART1 $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function can not be utilized. Set the UART1 $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ disable bit to “1”.
2. This function separates $\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$, outputs $\overline{\text{RTS0}}$ from the P6_0 pin, and inputs $\overline{\text{CTS0}}$ from the P6_4 pin. When this function is selected, UART1 $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function can not be utilized. Set the UART1 $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ disable bit to “1”.

4. Operation

(1) Writing dummy data to the UARTi transmit buffer register, setting the receive enable bit to “1”, and the transmit enable bit to “1”, makes the data receivable status ready. At this time, the output from the $\overline{\text{RTSi}}$ pin goes to “L” level, which informs the transmission side that the data receivable status is ready (output the transfer clock from the IC on the transmission side after checking that the $\overline{\text{RTS}}$ output has gone to “L” level).

(2) In synchronization with the first rising edge of the transfer clock, the input signal to the RxDi pin is stored in the highest bit of the UARTi receive register. Then, data is taken in by shifting right the content of the UARTi reception data in synchronization with the rising edges of the transfer clock.

(3) When 1-byte data lines up in the UARTi receive register, the content of the UARTi receive register is transmitted to the UARTi receive buffer register. The transfer clock stops at “H” level. At this time, the receive complete flag and the UARTi receive interrupt request bit goes to “1”.

(4) The receive complete flag goes to “0” when the lower-order byte of the UARTi buffer register is read.

Figure 4.1 shows the operation timing.

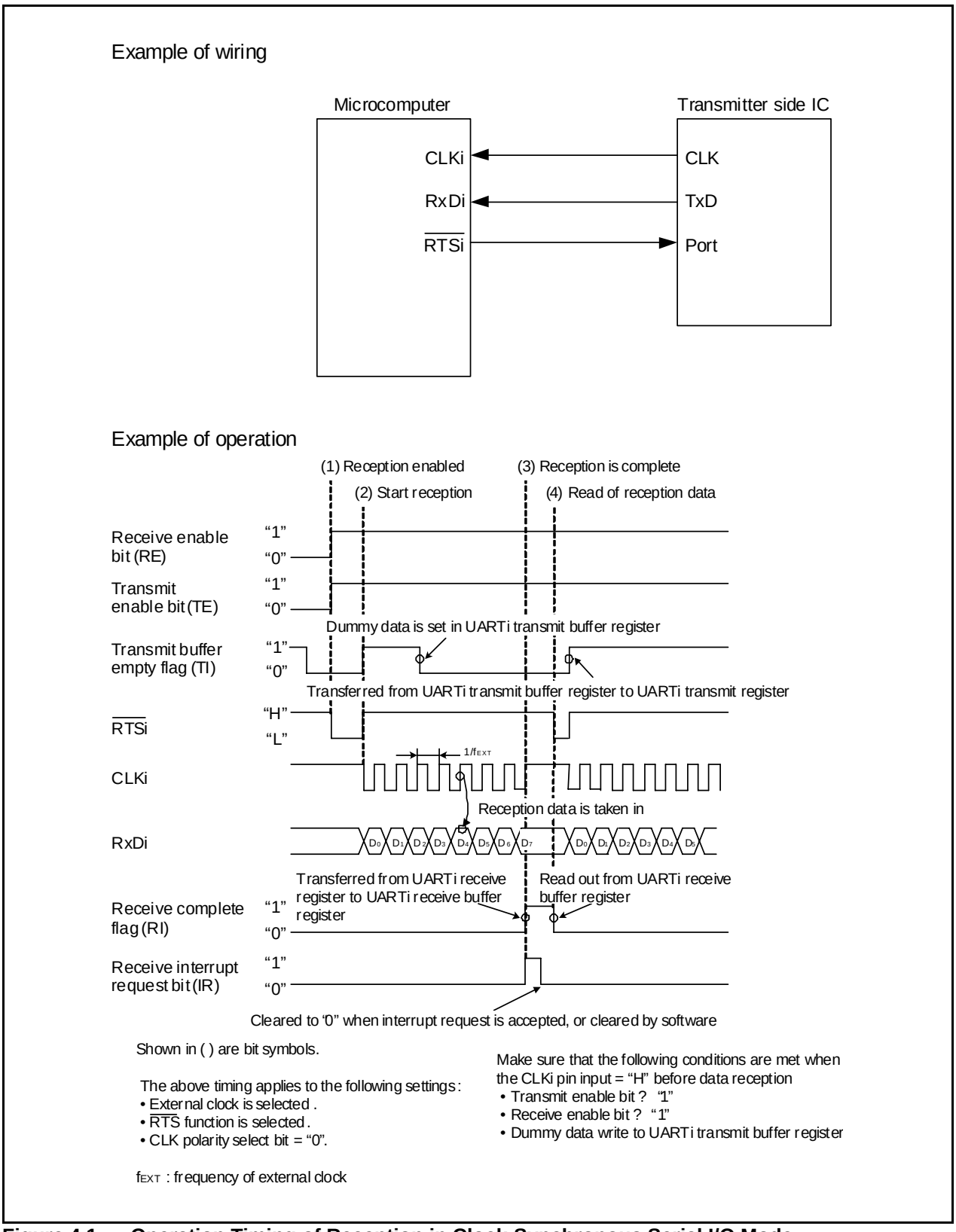
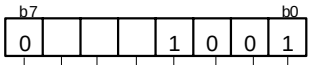


Figure 4.1 Operation Timing of Reception in Clock-Synchronous Serial I/O Mode

5. Set-up Procedure

Setting UARTi transmit/receive mode register (i = 0 to 2, 5 to 7)



UART0 transmit/receive mode register [Address 0248h] U0MR
UART1 transmit/receive mode register [Address 0258h] U1MR
UART2 transmit/receive mode register [Address 0268h] U2MR
UART5 transmit/receive mode register [Address 0288h] U5MR
UART6 transmit/receive mode register [Address 0298h] U6MR
UART7 transmit/receive mode register [Address 02A8h] U7MR

Must be fixed to "001"

Internal/external clock select bit
1 : External clock

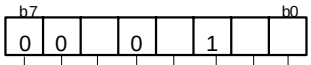
Invalid in clock synchronous I/O mode

Invalid in clock synchronous I/O mode

Invalid in clock synchronous I/O mode

TxD, RxD I/O polarity reverse bit
Usually set to "0"

Setting UARTi transmit/receive control register (i = 0 to 2, 5 to 7)



UART0 transmit/receive control register [Address 024Ch] U0C0
UART1 transmit/receive control register [Address 025Ch] U1C0
UART2 transmit/receive control register [Address 026Ch] U2C0
UART5 transmit/receive control register [Address 028Ch] U5C0
UART6 transmit/receive control register [Address 029Ch] U6C0
UART7 transmit/receive control register [Address 02ACh] U7C0

UiBRG count source select bit

b1 b0
0 0 : f_{1SIO} or f_{2SIO} is selected (Note1)
0 1 : f_{8SIO} is selected
1 0 : f_{32SIO} is selected
1 1 : Do not set to this value

CTS/RTS function select bit (Valid when bit4 = "0")
1 : RTS function is selected (Note2)

Transmit register empty flag
0 : Data present in transmit register (during transmission)
1 : No data present in transmit register (transmission completed)

CTS/RTS disable bit
0 : CTS/RTS function enabled

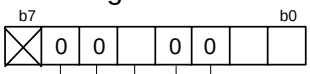
Data output select bit
0 : Pins TxDi/SDAi and SCLi are CMOS output
1 : Pins TxDi/SDAi and SCLi are N-channel opendrain output

CLK polarity select bit
0 : Transmission data is output at falling edge of transfer clock and reception data is input at rising edge

Transfer format select bit
0 : LSB first

Note 1: When the PCLK1bit in the PCLKR register is "1", the selected clock source is f_{1SIO}. When the PCLK1 bit is "0", the selected clock source is f_{2SIO}.
Note 2: Set the corresponding port direction register to "1" (output mode).

Setting UART transmit/receive control register 2



UART transmit/receive control register 2 [Address 0250h] UCON

UART0 continuous receive mode enable bit
0 : Continuous receive mode disabled

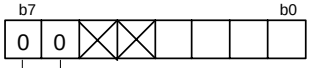
UART1 continuous receive mode enable bit
0 : Continuous receive mode disabled

Valid when bit5 = "1"

UART1 CLK/CLKS select bit 1
0 : CLK output is only from CLK1

Separate UART0 $\overline{CTS}/\overline{RTS}$ bit
0 : $\overline{CTS}/\overline{RTS}$ shared pin

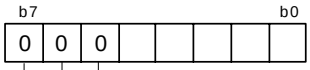
Setting UARTi transmit/receive control register 1 (i = 0 to 2, 5 to 7)



UART0 transmit/receive control register 1 [Address 024Dh] U0C1
UART1 transmit/receive control register 1 [Address 025Dh] U1C1

Data logic select bit
0 : No reverse

Error signal output enable bit
Must always be "0" in clock synchronous I/O mode



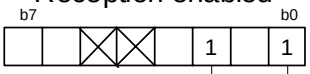
UART2 transmit/receive control register 1 [Address 026Dh] U2C1
UART5 transmit/receive control register 1 [Address 028Dh] U5C1
UART6 transmit/receive control register 1 [Address 029Dh] U6C1
UART7 transmit/receive control register 1 [Address 02ADh] U7C1

UARTi continuous receive mode enable bit
0 : Continuous receive mode disable

Data logic select bit
0 : No reverse

Error signal output enable bit
Must always be "0" in clock synchronous I/O mode

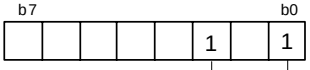
Reception enabled



UART0 transmit/receive control register 1 [Address 024Dh] U0C1
UART1 transmit/receive control register 1 [Address 025Dh] U1C1

Transmit enable bit
1 : Transmission enabled

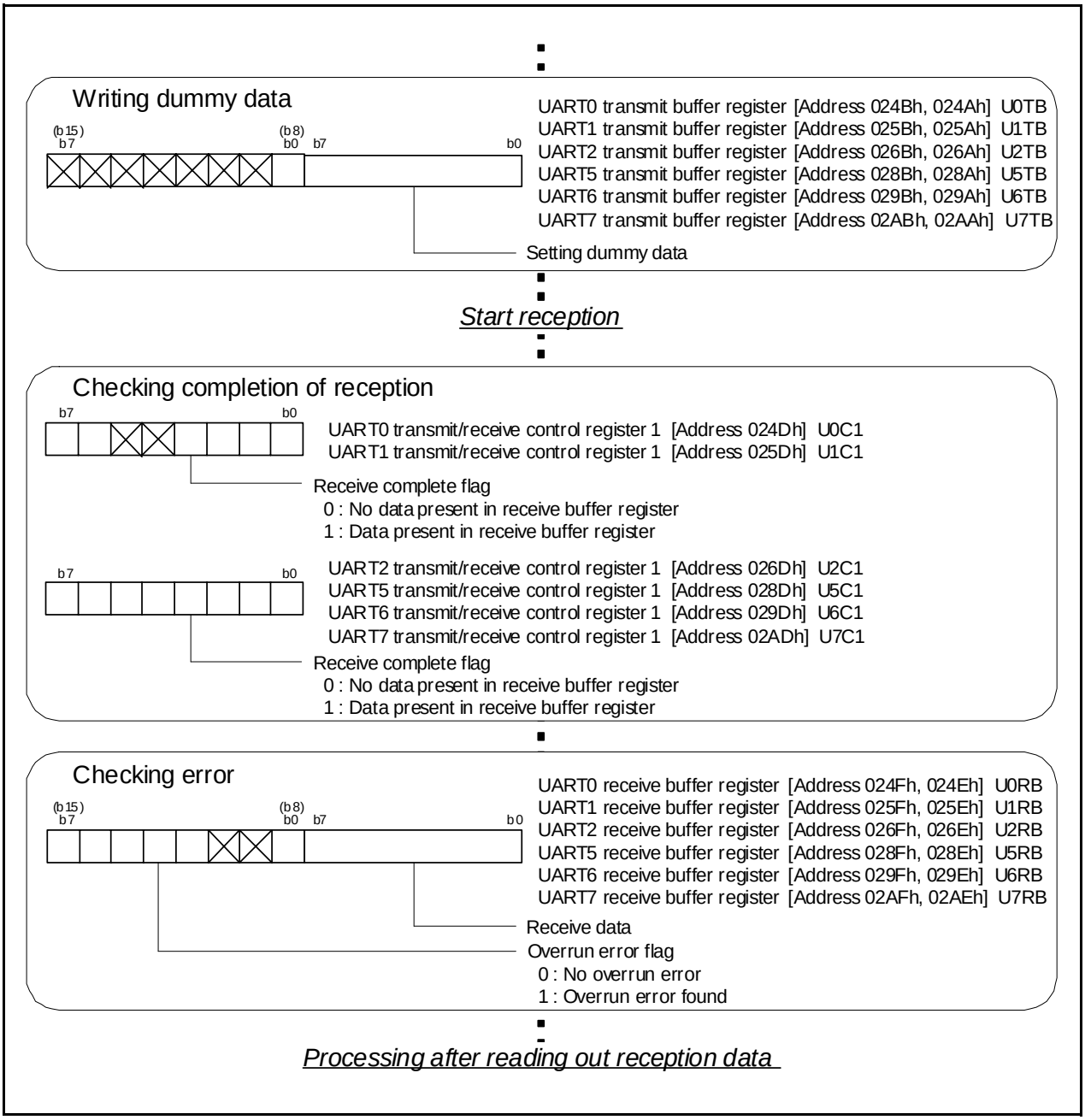
Receive enable bit
1 : Reception enabled



UART2 transmit/receive control register 1 [Address 026Dh] U2C1
UART5 transmit/receive control register 1 [Address 028Dh] U5C1
UART6 transmit/receive control register 1 [Address 029Dh] U6C1
UART7 transmit/receive control register 1 [Address 02ADh] U7C1

Transmit enable bit
1 : Transmission enabled

Receive enable bit
1 : Reception enabled


Writing dummy data
(b15) b7
(b8) b0
b7
b0
UART0 transmit buffer register [Address 024Bh, 024Ah] U0TB
UART1 transmit buffer register [Address 025Bh, 025Ah] U1TB
UART2 transmit buffer register [Address 026Bh, 026Ah] U2TB
UART5 transmit buffer register [Address 028Bh, 028Ah] U5TB
UART6 transmit buffer register [Address 029Bh, 029Ah] U6TB
UART7 transmit buffer register [Address 02ABh, 02AAh] U7TB
Setting dummy data
Start reception
Checking completion of reception
b7
b0
UART0 transmit/receive control register 1 [Address 024Dh] U0C1
UART1 transmit/receive control register 1 [Address 025Dh] U1C1
Receive complete flag
0 : No data present in receive buffer register
1 : Data present in receive buffer register
UART2 transmit/receive control register 1 [Address 026Dh] U2C1
UART5 transmit/receive control register 1 [Address 028Dh] U5C1
UART6 transmit/receive control register 1 [Address 029Dh] U6C1
UART7 transmit/receive control register 1 [Address 02ADh] U7C1
Receive complete flag
0 : No data present in receive buffer register
1 : Data present in receive buffer register
Checking error
UART0 receive buffer register [Address 024Fh, 024Eh] U0RB
UART1 receive buffer register [Address 025Fh, 025Eh] U1RB
UART2 receive buffer register [Address 026Fh, 026Eh] U2RB
UART5 receive buffer register [Address 028Fh, 028Eh] U5RB
UART6 receive buffer register [Address 029Fh, 029Eh] U6RB
UART7 receive buffer register [Address 02AFh, 02AEh] U7RB
Receive data
Overrun error flag
0 : No overrun error
1 : Overrun error found
Processing after reading out reception data

6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

M16C/63 Group User's Manual: Hardware Rev.2.00
M16C/64A Group User's Manual: Hardware Rev.2.00
M16C/64C Group User's Manual: Hardware Rev.1.00
M16C/65 Group User's Manual: Hardware Rev.2.00
M16C/65C Group User's Manual: Hardware Rev.1.00
M16C/6C Group User's Manual: Hardware Rev.2.00
M16C/5LD Group, M16C/56D Group User's Manual: Hardware Rev.1.10
M16C/5L Group, M16C/56 Group User's Manual: Hardware Rev.1.00
M16C/5M Group, M16C/57 Group User's Manual: Hardware Rev.1.01
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
M16C Series, R8C Family C Compiler Package V.5.45
C Compiler User's Manual Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

8. Website and Support

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Revision History	M16C/63,64A,64C,65,65C,6C,5LD,56D,5L,56,5M,57 Groups Operation of Serial I/O (Reception in Clock-Synchronous Serial I/O Mode)

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		Page	Summary
1.00	Oct. 30, 2009	—	First edition issued
1.01	Apr. 28, 2011	—	Add: M16C/63, M16C/64A, M16C/64C, M16C/65C, M16C/6C, M16C/5LD, M16C/56D, M16C/5L, M16C/56, M16C/5M, and M16C/57

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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