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H8S/20103, H8S/20203, and H8S/20223 Groups

Initial Setting for External Oscillation and Release of All Modules from Standby Mode

Introduction

After an MCU of the H8S/20103, H8S/20203, and H8S/20223 Groups is released from the reset state, the watchdog timer (WDT) operates, the base clock source is the low-speed on-chip oscillator (OCO), and the on-chip modules are placed on standby. The task covered by this application note stops the WDT, switches to an external oscillator as the base clock for the chip, and releases all on-chip modules from the standby state.

Target Devices

H8S/20103 (R4F20103)

H8S/20203 (R4F20203)

H8S/20223 (R4F20223)

Frequency Used in Confirming Operation

System clock $\phi = \phi osc = 20$ MHz

Contents

1. Specifications

Specifications of this sample task are given below. Figure 1 shows a state transition diagram for the LSI system's base clock.

(1) Immediately after an MCU of the H8S/20103, H8S/20203, and H8S/20223 Groups is released from the reset state, the WDT operates, the base clock source is the low-speed OCO, and the on-chip modules are placed on standby.
(2) The WDT is released from standby and is halted.
(3) The base clock is changed from the low-speed OCO to the main oscillator clock.
(4) All modules are released from standby.

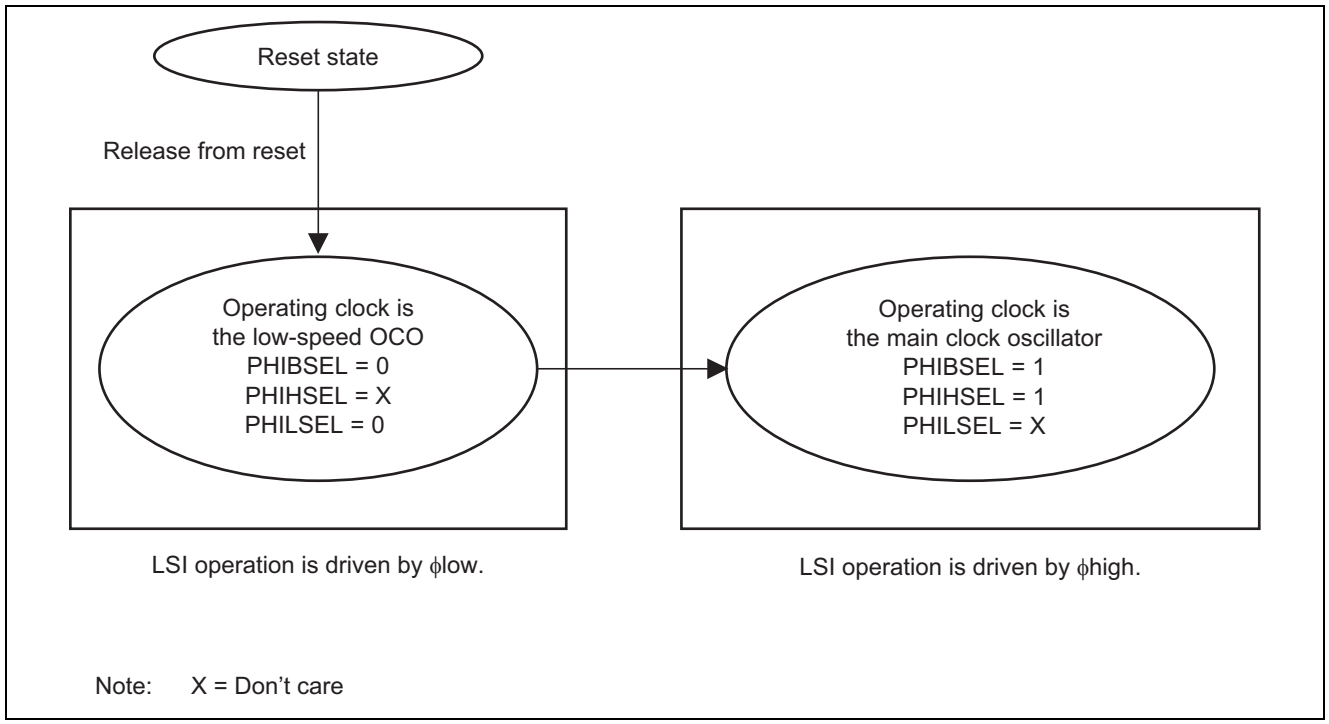


Figure 1 State Transition Diagram for the LSI System's Base Clock

2. Description of Module Used

2.1 Clock Pulse Generator

Blocks of the clock pulse generator are described below.

- The clock pulse generator is comprised of a high-speed on-chip oscillator (OCO), a 1/2 divider for the high-speed OCO, the main oscillator, a duty correction circuit, a low-speed OCO, a suboscillator, a clock selection circuit, a system clock divider, a PSC divider for peripheral modules, and a ϕs divider for the bus master and memory.
  Table 1 lists clock source symbols and their meanings used in this application note.

Table 1 Clock Source Symbols

Symbol	Description
ϕ40	High-speed OCO output
ϕhoco	High-speed OCO frequency/2
ϕloco	Low-speed OCO output
ϕosc	Main oscillator output clock (duty correction)
ϕsub	Sub-oscillator output clock
ϕhigh	High-speed clock (ϕhoco or ϕosc)
ϕlow	Low-speed clock (ϕloco or ϕsub)
ϕbase	System base clock
ϕ	System operation clock
ϕs	Bus-master operating clock

- Choice of four clock sources:
  ϕloco, ϕsub, ϕhoco and ϕosc
- Choice of two frequencies of the high-speed OCO by the user software:
  40 MHz and 32 MHz
  The signal generated by dividing the above clock by 2 can be used as a ϕbase and the above clock can be used as the clock source for timer RC, timer RD, and timer RG.
- Trimmable high-speed OCO oscillation frequencies
  Although the high-speed OCO is trimmed to 40 MHz in its initial state, it can also be trimmed to accommodate specific user operation conditions.
- Main oscillation backup function
  By detecting a ϕosc stop, it is possible to automatically switch the system clock to either ϕhoco or ϕlow.
- Clock switching interrupt function
  When the system clock is switched from ϕosc to ϕhoco or ϕloco, a CPU interrupt can be generated if enabled.

Figure 2 shows a block diagram of the clock pulse generation circuit.

The system base clock (ϕbase) is the basic clock on which the CPU and on-chip peripheral modules operate. ϕbase can be divided by a value from 1 to 128 in the system clock divider, and the divided clock is supplied as the system clock ϕ. The system clock ϕ is divided by a value from 2 to 8192 in the PSC divider, and the divided clock can be supplied to on-chip peripheral modules. The system clock ϕ is also divided by a value from 1 to 32 in the ϕs divider, and the divided clock can be supplied to the bus master and memory.

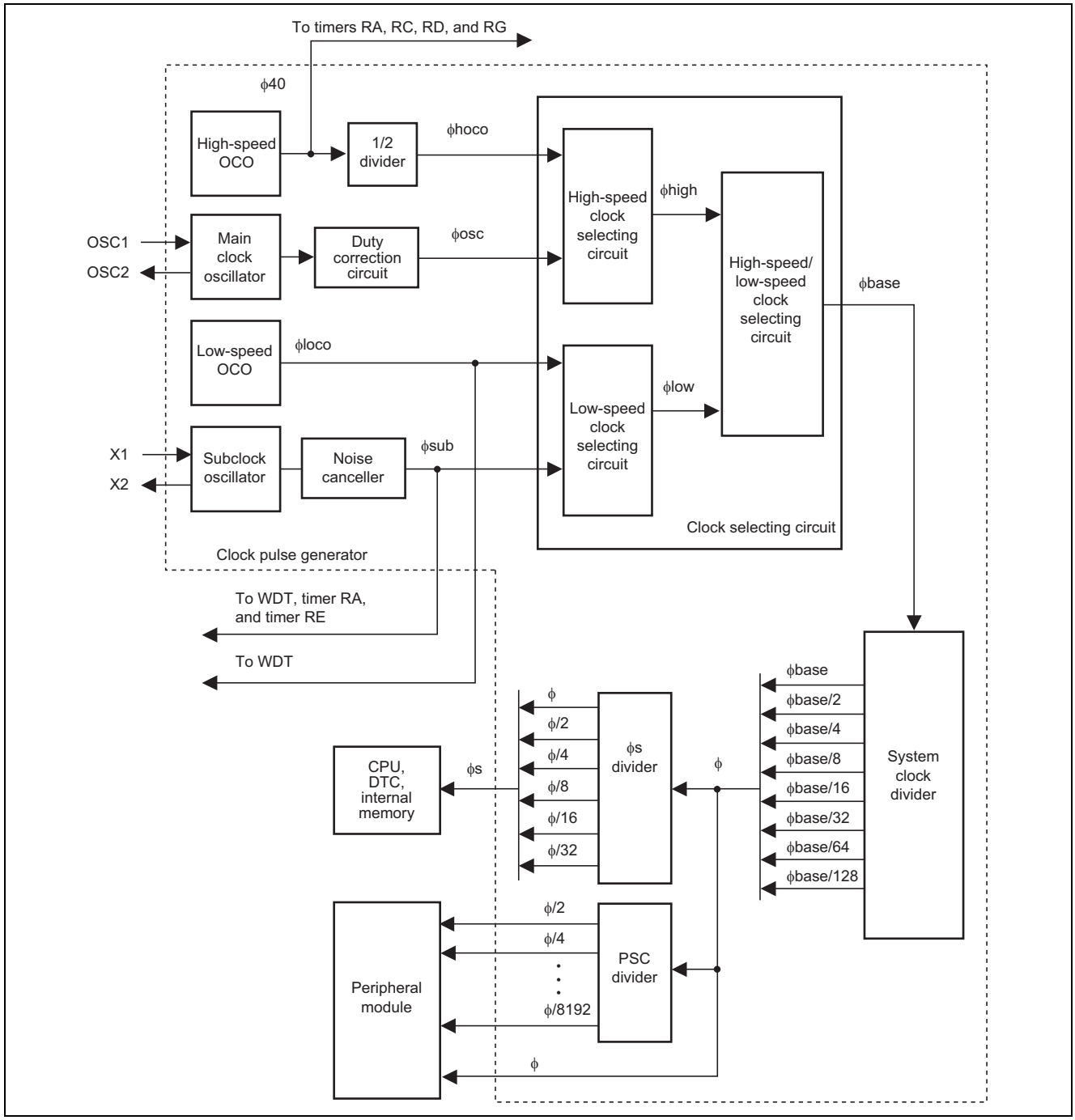


Figure 2 Block Diagram of Clock Pulse Generation Circuit

2.2 Power-Down Modes

In addition to normal active mode, this LSI can enter either of the two power-down modes after release from a reset, in which power consumption is reduced. As other measures for reduced power consumption, this LSI also has a bus-master-clock division function for the low-speed operation of bus masters, module standby function which allows the selective stopping of on-chip peripheral modules, and a PSC-divider stopping function. Further power consumption is possible by selecting the low-speed on-chip oscillator clock ϕloco, or sub-oscillator clock ϕsub as the source of the system clock ϕ to operate the LSI at a low speed.

- Active Mode
  The CPU and on-chip peripheral modules are driven by the system clock ϕ. The system clock frequency can be selected from among ϕbase to ϕbase/128, where ϕbase is the system base clock.
- Sleep Mode
  The CPU is stopped. On-chip peripheral modules are driven by the system clock ϕ.
- Standby Mode
  The CPU and all the on-chip peripheral modules are stopped. However, timer RE (TMRE) can operate when the realtime clock mode is selected. The watchdog timer (WDT) also operates when the low-speed OCO is selected as the WDT clock source.
- Bus-Master Clock Division Function
  For bus masters CPU and DTC, ROM, and RAM, the operating clock ϕs can be divided independently of the clock supplied to the peripheral modules. The bus master clock ϕs can be selected from among ϕ to ϕ/32.
- PSC Divider Stop Function
  The PSC divider can be stopped through software setting. Specifically, the peripheral modules using ϕ/2 to ϕ/8192 are stopped (register values are retained), whereas the ones using ϕ remain operating.
- Module Standby Function
  Power consumption can be reduced by halting individual on-chip peripheral modules that are not in use.

2.3 Watchdog Timer (WDT)

The watchdog timer (WDT) is an 8-bit timer that can generate an internal reset signal for this LSI if a system crash prevents the CPU from writing to the timer counter, thus allowing it to overflow. The block diagram of the watchdog timer is shown in figure 3.

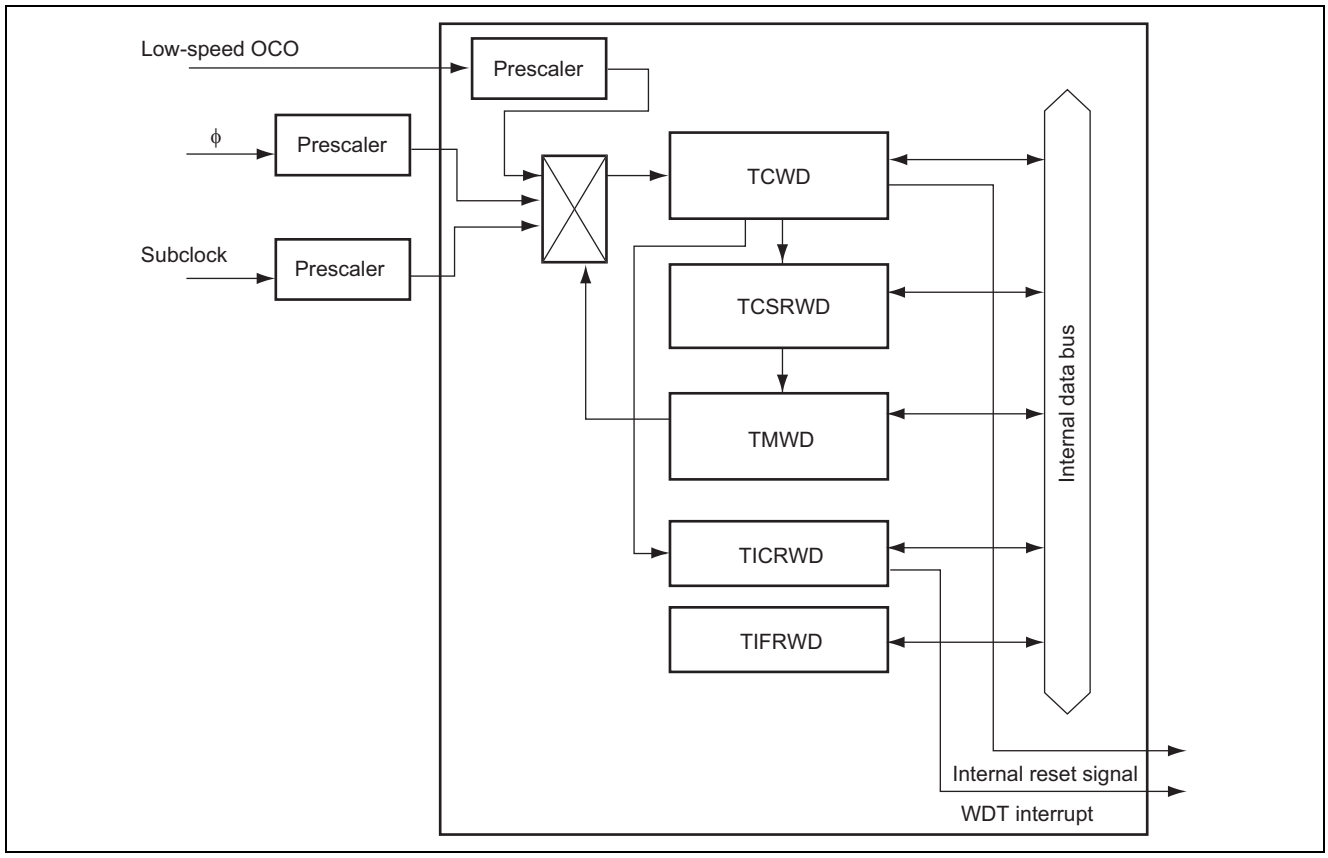


Figure 3 Block Diagram of Watchdog Timer

- Selectable from fifteen clock sources
  Eight clocks generated by dividing ϕ: ϕ/64, ϕ/128, ϕ/256, ϕ/512, ϕ/1024, ϕ/2048, ϕ/4096, and ϕ/8192
  Five clocks generated by dividing low-speed OCO clock: ϕloco/8, ϕloco/32, ϕloco/128, ϕloco/512, and ϕloco/1024
  Two clocks generated by dividing subclock: ϕsub/4 and ϕsub/256
  When the low-speed OCO clock or subclock is selected, the WDT operates as the watchdog timer in any operating mode.
- Reset signal generated on counter overflow
  An overflow period of 1 to 256 times the selected clock can be set.
- The watchdog timer is enabled in the initial state.
  The watchdog timer starts operating after a reset is released.
- Periodic timer function
  The timer counter can also be used as a periodic timer. Interrupts can be generated with a specific count value.

3. Principle of Operation

Figure 4 shows the principle of operation in this sample task. Initial settings to select the external oscillator and release all modules from standby mode are made by means of hardware and software processing as shown in figure 4.

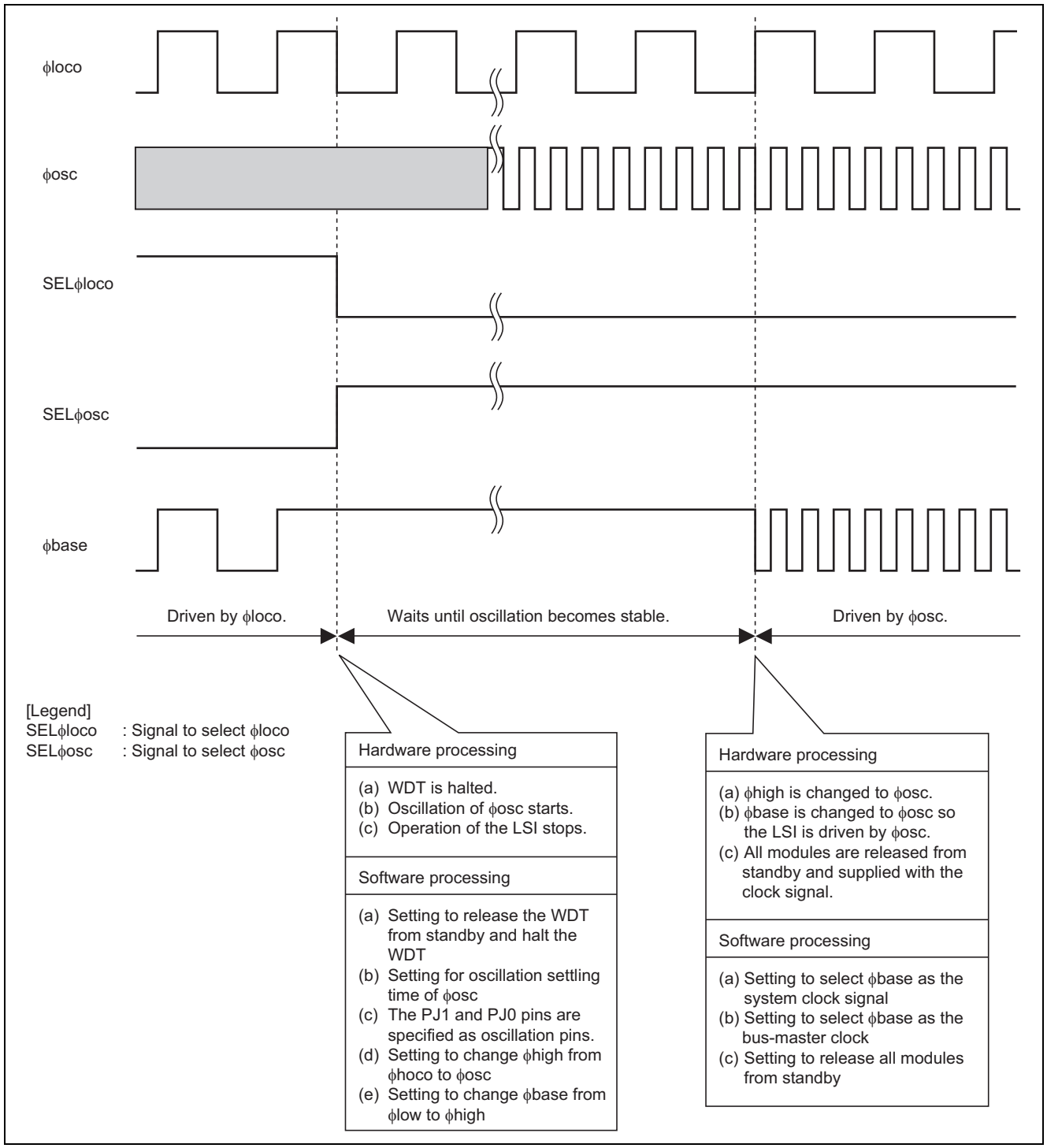


Figure 4 Principle of Operation in This Sample Task

4. Description of Software

4.1 Descriptions of Functions

The functions are listed and described in table 2.

Table 2 Descriptions of Functions

Function Name	Label Name	Description
Main routine	main	Calls other functions.
System initialization routine	h8s_sysinit	Makes settings for module standby, system clock and bus-master operating clock, and halts the WDT.

4.2 Description of Argument

No arguments are used in this sample task.

4.3 Description of Internal Registers

Table 3 gives descriptions of how internal registers are used in this sample task.

Table 3 Description of Internal Registers

Register Name	Symbol	Description	Address	Setting
PMRJ	PMRJ[1:0]	The OSC1 and OSC2 functions are selected for pins PJ0/OSC1 and PJ1/OSC2.	H'FF000C	B'11
SYSCCR	PHIHSEL	φhigh clock source is set to φosc.	H'FF06D0	1
LPCR1	PSCSTP	PSC divider is operating.	H'FF06D1	0
	PHIBSEL	φbase clock source is set to φhigh.		1
LPCR2	PHI[2:0]	System clock φ is set to φbase.	H'FF06D2	B'000
LPCR3	PHIS[2:0]	Bus-master operating clock φs is set to φ.	H'FF06D3	B'000
OSCCSR		φosc oscillation settling time is set.	H'FF06D5	H'0E
TMWD		Clock input to the WDT is prohibited.	H'FFFF99	H'F7
TCSRWD		Writing to the TMWD register is enabled.	H'FFFF9A	H'A3
MSTCR1	MSTWDT	Watchdog timer module standby is released.	H'FFFFDC	0
	MSTAD1	A/D converter unit 1 module standby is released.		0
	MSTAD2*[1]	A/D converter unit 2 module standby is released		0
	MSTDA	D/A converter module standby is released.		0
	MSTDTC	DTC module standby is released.		0
MSTCR2	MSTSCI3_1	SCI3 channel 1 module standby is released.	H'FFFFDD	0
	MSTSCI3_2	SCI3 channel 2 module standby is released.		0
	MSTSCI3_3	SCI3 channel 3 module standby is released.		0
	MSTICSU	IIC2/SSU module standby is released.		0
MSTCR3	MSTTMRA	Timer RA module standby is released.	H'FFFFDE	0
	MSTTMRB	Timer RB module standby is released.		0
	MSTTMRC*[2]	Timer RC module standby is released.		0
	MSTTMRD1	Timer RD unit 0 module standby is released.		0
	MSTTMRD2*[3]	Timer RD unit 1 module standby is released.		0
	MSTTMRG	Timer RG module standby is released.		0
	MSTTMRE	Timer RE module standby is released.		0

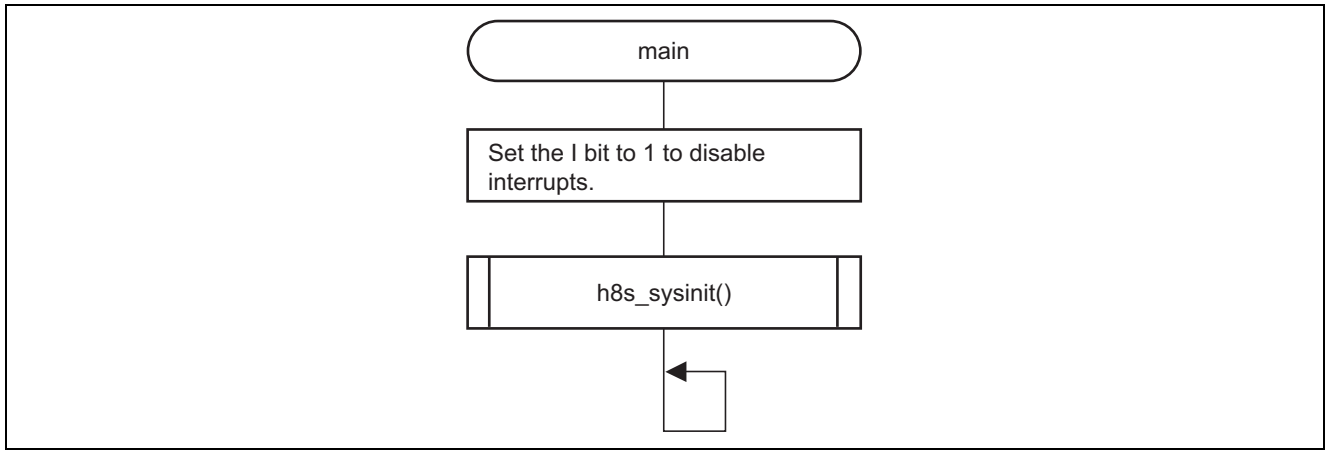
Notes: 1. A/D converter unit 2 is not available on the H8S/20103 and H8S/20203 Groups; this bit is reserved on these devices. For a write-access, write 1 to this bit.
2. Timer RC is not available on the H8S/20203 and H8S/20223 Groups; this bit is reserved on these devices. For a write-access, write 1 to this bit.
3. Timer RD unit 1 is not available on the H8S/20103 Group; this bit is reserved on the device. For a write-access, write 1 to this bit.

4.4 RAM Usage

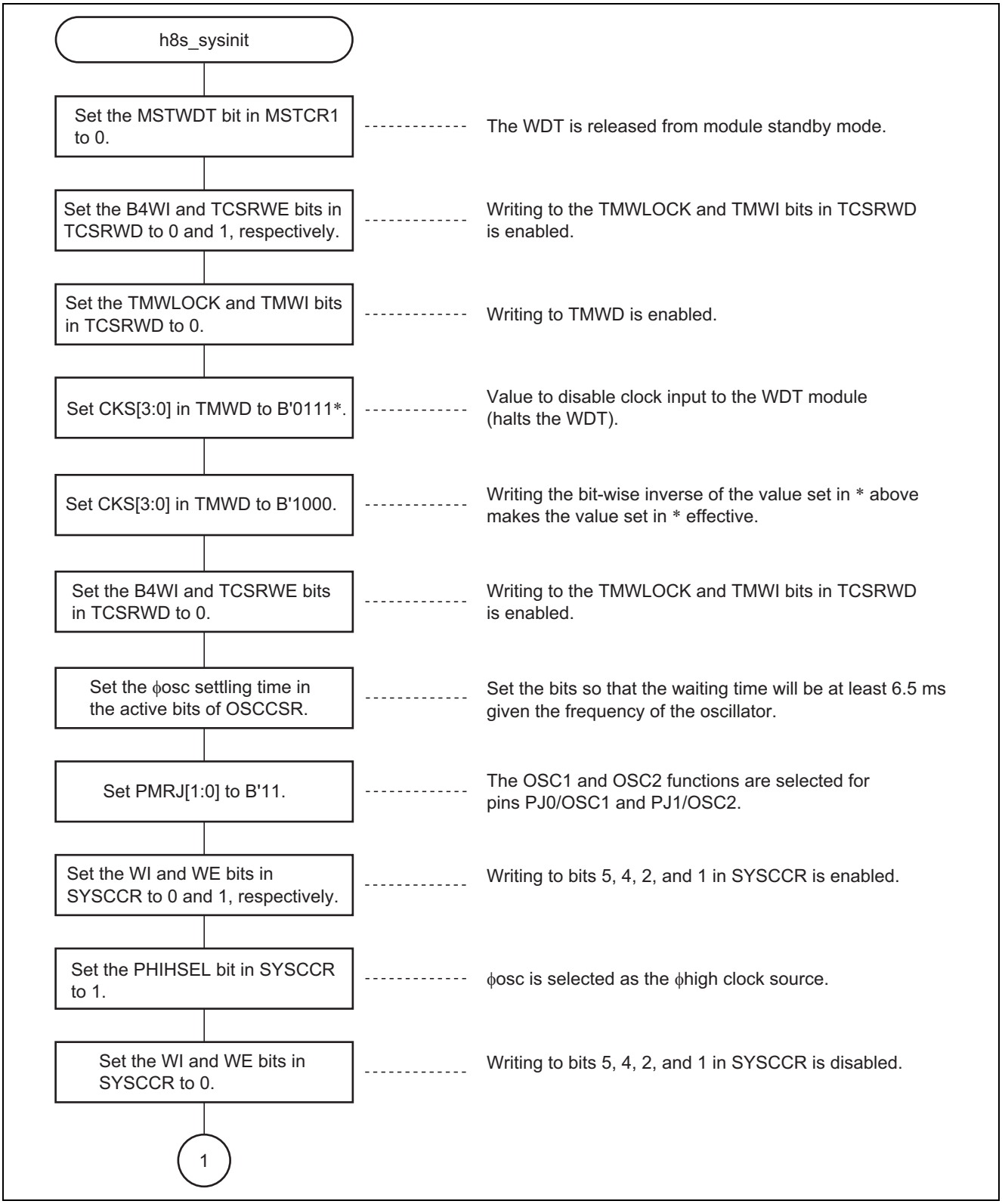
No RAM is used in this sample task.

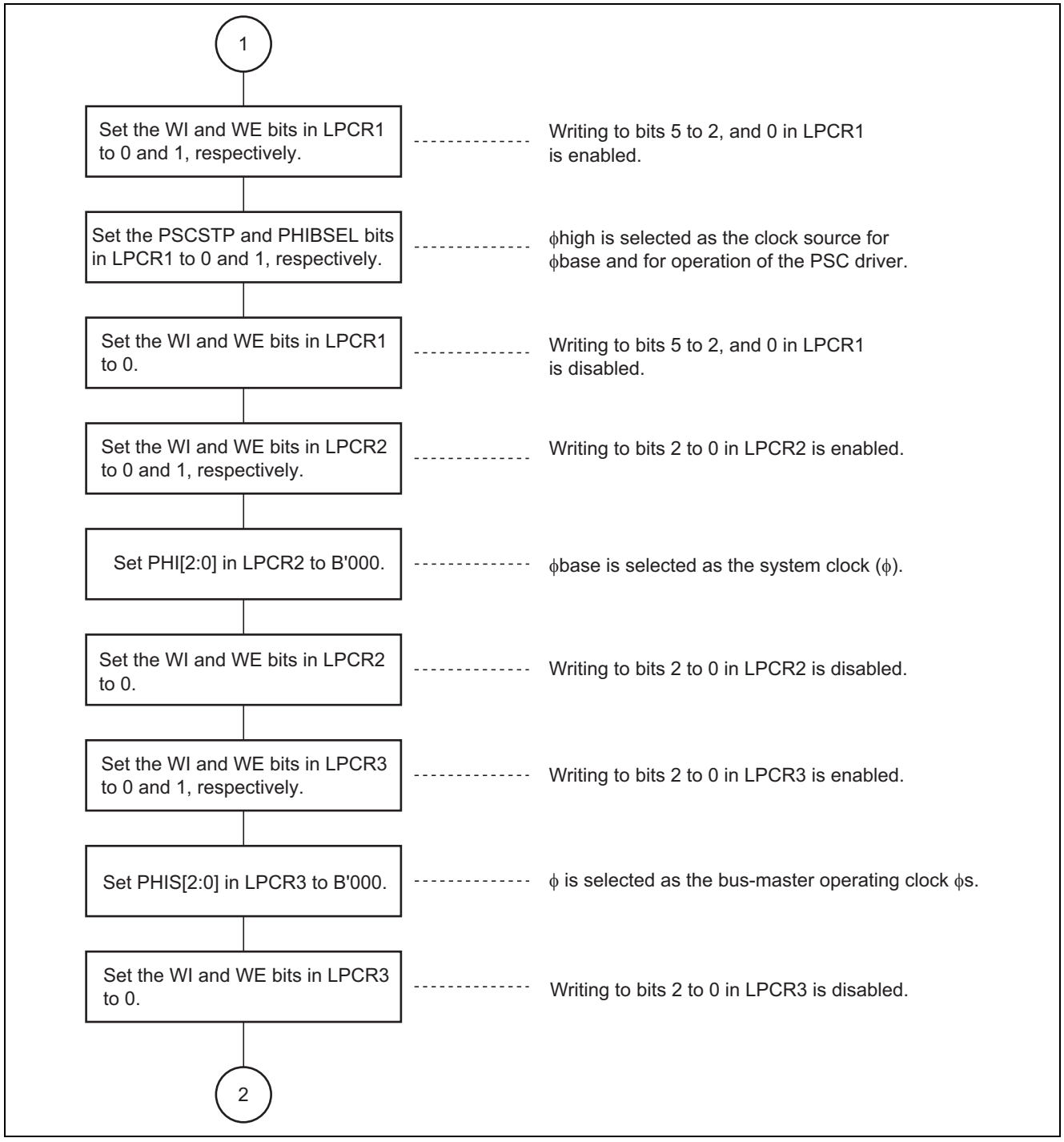
5. Flowcharts

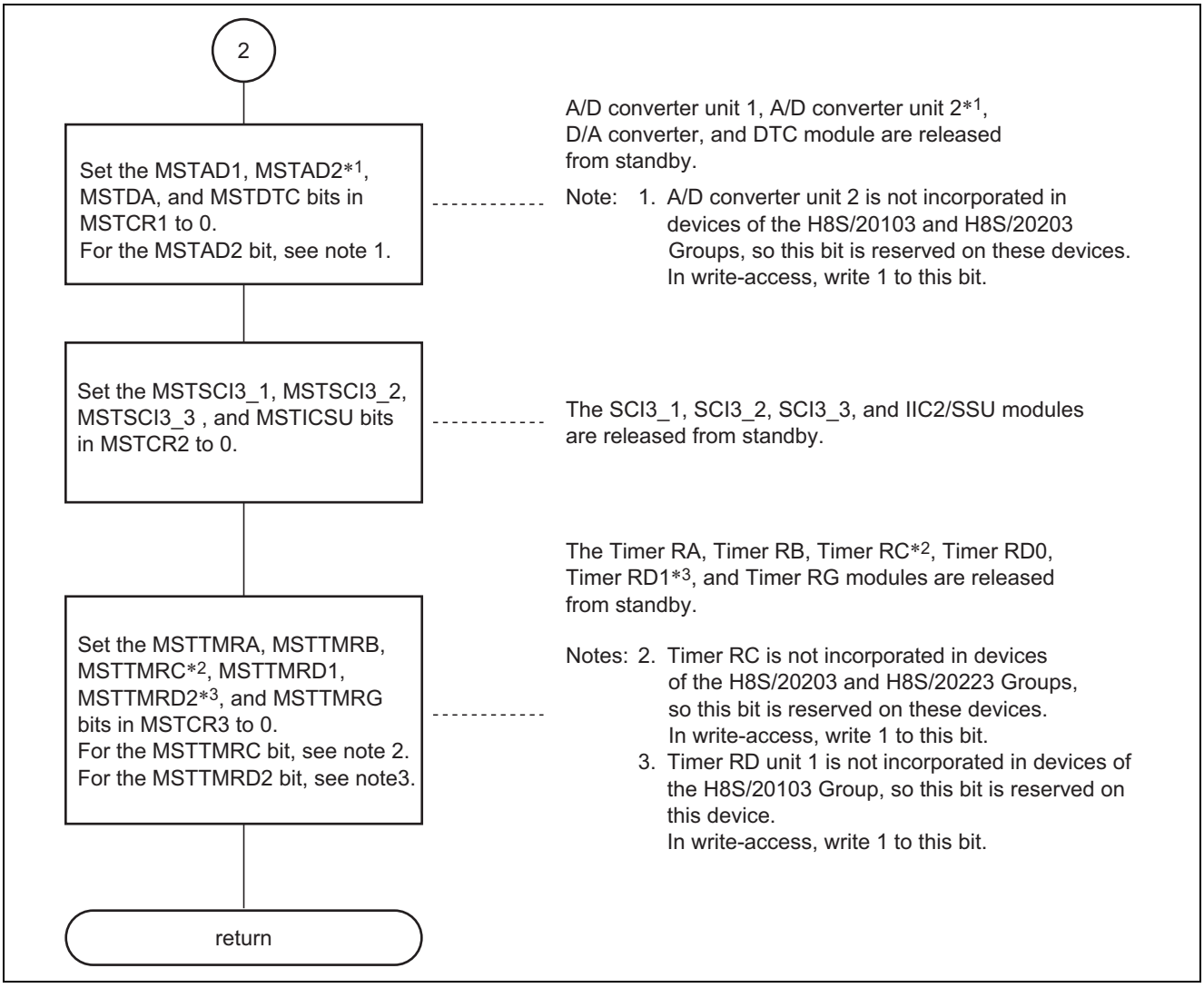
5.1 Main Routine



5.2 System Initialization Routine




1
Set the WI and WE bits in LPCR1 to 0 and 1, respectively.
Writing to bits 5 to 2, and 0 in LPCR1 is enabled.
Set the PSCSTP and PHIBSEL bits in LPCR1 to 0 and 1, respectively.
ϕhigh is selected as the clock source for ϕbase and for operation of the PSC driver.
Set the WI and WE bits in LPCR1 to 0.
Writing to bits 5 to 2, and 0 in LPCR1 is disabled.
Set the WI and WE bits in LPCR2 to 0 and 1, respectively.
Writing to bits 2 to 0 in LPCR2 is enabled.
Set PHI[2:0] in LPCR2 to B'000.
ϕbase is selected as the system clock (ϕ).
Set the WI and WE bits in LPCR2 to 0.
Writing to bits 2 to 0 in LPCR2 is disabled.
Set the WI and WE bits in LPCR3 to 0 and 1, respectively.
Writing to bits 2 to 0 in LPCR3 is enabled.
Set PHIS[2:0] in LPCR3 to B'000.
ϕ is selected as the bus-master operating clock ϕs.
Set the WI and WE bits in LPCR3 to 0.
Writing to bits 2 to 0 in LPCR3 is disabled.
2


2
Set the MSTAD1, MSTAD2*1, MSTDA, and MSTDTC bits in MSTCR1 to 0.
For the MSTAD2 bit, see note 1.
A/D converter unit 1, A/D converter unit 2*1, D/A converter, and DTC module are released from standby.
Note: 1. A/D converter unit 2 is not incorporated in devices of the H8S/20103 and H8S/20203 Groups, so this bit is reserved on these devices. In write-access, write 1 to this bit.
Set the MSTSCI3_1, MSTSCI3_2, MSTSCI3_3 , and MSTICSU bits in MSTCR2 to 0.
The SCI3_1, SCI3_2, SCI3_3, and IIC2/SSU modules are released from standby.
Set the MSTTMRA, MSTTMRB, MSTTMRC*2, MSTTMRD1, MSTTMRD2*3, and MSTTMRG bits in MSTCR3 to 0.
For the MSTTMRC bit, see note 2.
For the MSTTMRD2 bit, see note3.
The Timer RA, Timer RB, Timer RC*2, Timer RD0, Timer RD1*3, and Timer RG modules are released from standby.
Notes: 2. Timer RC is not incorporated in devices of the H8S/20203 and H8S/20223 Groups, so this bit is reserved on these devices. In write-access, write 1 to this bit.
3. Timer RD unit 1 is not incorporated in devices of the H8S/20103 Group, so this bit is reserved on this device. In write-access, write 1 to this bit.
return

6. Program Listing

```
/************************************************************************************/
/* H8S/2000 Tiny Series -H8S/20203-                                                 */
/* Application Note                                                                 */
/*                                                                                  */
/* System initialize                                                                */
/*                                                                                  */
/* Function: System initialize                                                      */
/* (Watch Dog Timer) active -> stop                                                 */
/* (System base clock) Phi_loco -> Phi_osc                                          */
/* (Module Standby) standby -> active                                               */
/*                                                                                  */
/* External Clock: 20MHz                                                            */
/* Internal Clock: 20MHz                                                            */
/************************************************************************************/
#include <machine.h>
#include "iodefine.h"

/*******************************************************/
/* Declaration of function prototype                   */
/*******************************************************/
void main(void);
void h8s_sysinit(void);

/*******************************************************/
/* Name        : main                                  */
/* Parameters  : None                                  */
/* Returns     : None                                  */
/* Description : User main                             */
/*******************************************************/
void main(void)
{
    set_ccr(0x80); /* set CCR-Ibit */

    h8s_sysinit(); /* initialize system */

    while(1);

}
```

```
/*********************************************************/
/* Name        : h8s_sysinit                             */
/* Parameters  : None                                    */
/* Returns     : None                                    */
/* Description : initialize H8S/20203                    */
/*********************************************************/
void h8s_sysinit(void)
{
    MSTCR1.BIT.MSTWDT = 0;                                  /* WDT module standby off */

/* stop WDT */
    WDT.TCSRWD.BYTE = 0x97;                                 /* write enable TMWLOCK, TMWI */
    WDT.TCSRWD.BYTE = 0xA3;                                 /* write enable TMWD */
    WDT.TMWD.BYTE = 0xF7;                                   /* Not select clock source */
    WDT.TMWD.BYTE = 0xF8;                                   /* write bit inversion */
    WDT.TCSRWD.BYTE = 0x87;                                 /* write disable TMWLOCK, TMWI */

    CPG.OSCCSR.BYTE = 0x0E;                                 /* wait over 6.5ms, Phi_osc=20MHz */
    PMRJ.BYTE = 0x03;                                       /* select OSC1,OSC2 */

    CPG.SYSCCR.BYTE = (CPG.SYSCCR.BYTE & 0x7F)| 0x40;       /* WI=0, WE=1 */
    CPG.SYSCCR.BYTE = 0x60;                                 /* high=Phi_osc, Phi_low=Phi_loco */
    CPG.SYSCCR.BYTE = CPG.SYSCCR.BYTE & 0x3F;               /* WI=0, WE=0 */

    CPG.LPCR1.BYTE = (CPG.LPCR1.BYTE & 0x7F) | 0x40;        /* WI=0, WE=1 */
    CPG.LPCR1.BYTE = 0x41;                                  /* PSC on, Phi_base=Phi_high */
    CPG.LPCR1.BYTE = CPG.LPCR1.BYTE & 0x3F;                 /* WI=0, WE=0 */

    CPG.LPCR2.BYTE = (CPG.LPCR2.BYTE & 0x7F) | 0x40;        /* WI=0, WE=1 */
    CPG.LPCR2.BYTE = 0x40;                                  /* select system clock=Phi_base */
    CPG.LPCR2.BYTE = CPG.LPCR2.BYTE & 0x3F;                 /* WI=0, WE=0 */

    CPG.LPCR3.BYTE = (CPG.LPCR3.BYTE & 0x7F) | 0x40;        /* WI=0, WE=1 */
    CPG.LPCR3.BYTE = 0x40;                                  /* select clock of bus master=Phi_base */
    CPG.LPCR3.BYTE = CPG.LPCR3.BYTE & 0x3F;                 /* WI=0, WE=0 */

    /* all module standby off */
    MSTCR1.BYTE = 0x53;
    MSTCR2.BYTE = 0x1B;
    MSTCR3.BYTE = 0x22;
}
```

6.1 Designation of Link Addresses

Section Name	Address
PResetPRG, PIntPRG	H'000400
P, C$DSEC, C$BSEC, D	H'000800
B, R	H'FFDF80
S	H'FFFD80

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