R32C/100 Series

How to Use Intelligent I/O Interrupt

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1. Abstract

The intelligent I/O interrupt has multiple interrupt request sources, such as a time measurement interrupt and a waveform generation interrupt. It bundles several interrupt requests sources and use them as one intelligent I/O interrupt. This document describes how to use the intelligent I/O interrupt.

2. Introduction

The application example described in this document applies to the following microcomputers (MCUs):

MCUs: R32C/116 Group, R32C/117 Group, R32C/118 Group, R32C/120 Group, and R32C/121 Group

This application note can be used with other R32C/100 Series MCUs which have the same special function registers (SFRs) as the above groups. Check the manuals for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Intelligent I/O Interrupt

3.1 Explanation

Figure 3.1 shows the Intelligent I/O Interrupt Block Diagram (i = 0 to 11). Figure 3.2 and Figure 3.3 show Bit Symbols for the Intelligent I/O Interrupt Request Register i (i = 0 to 11) and Bit Symbols for the Intelligent I/O Interrupt Enable Register i, respectively.

To use the intelligent I/O interrupt, the IRLT bit in the IIOiIE register should be set to 1 (interrupt requests used for interrupt) (i = 0 to 11).

The intelligent I/O interrupt has multiple request sources. When an interrupt request is generated with an intelligent I/O function, the corresponding bit in the IIOiIR register becomes 1 (interrupt requested). If the corresponding bit in the IIOiIC register is set to 1 (interrupt enabled), the IR bit in the corresponding IIOilC register changes to 1 (interrupt requested).

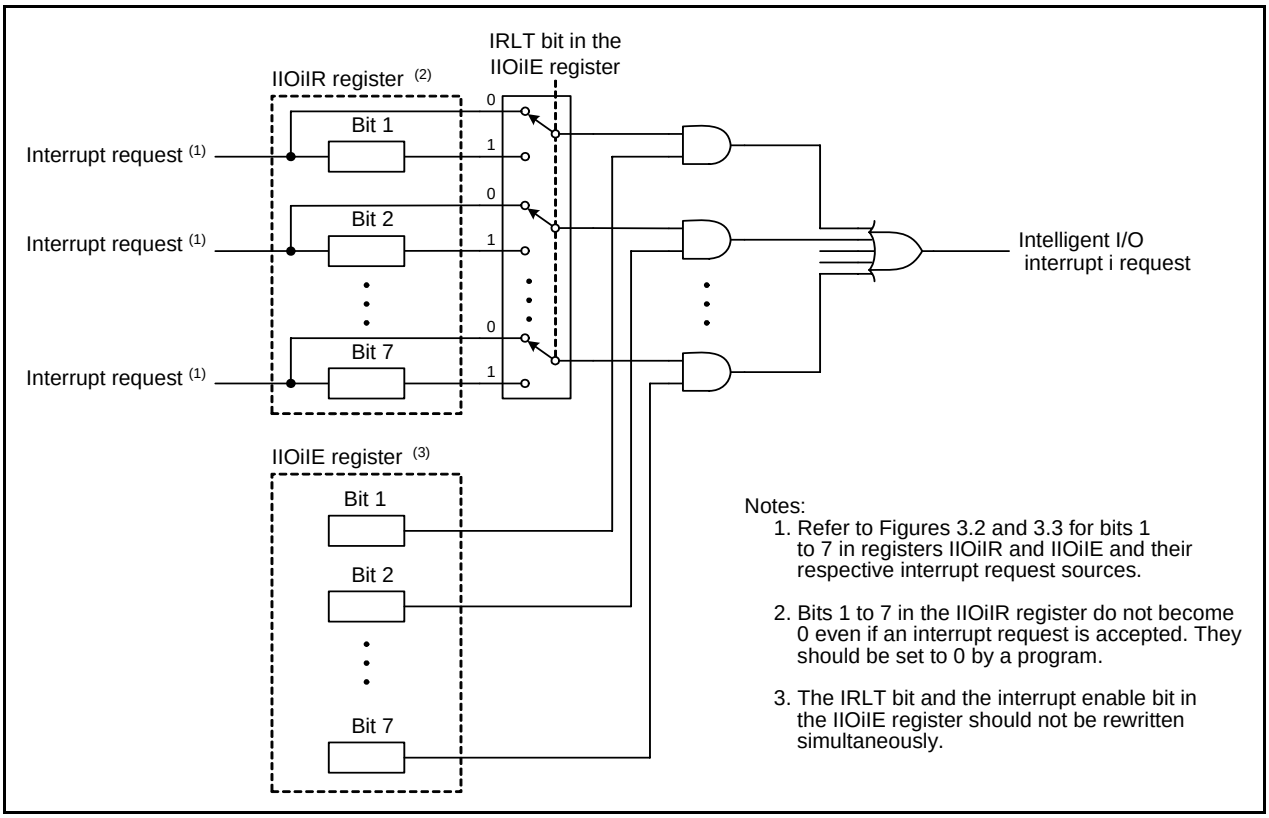

Figure 3.1 Intelligent I/O Interrupt Block Diagram (i = 0 to 11)

Symbol	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IIO0IR	00A0h	—	—	—	—	—	TM13R/PO13R	TM02R/PO02R	—
IIO1IR	00A1h	—	—	—	—	—	TM14R/PO14R	TM00R/PO00R	—
IIO2IR	00A2h	—	—	—	—	—	TM12R/PO12R	—	—
IIO3IR	00A3h	—	—	—	—	PO27R	TM10R/PO10R	TM03R/PO03R	—
IIO4IR	00A4h	—	—	—	BT1R	—	TM17R/PO17R	TM04R/PO04R	—
IIO5IR	00A5h	—	—	—	SIO2RR	—	PO21R	TM05R/PO05R	—
IIO6IR	00A6h	—	—	—	SIO2TR	—	PO20R	TM06R/PO06R	—
IIO7IR	00A7h	IE0R	—	—	BT0R	—	PO22R	TM07R/PO07R	—
IIO8IR	00A8h	IE1R	IE2R	—	BT2R	—	PO23R	TM11R/PO11R	—
IIO9IR	00A9h	—	INT6R	—	—	—	PO24R	TM15R/PO15R	—
IIO10IR	00AAh	—	INT7R	—	—	—	PO25R	TM16R/PO16R	—
IIO11IR	00ABh	—	INT8R	—	—	—	PO26R	TM01R/PO01R	—

BTxR : Intelligent I/O group x base timer interrupt request (x = 0 to 2)
TMxyR : Intelligent I/O group x time measurement channel y interrupt request (x = 0, 1; y = 0 to 7)
POxyR : Intelligent I/O group x waveform generation channel y interrupt request (x = 0 to 2; y = 0 to 7)
IEzR : Intelligent I/O group 2 IEBus interrupt request (z = 0 to 2)
SIO2RR : Intelligent I/O group 2 receive interrupt request
SIO2TR : Intelligent I/O group 2 transmit interrupt request
INTmR : INTm interrupt request (m = 6 to 8)

Figure 3.2 Bit Symbols for the Intelligent I/O Interrupt Request Register i (i = 0 to 11)

Symbol	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IIO0IE	00B0h	—	—	—	—	—	TM13E/PO13E	TM02E/PO02E	IRLT
IIO1IE	00B1h	—	—	—	—	—	TM14E/PO14E	TM00E/PO00E	IRLT
IIO2IE	00B2h	—	—	—	—	—	TM12E/PO12E	—	IRLT
IIO3IE	00B3h	—	—	—	—	PO27E	TM10E/PO10E	TM03E/PO03E	IRLT
IIO4IE	00B4h	—	—	—	BT1E	—	TM17E/PO17E	TM04E/PO04E	IRLT
IIO5IE	00B5h	—	—	—	SIO2RE	—	PO21E	TM05E/PO05E	IRLT
IIO6IE	00B6h	—	—	—	SIO2TE	—	PO20E	TM06E/PO06E	IRLT
IIO7IE	00B7h	IE0E	—	—	BT0E	—	PO22E	TM07E/PO07E	IRLT
IIO8IE	00B8h	IE1E	IE2E	—	BT2E	—	PO23E	TM11E/PO11E	IRLT
IIO9IE	00B9h	—	INT6E	—	—	—	PO24E	TM15E/PO15E	IRLT
IIO10IE	00BAh	—	INT7E	—	—	—	PO25E	TM16E/PO16E	IRLT
IIO11IE	00BBh	—	INT8E	—	—	—	PO26E	TM01E/PO01E	IRLT

BTxE : Intelligent I/O group x base timer interrupt enabled (x = 0 to 2)
TMxyE : Intelligent I/O group x time measurement channel y interrupt enabled (x = 0, 1; y = 0 to 7)
POxyE : Intelligent I/O group x waveform generation channel y interrupt enabled (x = 0 to 2; y = 0 to 7)
IEzE : Intelligent I/O group 2 IEBus interrupt enabled (z = 0 to 2)
SIO2RE : Intelligent I/O group 2 receive interrupt enabled
SIO2TE : Intelligent I/O group 2 transmit interrupt enabled
INTmE : INTm interrupt enabled (m = 6 to 8)

Figure 3.3 Bit Symbols for the Intelligent I/O Interrupt Enable Register i

3.2 Notes on the Intelligent I/O Interrupt

The IR bits in the IIOiIC register are set to 0 automatically if an interrupt is accepted (i = 0 to 11). However, bits in the IIOiIR register do not become 0 even if an interrupt is accepted. They should be set to 0 by either the AND or BCLR instruction within an interrupt handler.

Note that every generated interrupt request is ignored until these bits are set to 0.

4. Usage Example

4.1 Peripheral Function

This section describes an example of how to use the intelligent I/O interrupt using waveform generation.
Table 4.1 lists the Group, Channel Number, and Function Assignment.

Table 4.1 Group, Channel Number, and Function Assignment

Group	Channel	Function
Group 0	Channel 0	Waveform generation (single-phase waveform output mode)
Group 1	Channel 4	Waveform generation (single-phase waveform output mode)

To use both the group 0 waveform generation function channel 0 (PO00) interrupt and the group 1 waveform generation function channel 4 (PO14) interrupt, set both bits PO00E and PO14E in the IIO1IE register to 1.
When the PO00 interrupt request is generated, the PO00R bit in the IIO1IR register becomes 1 and when the PO14R interrupt request is generated, the PO14R bit in the IIO1IR register becomes 1. When either the PO00R bit or the PO14R bit, or both bits become 1, the IR bit in the II01IC register becomes 1. When reading the IIO1IR register within an interrupt handler, the MCU determines the generated interrupt sources and executes the interrupt handler.

Figure 4.1 shows an Operation Example of Intelligent I/O Interrupt 1.

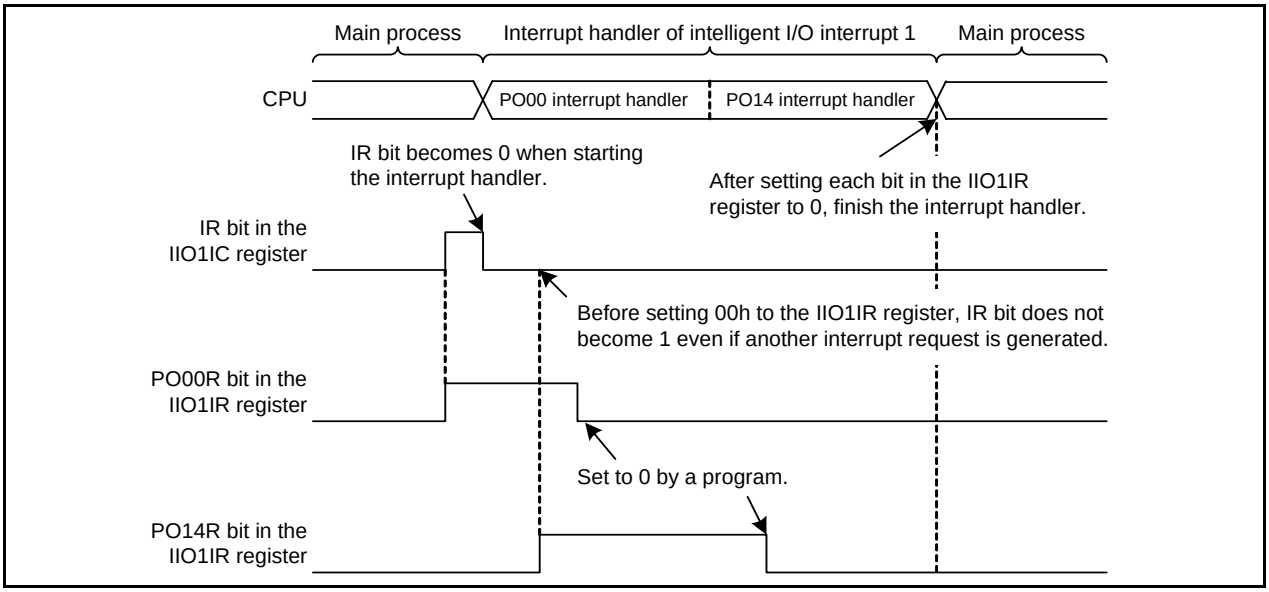

Figure 4.1 Operation Example of Intelligent I/O Interrupt 1

4.2 Settings

This section shows the setting procedure and setting values in registers IIO1IR, IIO1IE, and IIO1IC to execute the example in 4. “Usage Example”. Refer to the hardware user’s manuals for details of each register.

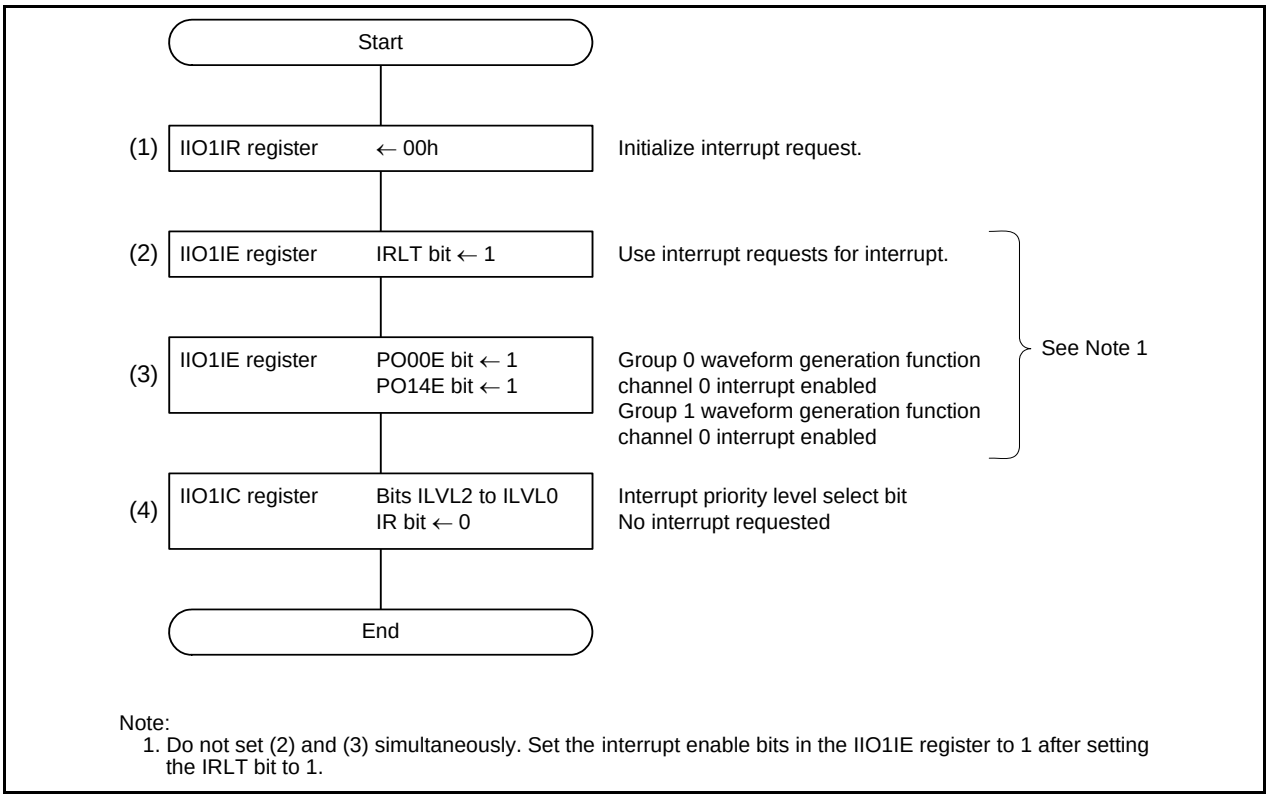

Figure 4.2 Register Setting Procedure of Intelligent I/O Interrupt 1

4.3 Program Flowchart

Figure 4.3 and Figure 4.4 show the main Function Flowchart and the Function Flowchart of Intelligent I/O Interrupt 1, respectively.

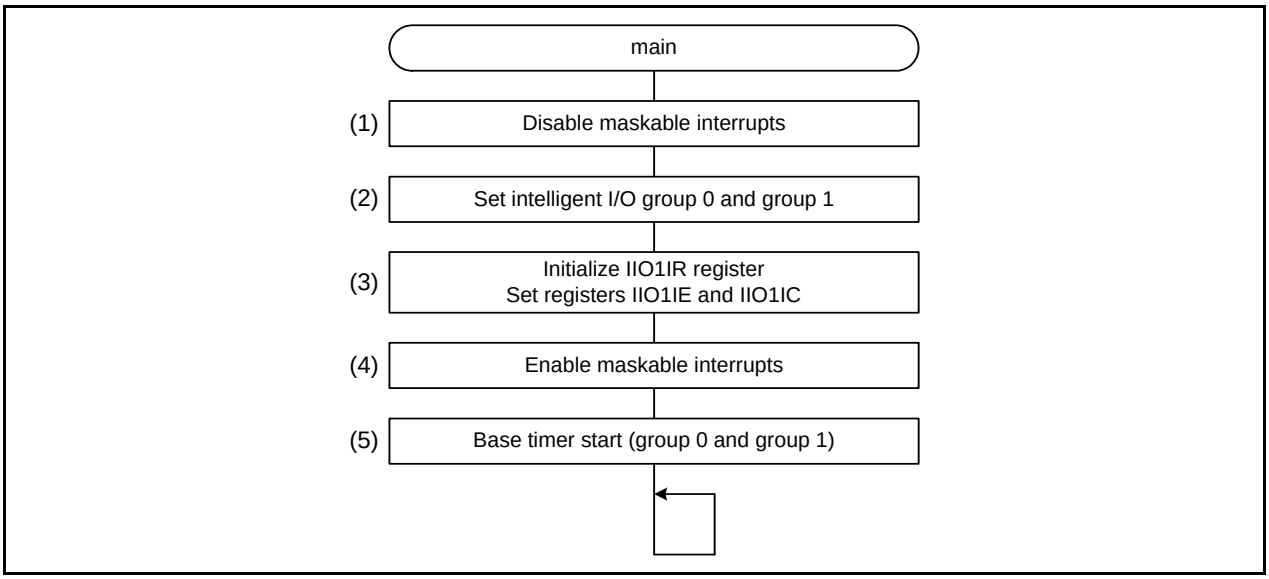

Figure 4.3 main Function Flowchart

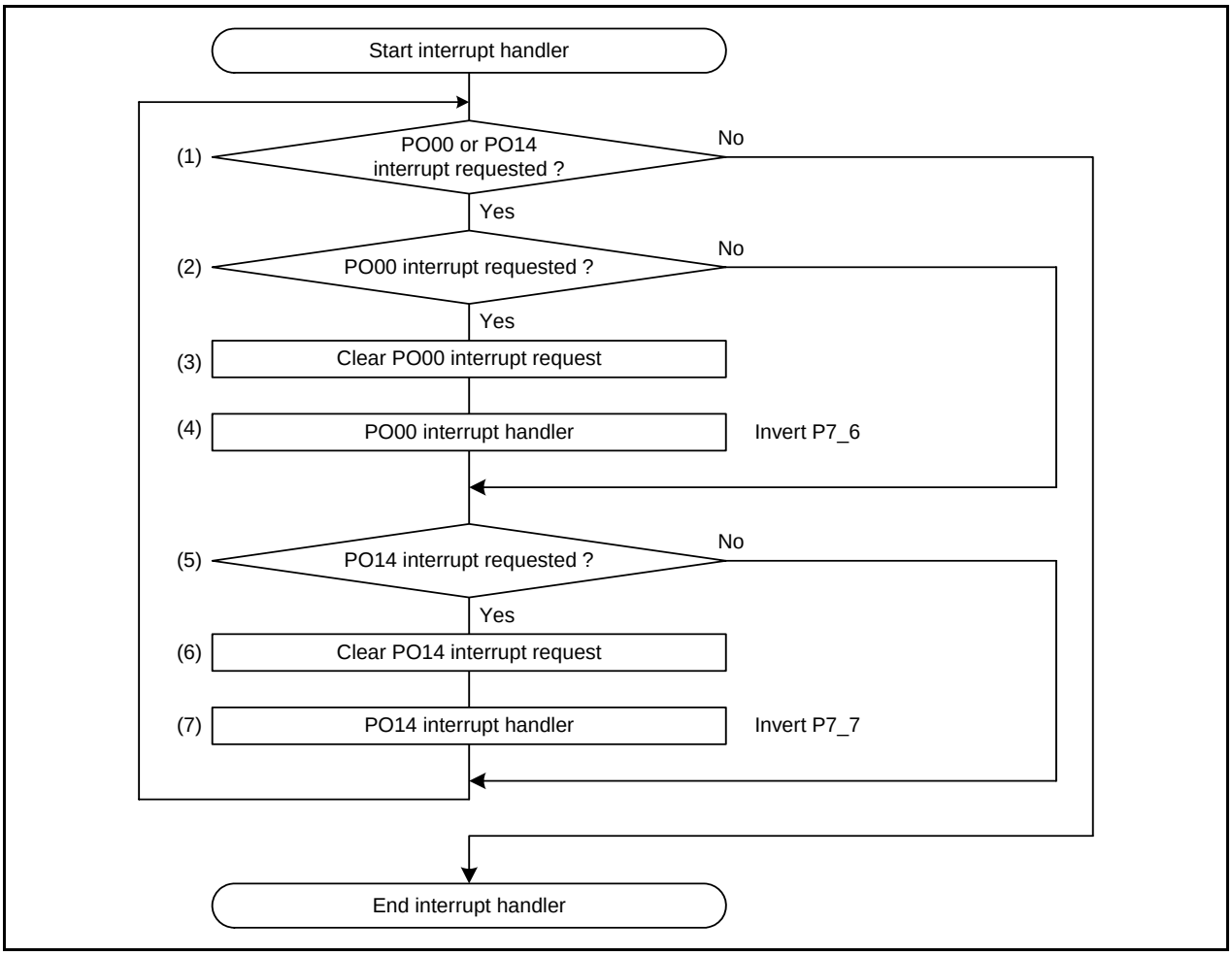

Figure 4.4 Function Flowchart of Intelligent I/O Interrupt 1

5. Sample Program

A sample program can be downloaded from the Renesas Electronics website.

6. Reference Documents

User's Manuals
R32C/116 Group User's Manual: Hardware Rev.1.00
R32C/117 Group User's Manual: Hardware Rev.1.00
R32C/118 Group User's Manual: Hardware Rev.1.00
R32C/120 Group User's Manual: Hardware Rev.1.10
R32C/121 Group User's Manual: Hardware Rev.1.10
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
R32C/100 Series C Compiler Package V.1.02 C Compiler User's Manual Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

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REVISION HISTORY	R32C/100 Series How to Use Intelligent I/O Interrupt

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		Page	Summary
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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
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Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
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Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
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Renesas Electronics Korea Co., Ltd.
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Tel: +82-2-558-3737, Fax: +82-2-558-5141

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