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Notice

H8/300L

Hardware Interface Technique for Peripherals (HWperh)

Introduction

This application note aims to describe the critical areas to observe while working with the peripherals of the H8/38024F microcomputer.

The key peripherals focused in this application note are catered mainly for SCI and LCD functions found in the microcomputer.

Target Device

H8/300L Super Low Power series – H8/38024F

Contents

1. SCI Interface 3
1.1 Asynchronous Mode 3
1.2 Synchronous Mode 4
1.3 Clock 5
1.3.1 Asynchronous Mode 5
1.3.2 Synchronous Mode 5
1.4 Interrupts 6

2. LCD Interface 6
2.1 What is frame frequency? 7
2.2 What is drive waveform? 7
2.3 How to boost the LCD Drive Power? 8
2.4 How to operate LCD controller/driver in Power Down Modes 8
2.5 Relationships between LCD RAM and Duty Cycle 9
2.6 Electrical Characteristic 11
2.6.1 Mask or Z-TAT version 11
2.6.2 F-ZTAT version 11

Reference 12

Revision Record 13

1. SCI Interface

In H8/38024F microcomputer, there is only one serial communication interface, SCI3. It is capable of carrying out either in asynchronous and synchronous mode. It supports full-duplex communication; has an on-chip baud rate generator which allows any desired bit rate to be selected; has a choice of an internal or external clock as the transmit/receive clock source; has six interrupts

It also supports multiprocessor communication function that enables serial data to be transferred among processors.

In this application note, it does not go to the extent to cover the introduction of the various SCI registers and on how to configure as well as access these registers. Instead it would focus on informing the various concerns or consideration when working on the SCI3 such as observing the timing aspect, etc.

1.1 Asynchronous Mode

For asynchronous mode, serial data is transferred with synchronization provided character by character. Serial data can be exchanged with standard asynchronous communication LSI receiver/transmitter and such as UART & ACIA. There is a choice of 16 transfer formats.

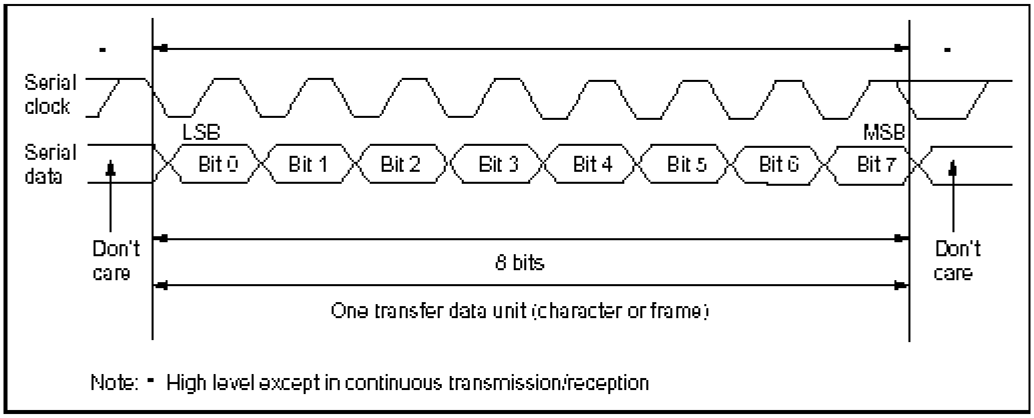
Data Length	7, 8, 5 bits
Stop bit Length	1 or 2 bits
Parity	Even, Odd, or None
Multiprocessor Bit	1 or 0
Receive Error Detection	Parity, Overrun, and Framing Errors
Break Detection	Break detected by reading the RXD_{32} pin level directly when a framing error occurs.

1.2 Synchronous Mode

For synchronous mode, serial data is synchronized with a clock, and it can be exchanged with another LSI that has a synchronous communication function. This mode is suitable for high-speed serial communication.

Data Length	8 bits
Receiver Error Detection	Overrun Errors

In synchronous communication, data on the communication line is output from one falling edge of the serial clock until the next falling edge. Data confirmation is guaranteed at the rising edge of the serial clock. Refer to the Figure below.



One transferred data begins with LSB and ends with the MSB. After output of the MSB, the communication line retains the MSB state. When receiving the date in synchronous mode, SCI3 latches receive data at the rising edge of the serial clock. The data transfer format uses a fixed 8-bit data length and parity and microprocessor bits cannot be added.

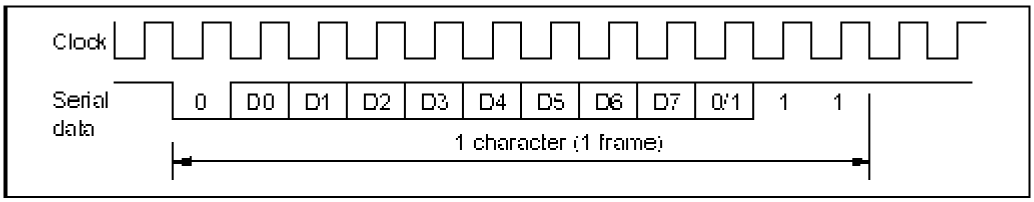
1.3 Clock

1.3.1 Asynchronous Mode

Either an internal clock generated by the baud rate generator or an external clock input at the SCK_{32} pin can be selected as the SCI3 transmit/receive clock. For selection of the clock source, one has to set the respective registers stated in the hardware manual.

When an external clock is input at the SCK_{32} pin, the clock frequency should be16 times the bit rate.

When SCI3 operates on an internal clock, the clock can be output at the SCK_{32} pin. In this case, the frequency of the output clock is the same as the bit rate and the phase is such that the clock rises at the center of each bit of transmit/receive data as shown in the Figure below in asynchronous mode.

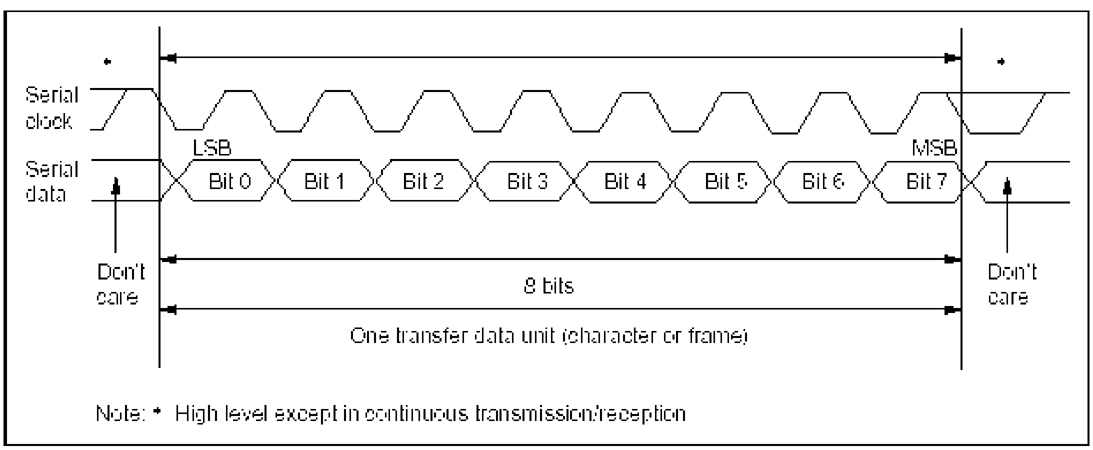


1.3.2 Synchronous Mode

Either an internal clock generated by the baud rate generator or an external clock input at the SCK_{32} pin can be selected as the SCI3 transmit/receive clock.

When SCI3 operates on an internal clock, the clock can be output at the SCK_{32} pin. Eight pulses of the serial clock are output in transmission or reception of a character.

When SCI3 is not transmitting or receiving, the clock is fixed in the high level. Refer to the Figure below for illustration.

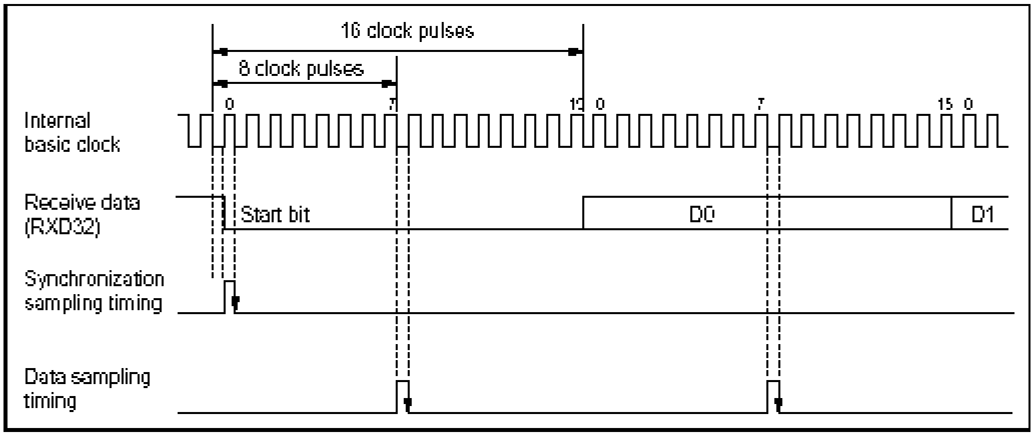


Note that when an external clock is used in asynchronous mode, the clock should not be stopped during operation including initialization. When an external clock is used in synchronous mode, the clock should not be supplied during operation including initialization.

1.4 Interrupts

SCI3 can generate six kinds of interrupts: transmit ends, transmit data empty, receive data full and three receive error interrupts (overrun error, framing, parity error). These interrupts have the same vector address. For details on the enabling and disabling of the interrupts, refer to the microcomputer hardware manual.

Last but not least, one of the key points worth highlighting here is the receive data sampling timing and receive margin in asynchronous mode. In asynchronous mode, SCI3 operates on a basic clock with a frequency 16 times the transfer rate. When receiving, SCI3 performs internal synchronization by sampling the falling edge of the start bit with the basic clock. Receive data is latched internally at the 8th rising edge of the basic clock. This is illustrated in the Figure below.



2. LCD Interface

This section aims to address the various concerns when interfacing with a LCD panel using the LCD function of the H8/38024F microcomputer. It does not go further into describing on how to set the various registers.

For H8/38024F microcomputer, it provides an on-chip segment type LCD control circuit, LCD driver, and power supply circuit, enabling it to directly drive a LCD panel. Features of the LCD driver/controller are given below:

- Display capacity

Duty Cycle	Internal Driver
Static	32 seg
1/2	32 seg
1/3	32 seg
1/4	32 seg

- LCD RAM capacity [128bits = 8bits x 16bytes]
- Word Access to LCD RAM
- Capable of parallel connection
- Display possible in all operating modes except standby mode
- Choice of 11 frame frequencies
- Built-in power supply spilt-resistance, supplying LCD drive power
- A or B waveform selectable

2.1 What is frame frequency?

The LCD frame frequency is defined as the rate at which the backplane and segment outputs change. The frame frequency is calculated to be the LCD period/2 * number of backplanes. The range of frame frequencies is from 25 to 250Hz with the most common being between 50 and 150Hz. Higher frequencies result in higher power consumption while lower frequencies cause flicker in the images on the LCD panel. The following table shows the frame frequency selection.

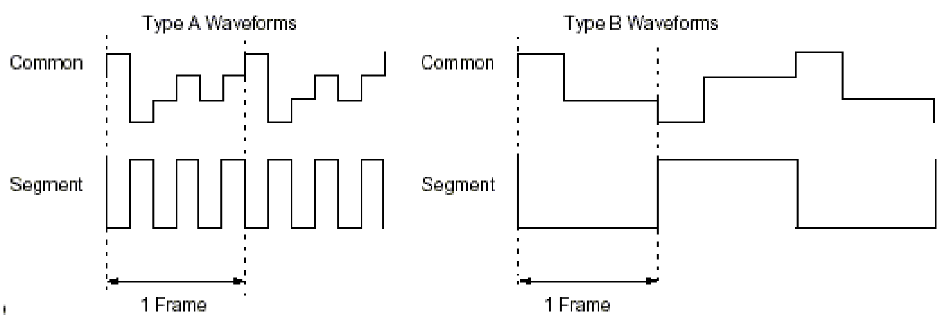
Bit 3	Bit 2	Bit 1	Bit 0		Frame Frequency*2	
CKS3	CKS2	CKS1	CKS0	Operating Clock	ø = 2 MHz	ø = 250 kHz*1
0	*	0	0	øw	128 Hz*3 (initial value)	
0	*	0	1	øw/2	64 Hz*3	
0	*	1	*	øw/4	32 Hz*3	
1	0	0	0	ø/2	—	244 Hz
1	0	0	1	ø/4	977 Hz	122 Hz
1	0	1	0	ø/8	488 Hz	61 Hz
1	0	1	1	ø/16	244 Hz	30.5 Hz
1	1	0	0	ø/32	122 Hz	—
1	1	0	1	ø/64	61 Hz	—
1	1	1	0	ø/128	30.5 Hz	—
1	1	1	1	ø/256	—	—

*: Don't care

Notes: *1 This is the frame frequency in active (medium-speed, øosc/16) mode when ø = 2 MHz.
*2 When 1/3 duty is selected, the frame frequency is 4/3 times the value shown.
*3 This is the frame frequency when øw = 32.768 kHz.

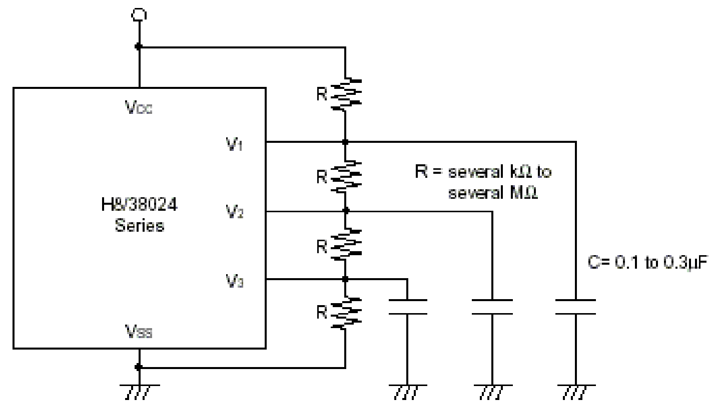
2.2 What is drive waveform?

Two types of waveforms are used to drive LCD panel, namely type A and type B. A LCD driver must maintain a 0 V_{DC} across each pixel. Type A waveforms maintain 0 VDC over a single frame whereas type B takes two frames. The following Figure illustrates the different type drive waveforms.



2.3 How to boost the LCD Drive Power?

When a large LCD panel is used, the on-chip power supply capacity may be insufficient. If the power supply is insufficient when VCC is used as the power supply, the power supply impedance must be reduced. How do we go about doing it? You can connect a bypass capacitor of value around 0.1uF to 0.3uF to pins V1 to V3 or by adding spilt-resistance externally. This following Figure illustrates the connection of the external spilt-resistance.



2.4 How to operate LCD controller/driver in Power Down Modes

In the H8/38024 series, the LCD controller/driver can be operated even in the power-down modes.

Note that in subactive, watch mode and subsleep mode, the system clock oscillator stops and therefore, unless the on-chip subclock is selected, the clock will not be supplied and display will halt. Since there is a possibility that a direct current will be supplied to the LCD panel in this case, it is essential to ensure that subclock is selected. In active(medium-speed) mode, the system clock is enabled, therefore the frame frequency setting must be modified to ensure that the frame frequency does not change. You may refer to the section 2.1 in this application note concerning the frame frequency selection.

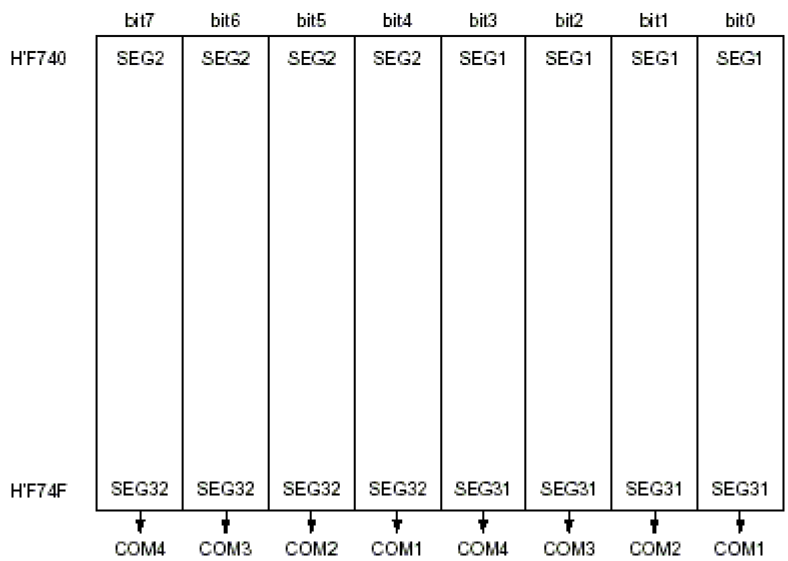
Mode		Reset	Active	Sleep	Watch	Sub-active	Sub-sleep	Standby	Module Standby
Clock	ø	Runs	Runs	Runs	Stops	Stops	Stops	Stops	Stops*4
	øw	Runs	Runs	Runs	Runs	Runs	Runs	Stops*1	Stops*4
Display	ACT = 0	Stops	Stops	Stops	Stops	Stops	Stops	Stops*2	Stops
operation	ACT = 1	Stops	Functions	Functions	Functions*3	Functions*3	Functions*3	Stops*2	Stops

Notes: *1 The subclock oscillator does not stop, but clock supply is halted.
*2 The LCD drive power supply is turned off regardless of the setting of the PSW bit.
*3 Display operation is performed only if øw, øw/2, or øw/4 is selected as the operating clock.
*4 The clock supplied to the LCD stops.

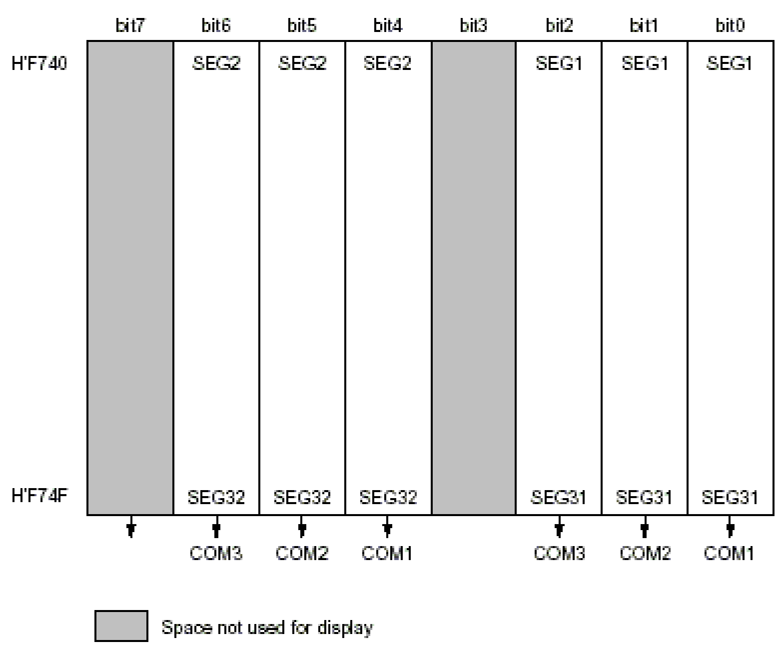
2.5 Relationships between LCD RAM and Duty Cycle

The relationships between the LCD RAM and the display segments differ according to the duty cycle. After setting the registers required for display, data is written to the part corresponding to the duty using the same kind of instruction as for ordinary RAM, and the display is started automatically when turned on. Word- or byte-access instructions can be used for RAM setting.

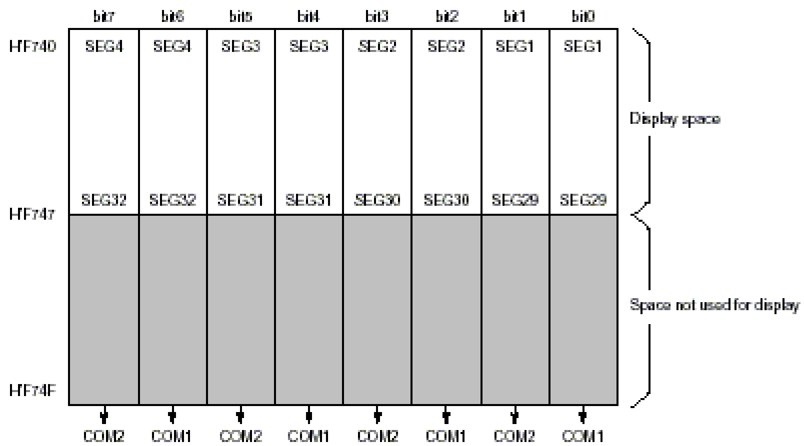
The following Figures illustrate the relationship between LCD RAM and various duty cycle supported.



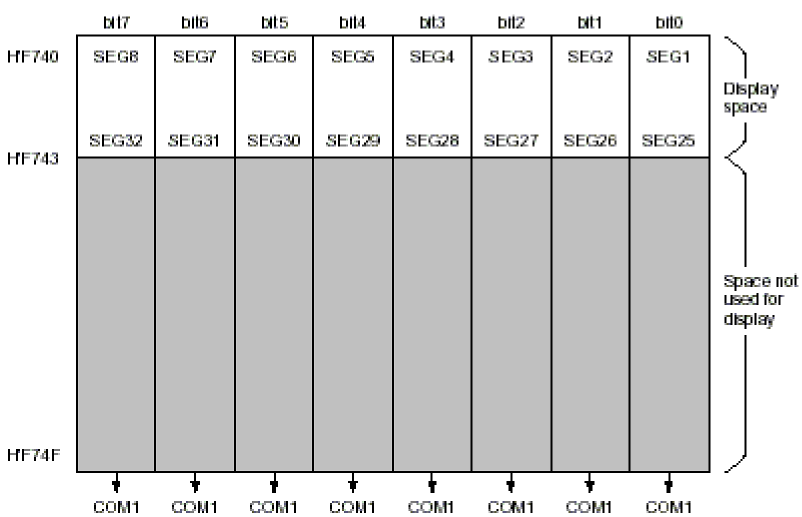
LCD RAM Map with ¼ Duty Cycle



LCD RAM Map with 1/3 Duty Cycle



LCD RAM Map with ½ Duty Cycle



LCD RAM Map with Static Mode

2.6 Electrical Characteristic

The electrical characteristic for the LCD controller/driver differs for mask & F-ZTAT version. Product designer has to take note of this difference to ensure correct operation. In addition to this, product designer also has to consult the electrical specification of the LCD panel provided by the LCD manufacturer to ensure that the LCD driver/controller is suitable to drive the LCD panel used.

The followings tables provide the readings for both mask and F-ZTAT version.

2.6.1 Mask or Z-TAT version

V_{CC} = 1.8 V to 5.5 V, AV_{CC} = 1.8 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = –20°C to +75°C*3 (including subactive mode) unless otherwise specified.

Item	Symbol	Applicable Pins	Test Conditions	Values Min	Typ	Max	Unit	Reference Figure
Segment driver drop voltage	V_{DS}	SEG_1 to SEG_{32}	I_D = 2 µA, V_1 = 2.7 V to 5.5 V	—	—	0.6	V	*1
Common driver drop voltage	V_{DC}	COM_1 to COM_4	I_D = 2 µA, V_1 = 2.7 V to 5.5 V	—	—	0.3	V	*1
LCD power supply split-resistance	R_{LCD}		Between V_1 and V_{SS}	0.5	3.0	9.0	MΩ	
Liquid crystal display voltage	V_{LCD}	V_1		2.2	—	5.5	V	*2

Notes: *1 The voltage drop from power supply pins V_1, V_2, V_3, and VSS to each segment pin or common pin.

*2 When the liquid crystal display voltage is supplied from an external power source, ensure that the following relationship is maintained: $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq V_{SS}$.

*3 The guaranteed temperature as an electrical characteristic for Die products is 75°C.

2.6.2 F-ZTAT version

V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_a = –20°C to +75°C*3 (including subactive mode) unless otherwise specified.

Item	Symbol	Applicable Pins	Test Conditions	Values Min	Typ	Max	Unit	Reference Figure
Segment driver drop voltage	V_{DS}	SEG_1 to SEG_{32}	I_D = 2 µA, V_1 = 2.7 V to 3.6 V	—	—	0.6	V	*1
Common driver drop voltage	V_{DC}	COM_1 to COM_4	I_D = 2 µA, V_1 = 2.7 V to 3.6 V	—	—	0.3	V	*1
LCD power supply split-resistance	R_{LCD}		Between V_1 and V_{SS}	0.5	3.0	9.0	MΩ	
Liquid crystal display voltage	V_{LCD}	V_1		2.2	—	3.6	V	*2

Notes: *1 The voltage drop from power supply pins V_1, V_2, V_3, and VSS to each segment pin or common pin.

*2 When the liquid crystal display voltage is supplied from an external power source, ensure that the following relationship is maintained: $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq V_{SS}$.

*3 The guaranteed temperature as an electrical characteristic for Die products is 75°C.

Reference

1. H8/38024 Series, H8/38024F-ZTAT™ Hardware Manual

2. www.embedded.com

3. www.ednmag.com

Revision Record

Rev.	Date	Description: Page	Description: Summary
1.00	Sep.03	-	First edition issued