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H8/300L

Hardware Interface Technique to IO Port (HWio)

Introduction

This application note is to assist the product design engineers to consider the various electrical characteristics and behaviors of all IO ports that are based on CMOS logic to ensure correct operation when implementing with them. In addition, it would also highlights the numerous concerns when designed with CMOS logic and also system involves multiple voltages.

In this application note, H8/38024F microcomputer is used as the example.

Target Device

H8/300L Super Low Power series – H8/38024F

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1. Electrical Characteristics of IO Ports

For H8/38024F microcomputer, there are a total of ten IO ports, namely port 1,3,4,5,6,7,8,9 and A. The following table shows the electrical reading of V_{IL} , V_{IH} , V_{OL} , and V_{OH} for all the IO ports for H8/38024F microcomputer:

Item	Symbol	Application Pins	Values			Unit	Notes
			Min.	Typical	Max.		
Input High Voltage	V_{IH}	P ₁₃ , P ₁₄	0.8VCC	-	VCC+0.3V	V	
		P ₁₆ , P ₁₇					
		P ₃₀ to P ₃₇					
		P ₄₀ to P ₄₃					
		P ₅₀ to P ₅₇					
		P ₆₀ to P ₆₇					
		P ₇₀ to P ₇₇					
		P ₈₀ to P ₈₇					
		P _{A0} to P _{A3}					
		P _{B0} to P _{B7}	0.8VCC	-	AVCC+0.3V		V
P95	0.9VCC	-	7.3	V			
Input Low Voltage	V_{IL}	P ₁₃ , P ₁₄	-0.3	-	0.2VCC	V	
		P ₁₆ , P ₁₇					
		P ₃₀ to P ₃₇					
		P ₄₀ to P ₄₃					
		P ₅₀ to P ₅₇					
		P ₆₀ to P ₆₇					
		P ₇₀ to P ₇₇					
		P ₈₀ to P ₈₇					
		P _{A0} to P _{A3}					
		P _{B0} to P _{B7}					

Item	Symbol	Application Pins	Values			Unit	Notes
			Min.	Typical	Max.		
Output High Voltage	V _{OH}	P ₁₃ , P ₁₄	VCC-1.0	-	-	V	-I _{OH} = 1.0mA
		P ₁₆ , P ₁₇	VCC-0.3	-	-	V	-I _{OH} = 0.1mA
		P ₃₀ to P ₃₇					
		P ₄₀ to P ₄₂					
		P ₅₀ to P ₅₇					
		P ₆₀ to P ₆₇					
		P ₇₀ to P ₇₇					
		P ₈₀ to P ₈₇					
Output Low Voltage	V _{OL}	P _{A0} to P _{A3}					
		P ₁₃ , P ₁₄	-	-	0.5	V	I _{OL} = 0.4mA
		P ₁₆ , P ₁₇					
		P ₃₀ to P ₃₇					
		P ₄₀ to P ₄₂					
		P ₅₀ to P ₅₇					
		P ₆₀ to P ₆₇					
		P ₇₀ to P ₇₇					
		P ₈₀ to P ₈₇					
		P _{A0} to P _{A3}					
		P ₉₀ to P ₉₂	-	-	0.5	V	I _{OL} = 25mA I _{OL} = 10mA
		P ₉₃ to P ₉₅	-	-	0.5	V	I _{OL} = 10mA

2. Electrical Behavior on CMOS Logic

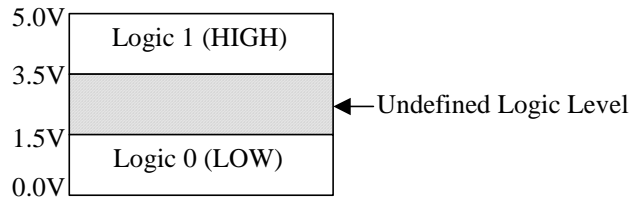
Having described in the previous section, the electrical characteristics of the IO ports for the H8/38024F microcomputer, the following section would explain briefly about the functional behavior of a CMOS logic circuit and MOS transistors. In addition, it would also explain the electrical behavior of CMOS logic to aid the product design engineer with a better understanding of the operation with CMOS logic.

The functional behavior of a CMOS logic circuit is fairly easy to understand, the basic building blocks in CMOS logic circuits are MOS transistors. However, before we mentioned anything further for the CMOS logic circuits and MOS transistors, we would briefly about logic levels

2.1 CMOS Logic Levels

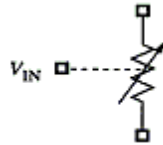
Abstract logic elements process binary digits, 0 and 1. However, real logic circuits process electrical signals such as voltage level.

In any logic circuit, there is a range of voltages (or other circuit conditions) that is interpreted as logic 0, and another, non-overlapping range that is interpreted as logic 1. A typical CMOS logic circuit may interpret any voltage in the range 0~1.5V as a logic 0, and in the range 3.5~5.0V as a logic 1. Voltages in the intermediate range (1.5~3.5V) are not expected to occur except during signal transitions and yield undefined logic values.



2.2 MOS Transistors

A MOS transistor can be modeled as a 3-terminal device that acts like a voltage controlled resistance. As suggested in the figure below, an input voltage applied to one terminal controls the resistance between the remaining two terminals. In digital logic applications, a MOS transistor is operated so its resistance is always either very high (and the transistor is 'off') or very low (and the transistor is 'on').



There are two types of MOS transistors, n-channel and p-channel; in this application, it will not discuss the configuration of the n-MOS and p-MOS transistor. Instead, it will explain the electrical behavior during operation. The voltage from gate to source (V_{gs}) in an NMOS transistor is normally zero or positive. If $V_{gs}=0$, then the resistance from drain to source (R_{ds}) is very high, on the order of a mega-ohm or more. As we increase V_{gs} (i.e. increases the voltage at the gate), R_{ds} decreases to a very low value, 10 ohms or less in some devices. In the case of PMOS transistor, the operation is analogous to that of NMOS transistor, except that the source is normally at a higher voltage than the drain, and V_{gs} is normally zero or negative. If V_{gs} is zero, then the resistance from the source to drain (R_{ds}) is very high. Theoretically, as we decrease V_{gs} (i.e. decrease the voltage on the gate), R_{ds} decreases to a very low value.

The following describes the electrical aspects when interfacing with CMOS port pins and the topics include:

- DC noise margin

Depending on loading and other factors, a CMOS output signal has a certain voltage in the LOW state, and another voltage in the HIGH state. Non-negative DC noise margins ensure that the highest LOW voltage produced by an output is always lower than the highest voltage that an input can reliably interpret as LOW, and the lowest HIGH voltage produced by an output is always higher than the lowest voltage that an input can reliably interpret as HIGH.

- Fan-out

This refers to the number and type of inputs that are connected to a given output. If too many inputs are connected to an output, the DC noise margins of the circuit may be inadequate. Fan-out may also affect the speed at which the output changes from one state to another.

- Speed

The time that it takes a CMOS output to change from the LOW state to the HIGH state, or vice versa, depends on both the internal structure of the device and the characteristics of the other devices that it drives, even to the extent of being affected by the wire or PCB traces connected to the output.

- Power Consumption

The power consumed by a CMOS device depends on a number of factors, including not only its internal structure, but also the input signals that receive, the other devices that it drives, and how often its output changes between LOW and HIGH.

- Noise

The reason for providing engineering design margin is to ensure proper circuit operation in the presence of noise. Noise can be generated by a number of sources such as cosmic rays, magnetic fields from nearby machinery, etc.

- Electrostatic Discharge

This can easily killed a CMOS device by merely touching it.

- Open-Drain outputs

Some CMOS output omits the usual p-channel pull up transistors. In HIGH state, such outputs are effectively a no-connection that is useful in some application.

The p-channel transistors in CMOS output structures are said to provide active pull-up since they actively pull the output voltage on a LOW-to-HIGH transition. These transistors are omitted in gates with open-drain outputs. The drain of the topmost n-channel transistor is left unconnected internally, so if the output is not LOW, it is open. An open-drain output requires an external pull-up resistor to provide passive pull-up to the HIGH level.

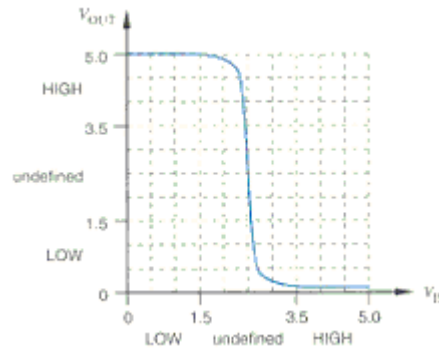
For the highest possible speed, an open-drain output's pull-up resistor should be as small as possible; this minimizes the RC time constant for LOW-to-HIGH transitions (rise time). However, the pull-up resistance cannot be arbitrarily small; the minimum resistance is determined by the open-drain output's maximum sink current, I_{OLmax} . Though open-drain gate exhibits slow rise time, they are useful for applications such as driving LEDs and other devices; performing wired logic; and driving multi-source buses.

- Three-state outputs

Some CMOS output have an extra output-enable control input that can be used to disable both the p-channel pull transistors and the n-channel pull-down transistors. Many such device outputs can be tied together to create a multi-source bus, as long as the control logic is arranged so that at most one output is enabled at a time.

2.3 CMOS Steady-State Electrical Behavior

The circuit's behavior when inputs and outputs are not changing. As an example, the CMOS inverter's behavior is defined as two discrete input voltages; other input voltages may yield different output voltages. The complete input-output transfer characteristic can be described by a graph as indicated in the figure below



In ideal case, we could define a CMOS LOW input level as any voltage under 2.4V, and a HIGH input level as anything over 2.6V. Only when the input is between 2.4V and 2.6V does the inverter produce a non-logic output voltage under this definition. Unfortunately, the typical transfer characteristic in the above figure is just typical but not guaranteed as it is dependent on power supply voltage, temperature and output loading.

Sound engineering practice dictates that we use more conservative specification for LOW and HIGH. The parameters are specified by CMOS device manufacturers in a data sheet and defined as follows:

- V_{OHmin}
- V_{IHmin}
- V_{ILmax}
- V_{OLmax}

The input parameters are determined mainly by switching thresholds of the two transistors, while the output parameters are determined mainly by the “ON” resistance of the transistors. These parameters apply when the device inputs and outputs are connected only to other CMOS devices.

For example, to illustrate for DC noise margin, at 1.5V, V_{ILmax} exceeds V_{OLmax} by 1.4V, so HC-series CMOS has a DC noise margin of 1.4V in the LOW state. That is, it takes at least 1.4V of noise to corrupt a worst-case LOW output into a voltage that is not guaranteed to be recognized by another gate as a LOW input. There is also a DC noise margin of 1.4V in the HIGH state.

Another consideration needs to be given is the load condition and it is specified in terms of current.

- I_{OLmax} : The maximum current that the output can sink in the LOW state while still maintaining an output voltage no greater than V_{OLmax} .
- I_{OHmax} : The maximum current that the output can source in the HIGH state while still maintaining an output voltage no less than V_{OHmin} .

Most CMOS devices have two sets of loading specifications. One set is for “CMOS” loads, meaning that the device output is connected to other CMOS loads, meaning that the device output is connected to other CMOS inputs, which consumes very little current. The other set is for “TTL” loads, meaning that the output is connected to TTL inputs or other devices that consume significant current.

For non-ideal inputs such that the input voltage is not closed to the power supply rail, then the “ON” transistor may not be fully “ON” and its resistance may increase. Likewise, the “OFF” transistor may not be fully “off” and its resistance may be quite a bit less than one mega-ohm. These two effects combine to move the output voltage away from the power-supply rail.

3. Effects of Loading

Besides the understanding about the electrical characteristics, other consideration should also go to stuffs such as the effect of loading on the system. Loading an output with more than its rated fan-out has several effects:

- In the LOW state, the output voltage (V_{OL}) may increase beyond V_{OLmax} .
- In the HIGH state, the output voltage (V_{OH}) may fall below V_{OHmin} .
- Propagation delay to the output increase beyond specification
- Output rise and fall times may increase beyond their specification
- The operating temperature of the device may increase, thereby reducing the reliability of the device and eventually causing device failure.

The first four effects reduce the DC noise margin and timing margins of the circuit. Thus, slightly overloaded circuit may work properly in ideal conditions, but experience says that it will fail once it's out of the friendly environment of engineering laboratory.

4. Unused CMOS Inputs

Unused CMOS inputs should never be left unattended (or floating). On one hand, such an input will behave as if it had a LOW signal applied to it and will normally show a value of 0V when probed with an oscilloscope or voltmeter. However, CMOS inputs have such high impedance, it takes only a small amount of circuit noise to temporarily make a floating input look HIGH, creating some very nasty inter-mitten circuit failures. Some subtle bugs concerning floating CMOS inputs are, often the cause of mysterious circuit behavior, as an unused input erratically changes its effective state based on noise and conditions elsewhere in the circuit. When you are trying to debug such a problem, the extra capacitance of an oscilloscope probe touched to the floating input is often enough to damp out the noise and make the problem go away. This can be baffling if you don't realize that the input is floating!

5. Current Spikes and Decoupling Capacitors

When a CMOS output switches between a LOW and HIGH, current flows from VCC to ground through the partially on p- and n-channel transistors. These current often called current spikes because of their duration, may show up as noise on the power-supply and ground connections in a CMOS circuit, especially when multiple outputs are switched simultaneously.

For this reason, systems that use CMOS circuits require decoupling capacitors between VCC and ground. These capacitors must be distributed throughout the circuit, at least one within an inch or so of each chip, to supply current during transitions. The large filtering capacitors typically found in the power supply itself do not satisfy this requirement, because stray wiring inductance prevents them from supplying the current fast enough, hence the need for physical distributed system of decoupling capacitors.

The following example shows the calculation of the decoupling capacitor value when designing with H8/38024F:

If you are switching all the IO ports, therefore the current demanded by the microcomputer for all IO ports is 100mA (ΣI_{OL} from H8/38024F microcomputer hardware manual). If you consider some droop from the power bus and the switching time is 31.25nsec, and allows a maximum voltage dip (ΔV) on the H8/38024F microcomputer is -0.1V, the choice of bypass capacitor become:

$$C = \frac{I \cdot dt}{dV}$$

$$dV$$

$$C = 0.03\mu F$$

Therefore, choosing a 0.1uF will allow for variations due to temperature and aging.

Selecting a correct bypass capacitor in a high-speed design has economic and design reliability consequences. You may be tempted to place any large value capacitor across the power pins for bypass. But choosing a value that exceeds the necessary value can result in higher series inductance, increased expense, and inferior electrical or nominal value stability characteristics.

Therefore, the bypass capacitor should have low effective series resistance (ESR) and series inductance while having a large enough capacitance value to supply current to the IC during switching.

6. Logic Families

The following table mentioned some of the logic families that are available for applications with specific voltage operation capability.

Logic Family Type	Application
LVC (Low Voltage CMOS)	Low voltage operation 2.7V to 3.6V with 3.3V/5.5V tolerant inputs
LVCI (Low Voltage CMOS)	Low voltage ranging from 1.65V to 5.5V operation
LCX (Low Voltage CMOS)	Interface with 3V and 5V devices.
LVQ (Low Voltage Quiet CMOS)	Ideal for low power/low noise application

The suitability of employing these above mentioned logic families is dependent on your application and therefore consultation with the manufacturer's data sheet is necessary.

7. MOS Pull-Up Transistor

Before it was forgotten, I would also like to mention here that certain IO ports within the H8/38024F microcomputer have built-in MOS pull-up function that can be selected by software. This is useful for product designers whom may have a need to provide pull-up function in their application.

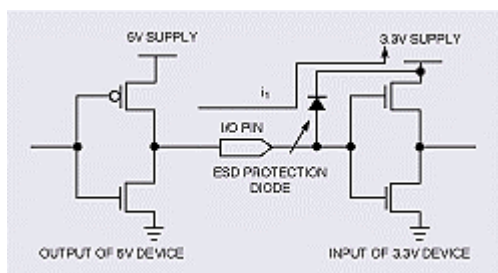
8. Large Current High Voltage Open-Drain IO Ports

For H8/38024F microcomputer, there exists a large current of 10mA & 25mA, high voltage of 7V open-drain pin, capable of driving large load such as LEDs, stepper motors etc. The large current drive can be enabled or disabled by register settings.

9. Consideration for 3 Volt and 5 Volt Interface

The following guidelines apply to a design that integrates 3.3V and 5V devices. Interfacing 3V TTL or CMOS devices to 5V CMOS devices causes problems because the 5V devices need extra drive to prevent leakage current. Many voltage translation devices translate 3.3V to 5V, however, this solution adds delay and board space.

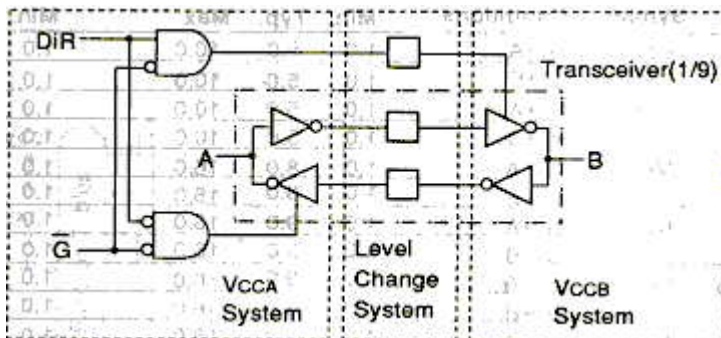
Interfacing 3V CMOS devices to 5V TTL devices doesn't compromise performance because a 3V device outputs have sufficient margin to drive 5V TTL-device inputs. However, you cannot directly connect a 5V output to a 3V input. Driving a 3V input, a 5V output can exceed the maximum supply-voltage rating and can forward-bias the ESD protection diode. The diode allows excess current to flow from the 5V device into the 3V power supply, possibly inducing latch-up. In this case, using a voltage-translation device is necessary. Refer to figure below.



If board space is critical and speed is not, you can place a series resistor between the 3V and 5V devices to limit the current flowing from 5V device into 3V device. The series resistor is placed such that the current before the series resistor is less than the current after the series resistor. The value calculated should take into consideration the electrical rating of the I_{OL} for the 3V device to ensure that the device can sink the current from the 5V device. This case of voltage translation is unidirectional.

However, in the case of bus application, it may require bi-directional interfaces such as Renesas level shifter, HD1510151, which has 3V or 5V signals driving the control inputs. Regardless of whether a 3V device resides on a 5V bus or a 5V device resides on a 3V bus, run the bus at one voltage and use translation circuitry and buffers between the other devices. Such bi-directional interface comprises of two terminals (V_{CCA} , V_{CCB}), V_{CCA} is connected with control input and A bus side, V_{CCB} is connected with B bus side. V_{CCA} and V_{CCB} are isolated. This interface is able to change V_{CCA} input level to V_{CCB} output level and vice versa by providing different supply voltages to V_{CCA} and V_{CCB} . The figures below show the HD1510151 circuitries for such implementation.

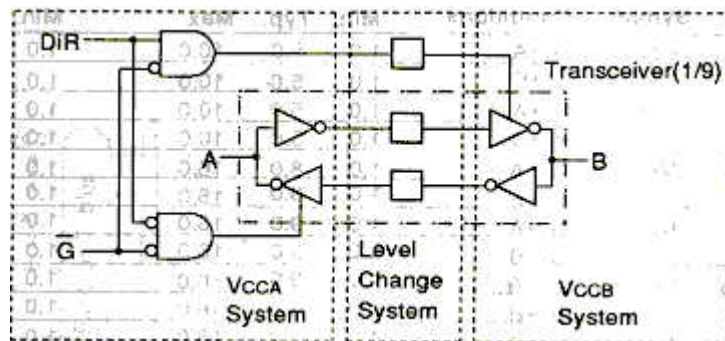
Logic Diagram



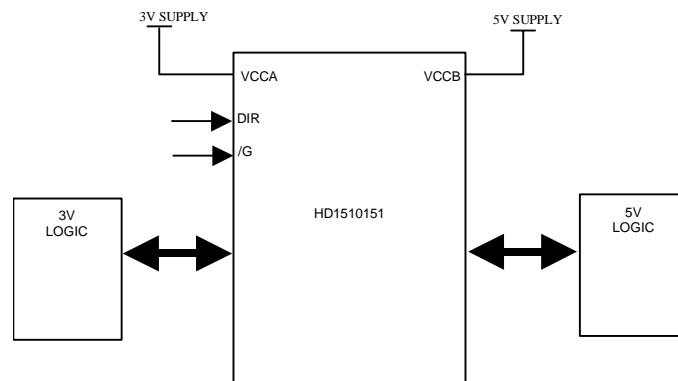
The following shows the truth table for HD1510151.

Inputs		Outputs
/G	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	High-Impedance, Z

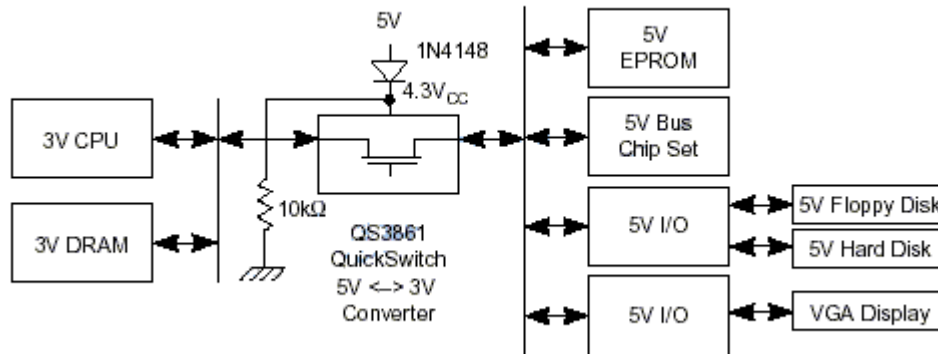
Input and Output Equivalent Circuit



Connection Circuitry



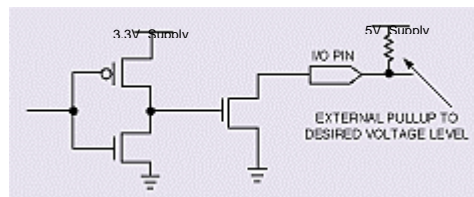
The following provides another example for the bi-directional interface using the part from Quality Semiconductor called the QuickSwitch such as the QS3861. The output limiting characteristics of the QuickSwitch can be used to make a very efficient 5V TTL to 3V TTL converter. By supplying 4.3V to the VCC pin of a QuickSwitch device, the driven output will be limited to 3.3V maximum., even under light loading. Adding a diode such as 1N4148 between the 5V supply and the device can create a 4.3V VCC. The diode will provide approximately 0.70V drop, supplying the QS3861 with a VCC of 4.3V. A 10KΩ resistor is added between the diode's cathode and ground to provide a current path for the diode. Note that the conversation is bi-directional and automatic. If either side is driven to 5V, the driven will be limited to 3.3V.



De-rating a 5V device for use as a 3V device may cause insufficient drive capability. The 3V devices operate at lower supply voltages, lowering the devices' output-drive capabilities. If you want to use these devices in bus applications, determine whether the parts are de-rated or truly low-voltage devices: A de-rated part often offers lower performance than that of an equivalent 5V device, whereas a true low-voltage design perform as well as or better than its 5V counterpart.

Another possibility for interfacing 5V and 3V devices is to use a device with an open-drain output configuration. These devices act a buffer and ensure safe operation of 3.3V devices. However, a device with an open-drain option may have an internal pull-up transistor whose parasitic diode may forward-bias, causing current to flow. A true open-drain device requires only an external pull-up resistor to the desired voltage. For highest possible speed, an open-drain output's pull-up resistor should be as small as possible. This is explained in the section 2.2 under *Open-Drain outputs*.

To calculate the minimum resistance required is determined by the open-drain output's maximum sink current, I_{Omax} . For example, in HC- and HCT-series CMOS, I_{Omax} is 4mA, and the pull-up resistor can be no less than $5.0V / 4mA$, or 1.25kΩ. Refer to Figure below.



Another possibility for interfacing 5V and 3V device is, to modify the input and output structures of a device so that internal voltage translations can occur. Occasionally, you can use a true CMOS transmission gate at the output.

Hybrid systems which include multiple voltage supplies, hence you must prevent latch-up on the IOs during power-up and power-down. To prevent latch-up on power-up, make sure that the 5V supply is greater than or equal to the 3V supply. To prevent latch-up on power-down, the 3V supply should be less than or equal to 5V supply.

To take full advantage of the two voltage devices, mix the design on the board so that speed-critical paths run at 5V and low-power paths run at 3.3V.

10. Conclusions

This application note hopes to help product designers to have a better understanding of working with CMOS logic pins by describing its electrical characteristics and behavior. In addition, it also explains the effect of loading and provides some pointers on how to derive the correct value for bypass capacitor for CMOS logic to ensure proper operation. It also highlighted some pointers for designing system with multiple voltage requirements.

Reference

1. H8/38024 Series, H8/38024F-ZTAT™ Hardware Manual
2. Renesas Interface IC, HD26/29/75/151 Series Data Book
3. www.ednmag.com
4. www.embedded.com
5. www.idt.com

Revision Record

Rev.	Date	Description	
		Page	Summary
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