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H8SX Family

Two-Phase Excitation Control of a Stepping Motor

Introduction

This application note discusses two-phase excitation control of a stepping motor using the TPU, PPG, and DTC functions incorporated in the H8SX/1657F.

Target Device

H8SX/1657F (advanced mode & 16M-byte address map mode)

Contents

1. Specifications

- A two-phase stepping motor is controlled by using the TPU, PPG, and DTC functions incorporated in the H8SX/1657F.
- The stepping motor is controlled through two-phase excitation and repeats the following sequence: forward rotation → stop → reverse rotation → stop.
- The sample task demonstrates speed-up and slow-down processing without software intervention.
- To protect the driver, a shoot-through current prevention period is set.

Figure 1 shows the connections for two-phase stepping motor control.

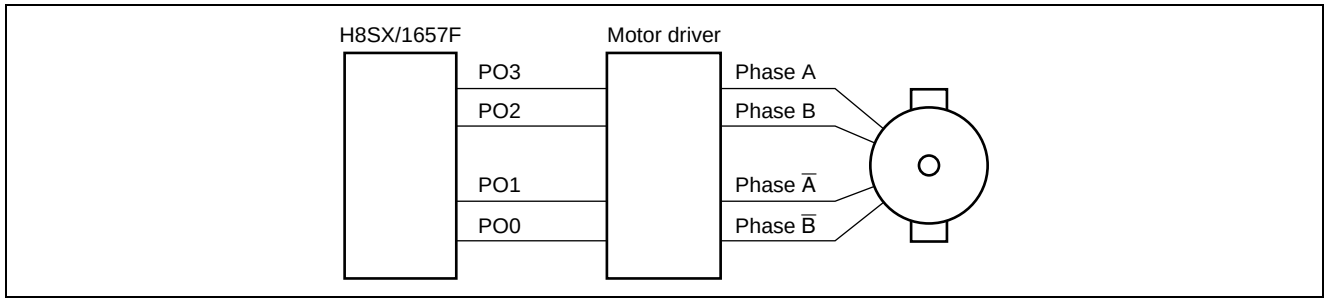


Figure 1 Connections for Two-Phase Stepping Motor Control

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Contents	
Operating frequency	Input clock:	17.5 MHz
	System clock:	35 MHz
	Peripheral module clock:	35 MHz
	External bus clock:	35 MHz
Operating mode	Mode 6 (MD2 = 1, MD1 = 1, MD0 = 0)	
Development tool	HEW Version 3.01.06	
C/C++ compiler	H8S, H8/300 SERIES C/C++ Compiler Version 6.00.00 (from Renesas Technology Corp.)	
Compile option	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3 -speed = (register, shift, struct, expression)	

Table 2 Section Settings

Address	Section Name	Description
H'000000	CV1	Reset vector
H'000160	CV2	TPU TGI0A interrupt vector
H'001000	P	Program area
	C	Data table storage
H'FF7000	B	RAM area
H'FF8560	DDTCV	DTC activation source vector

3. Description of Functions

3.1 Motor Specifications

This sample task uses a permanent magnet-type stepping motor (KP6P8-701 manufactured by Japan Servo Co., Ltd.). Table 3 summarizes the standard specifications of the KP6P8-701.

Table 3 Standard Specifications of KP6P8-701

Item	Specification
Model	KP6P8-701
Number of phases	2
Stepping angle [deg./step]	7.5
Voltage [V]	12
Current [A/phase]	0.33
Winding resistance [Ω/phase]	36
Inductance [mH/phase]	28
Maximum static torque [mN•m]	78.4
Detent torque [mN•m]	1.3
Rotor inertia [g•cm^2]	23.7

3.2 H8SX/1657F Functions

The H8SX/1657F functions used to control the stepping motor are described below. Figure 2 is a block diagram of the functions used in this sample task.

- DTC
  - Activated by compare-match A of the TPU.
  - Transfers an output pattern in the output pattern table to the NDR register of the PPG. After the transfer of an output pattern, the DTC transfers the pulse period data in the period data table to the TGRB register of the TPU by chain transfer.
- TPU
  - Compare-match A: Activates the DTC and PPG.
  - Compare-match B: Clears the timer counter and activates the PPG.
- PPG
  - In this sample task, outputs 4 bits of pulse signals that include shoot-through current prevention period (non-overlap time).
  - Compare-match B: Outputs pulse signals of high-to-low transition and suspends output of low-to-high transition.
  - Compare-match A: Outputs the low-to-high pulse signals that are suspended on compare-match B above. (This output is delayed by the time set by TGRA.)

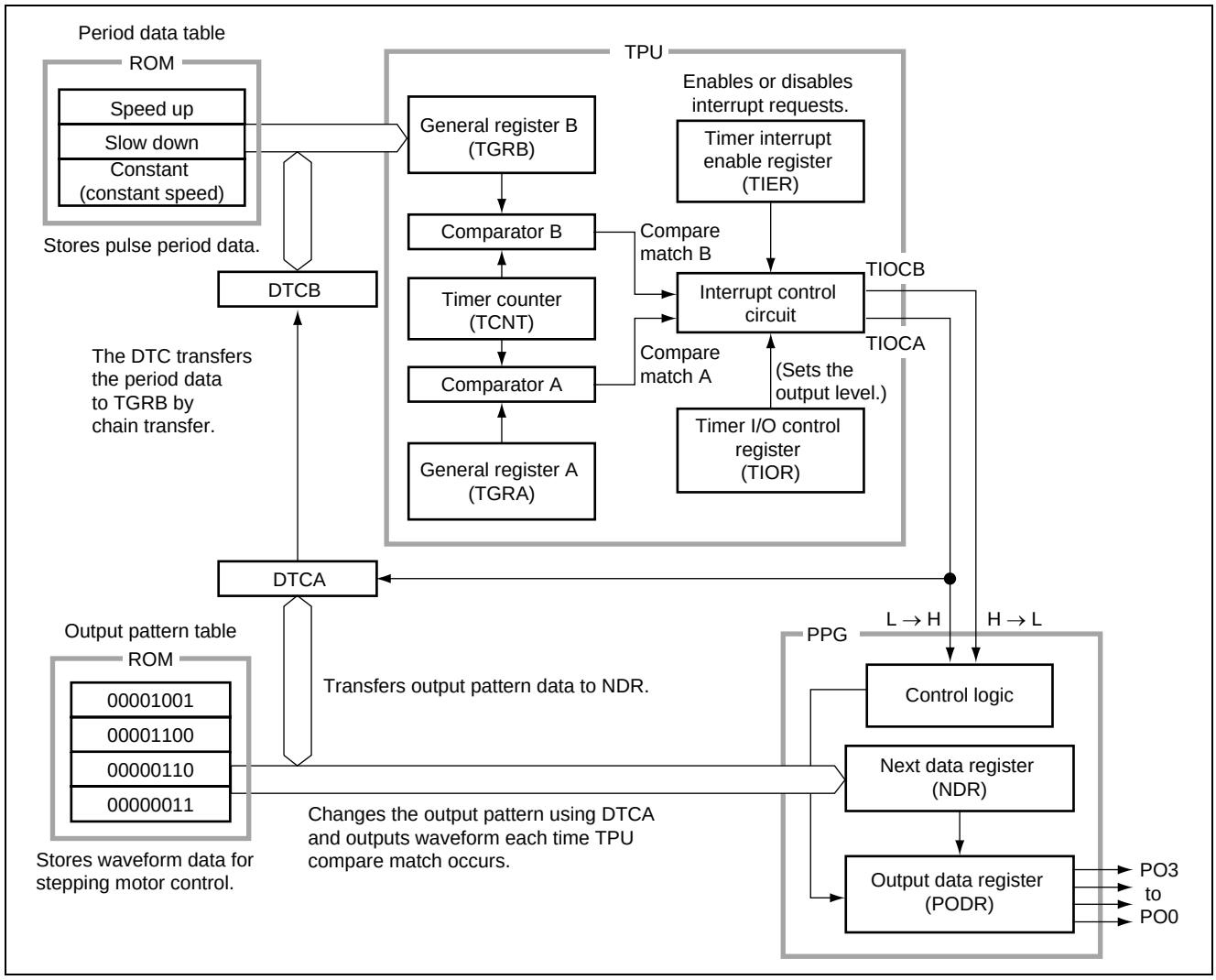


Figure 2 H8SX/1657F's Functions Used in This Application

3.3 DTC Vector Table

Figure 3 shows the DTC vector table and data arrangement in memory. The DTC transfer information should be stored to the addresses from H'FF6000 in the following order: MRA, SAR, MRB, DAR, CRA, and CRB.

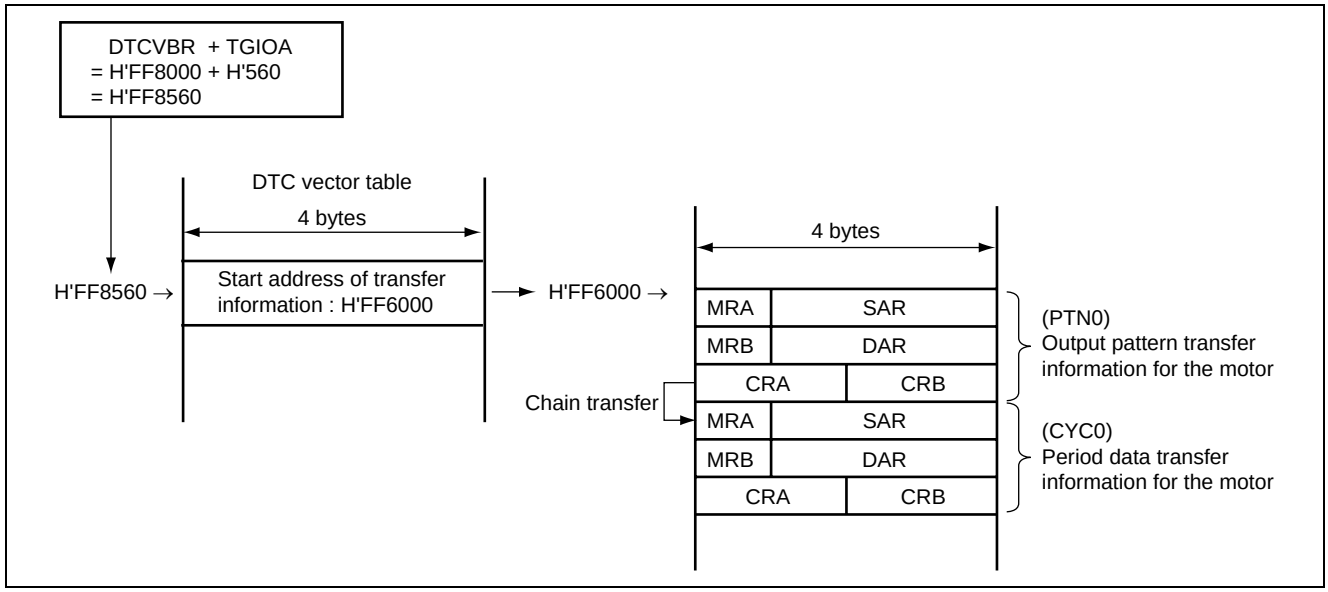


Figure 3 Example of DTC Vector Table and Data Arrangement in Memory

4. Description of Operation

4.1 Stepping Motor Operation

Figure 4 shows an example of two-phase stepping motor operation through two-phase excitation where the step angle of the motor is 7.5 degrees/step. The operation is summarized below.

- When the output pulse is high, the corresponding phase is excited, as shown in figure 4.
- Firstly, phases A and $\overline{B}$ are excited and the rotor is positioned between phases $\overline{B}$ and A.
- Next, phases A and B are excited simultaneously and the rotor is positioned between phases A and B. Subsequently, two adjacent phases are excited in the following sequence to cause the rotor to rotate: phases $\overline{B}$ and A $\rightarrow$ phases A and B $\rightarrow$ phases B and $\overline{A}$ $\rightarrow$ phases $\overline{A}$ and $\overline{B}$.
- Reverse rotation of the stepping motor is achieved by exciting the phases in the reverse sequence: phases $\overline{A}$ and $\overline{B}$ $\rightarrow$ phases B and $\overline{A}$ $\rightarrow$ phases A and B $\rightarrow$ phases $\overline{B}$ and A.
- The stepping motor is stopped by holding the phase excitation for a specified period at the last phase of forward or reverse rotation.

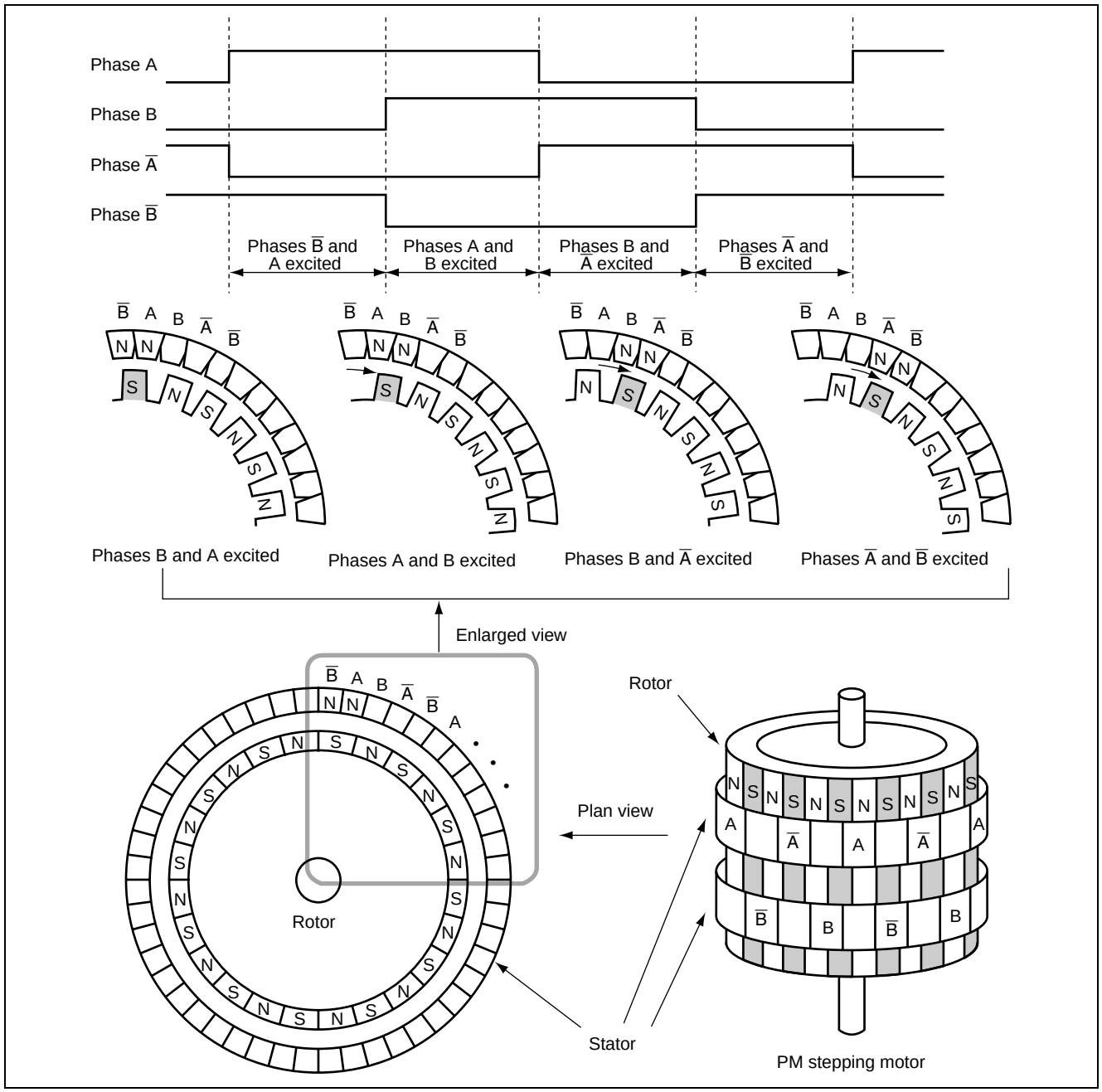


Figure 4 Example of Stepping Motor Operation

4.2 Non-Overlap Time

When the output pattern is switched, the shoot-through current prevention period n (non-overlap time) is inserted as shown in figure 5. The motor driver may be damaged by a turn-off delay that occurs when the excitation pattern is switched. Non-overlap time is inserted to prevent this problem.

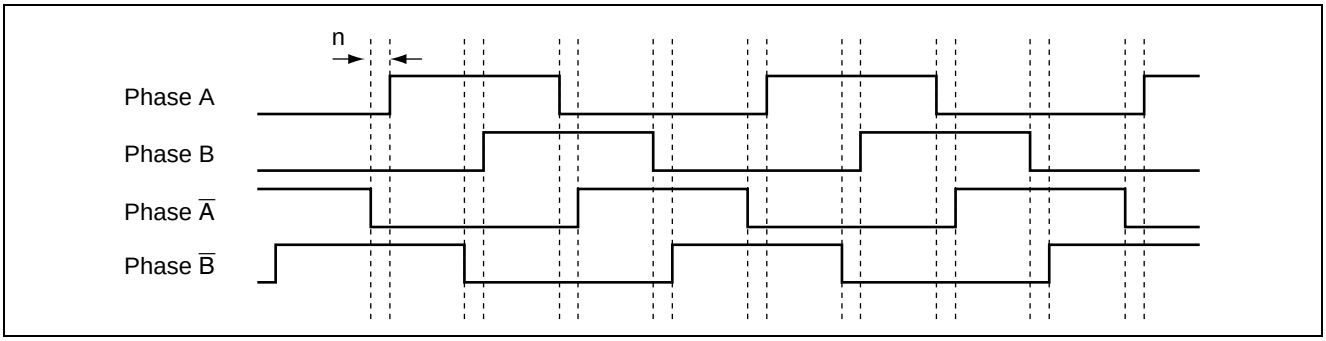


Figure 5 Example of Output with Non-Overlap Time

4.3 Speed-Up and Slow-Down Operation

Speed-up and slow-down operations effectively prevent motor from being out of step. In particular, if a train of short-period pulses is suddenly output, the motor may not be able to handle the load and does not rotate. Speed-up and slow-down operation control is applied to avoid this problem. The speed-up and slow-down operation sequence is described below.

- The pulse period is gradually shortened until the specified number of pulses has been output (Speed up).
- The specified number of pulses with a fixed pulse period is output. (Constant speed).
- The pulse period is gradually extended until the specified number of pulses has been output (Slow down).

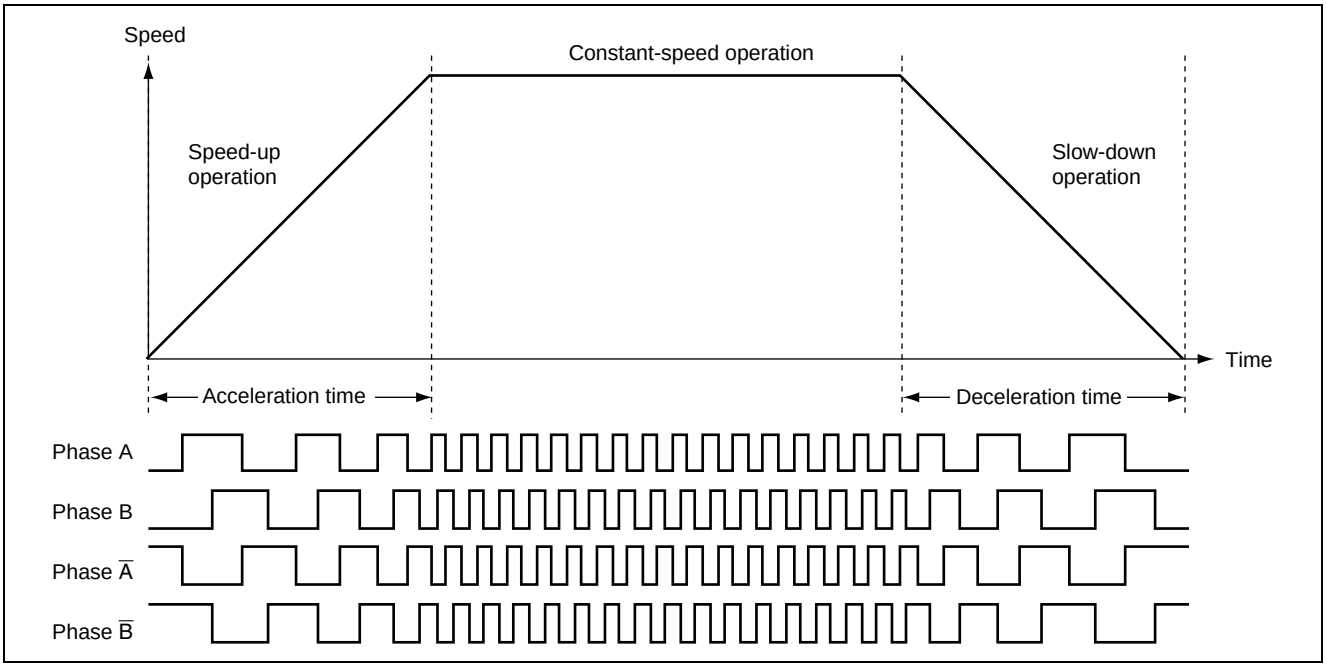


Figure 6 Speed-Up and Slow-Down Operation

4.4 Stepping Motor Control Flow

Figure 7 shows the flowchart of stepping motor control.

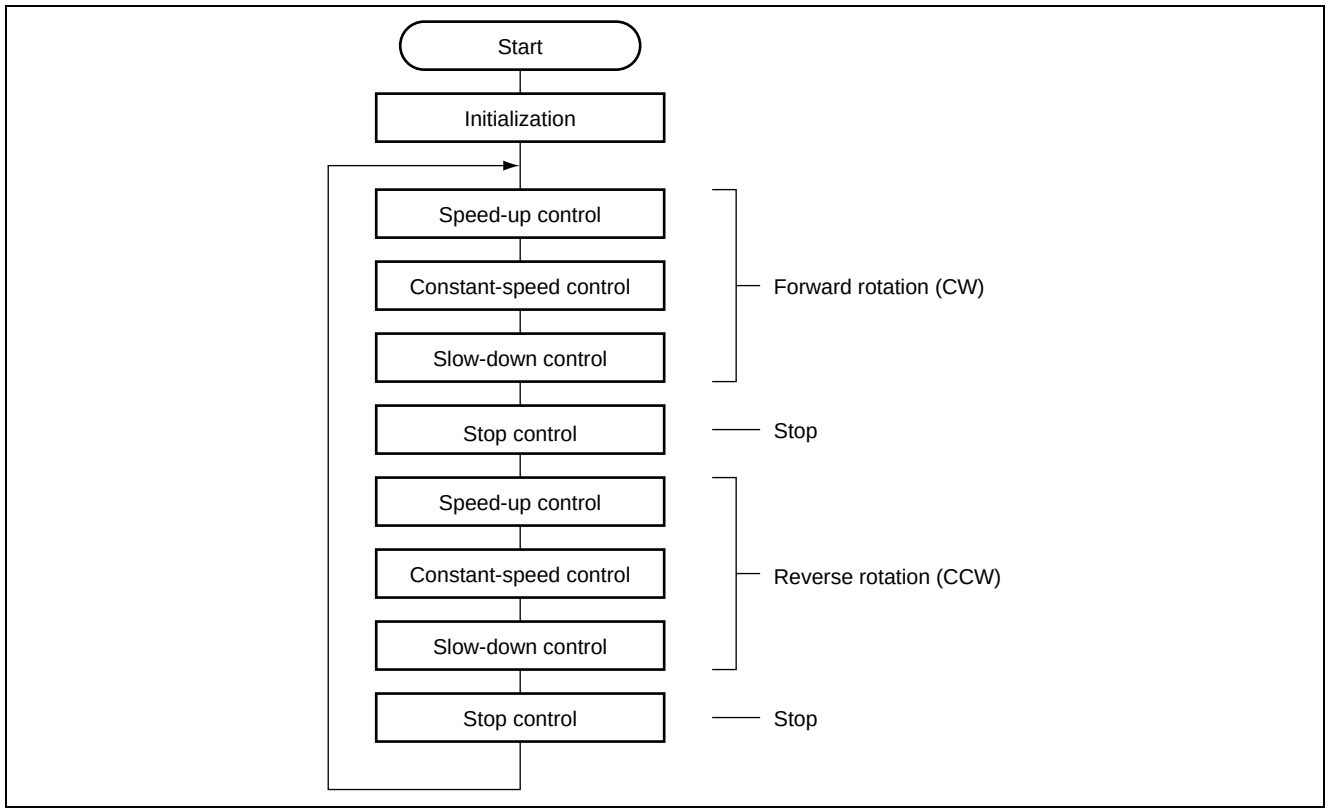


Figure 7 Flowchart of Stepping Motor Control

4.5 Example of Four-Phase Pulse Output

Figure 8 shows an example of four-phase pulse output.

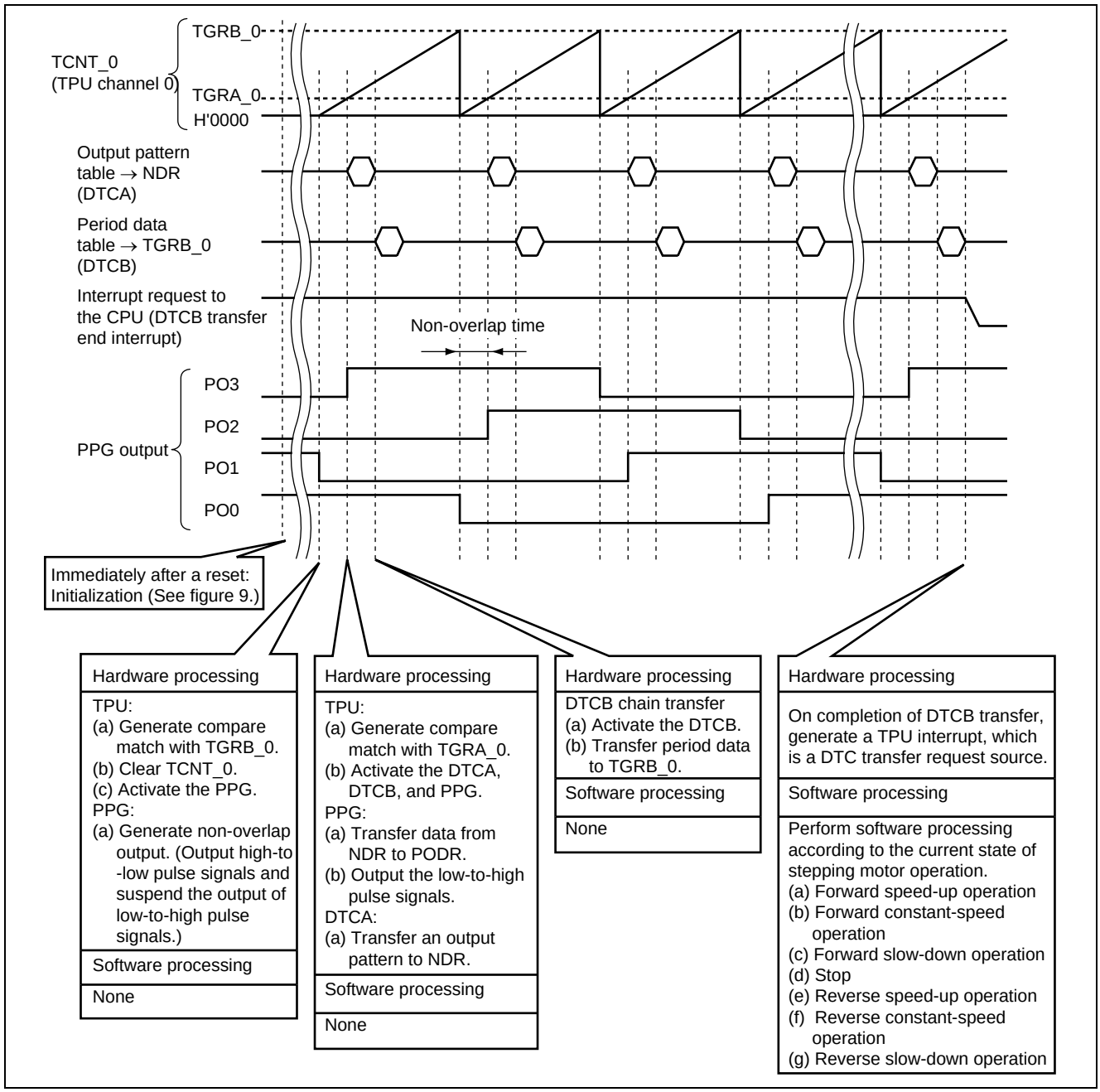


Figure 8 Timing of Stepping Motor Operation

Hardware processing
None
Software processing
PPG: • Set the first and second pulse output values. • Set up the P00 to P03 pins to function as output pins. • Set so that the output of pulse output group 0 is triggered by compare-match on TPU channel 0. • Select direct output and non-overlap operation for all pulse output groups. DTC: • Enable activation of DTC by TGI0A interrupt. • Set the DTC vector base register to H'FF8000. • PTN0 (Motor output pattern transfer information) - Increment SAR after transfer - DAR is fixed - Repeat mode - Byte-size transfer - Enable chain transfer - Transfer source is the repeat area - Transfer source address: start address of pattbl - Transfer destination address: address of NDRL_B - Number of transfers: 4 • CYC0 (Motor period data transfer information) - Increment SAR after transfer - DAR is fixed - Normal mode - Word-size transfer - Disable chain transfer - Transfer source address: start address of uptbl - Transfer destination address: address of TGRB_0 - Number of transfers: specified by "UPTIME" TPU: • Specify TGRA_0 and TGRB_0 as output compare registers. • Set non-overlap time. • Enable TGI0A interrupt requests. • Start counting by TCNT_0.

Figure 9 Initialization Processing Immediately After Reset

5. Description of Software

5.1 List of Functions

Table 4 lists the functions used in this sample task. Figure 10 shows the function hierarchy in this sample task.

Table 4 List of Functions

Function Name	Functions
init	Initialization routine: Cancels module stop mode, sets clocks, and calls main function.
main	Main routine: Initializes the TPU, PPG, and DTC and makes settings for forward speed-up operation.
tgi0a_int	TPU interrupt processing: Controls motor operation in each stage.
fslowup0	Called after completion of reverse stop operation and changes the DTC transfer modes for forward speed-up operation.
fconst0	Called after completion of forward speed-up operation and switches the DTC transfer modes for forward constant-speed operation.
fslowdwn0	Called after completion of forward constant-speed operation and changes the DTC transfer modes for forward slow-down operation.
rslowup0	Called after completion of forward stop operation and changes the DTC transfer modes for reverse speed-up operation.
rconst0	Called after completion of reverse speed-up operation and changes the DTC transfer modes for reverse constant-speed operation.
rslowdwn0	Called after completion of reverse constant-speed operation and changes the DTC transfer modes for reverse slow-down operation.
frstop0	Called after completion of reverse slow-down operation and changes the DTC transfer modes for stop operation.

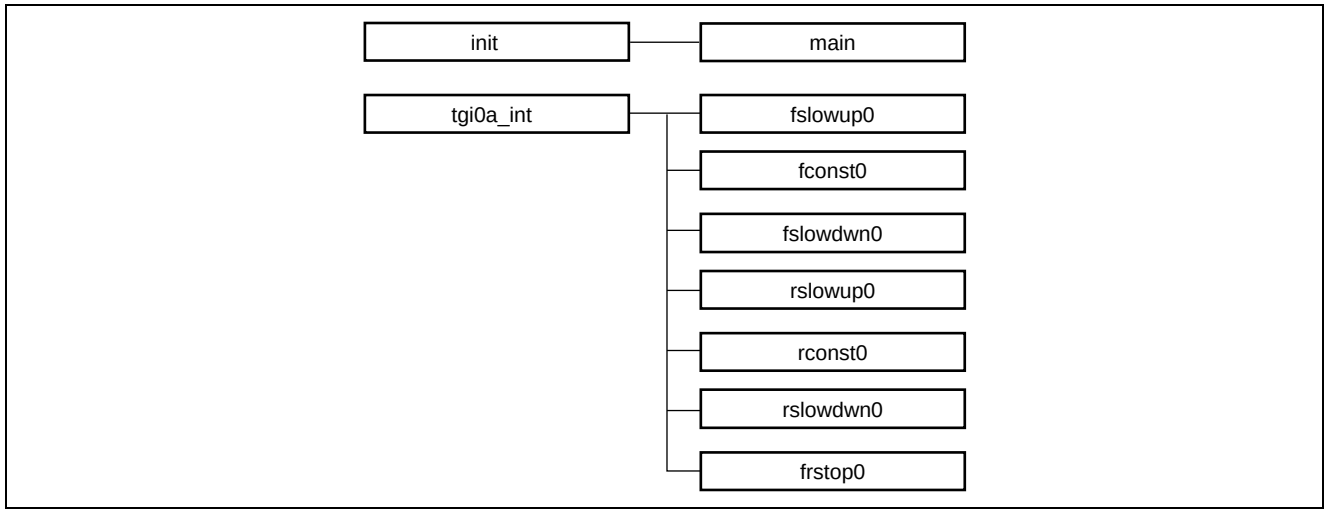


Figure 10 Hierarchy of Functions

5.2 Constants

Table 5 lists the constants used in this sample task.

Table 5 Description of Constants

Constant Name	Value	Description
UPTIME	49	Number of steps for speed-up and slow-down operations
CNSTTIME	481	Number of steps for constant-speed operation
STOPTIME	20	Number of steps for stop operation

5.3 Data Table Variables

- Output Pattern Table

  Data table of output patterns for stepping motor excitation.

```
pattbl[4] = {
    0xF6, .... Excites phase B̄ (PO0) and phase A (PO3)
    0xF3, .... Excites phase A (PO3) and phase B (PO2)
    0xF9, .... Excites phase B (PO2) and phase Ā (PO1)
    0xFC, .... Excites phase Ā (PO1) and phase B̄ (PO0)
};
```

- Period Data Table

```
uptbl[UPTIME] = {
     0xFFF0, 0xD000, 0x7000, 0x6F00, 0x6E00, 0x6D00, 0x6C00, 0x6B00, 0x6A00, 0x5900,
     0x5800, 0x5700, 0x5600, 0x5500, 0x5400, 0x5300, 0x5200, 0x5100, 0x5000, 0x4F00,
     0x4E00, 0x4D00, 0x4C00, 0x4B00, 0x4A00, 0x4900, 0x4800, 0x4700, 0x4600, 0x4500,
     0x4400, 0x4300, 0x4200, 0x4100, 0x4000, 0x3F00, 0x3E00, 0x3D00, 0x3C00, 0x3B00,
     0x3A00, 0x3900, 0x3800, 0x3700, 0x3600, 0x3500, 0x3400, 0x3200, 0x3000,
};
```

5.4 Internal Registers

The internal registers used in this sample task are described below.

- System Clock Control Register (SCKCR) Address: H'FFFDC4

Bit	Bit Name	Setting	Function
10	ICK2	0	System clock (Iϕ) select
9	ICK1	0	These bits selects the frequency of the system clock supplied to the CPU, DMAC, and DTC.
8	ICK0	1	001: Input clock × 2
6	PCK2	0	Peripheral module clock (Pϕ) select
5	PCK1	0	These bits selects the frequency of the peripheral module clock.
4	PCK0	1	001: Input clock × 2
2	BCK2	0	External bus clock (Bϕ) select
1	BCK1	0	These bits selects the frequency of the external bus clock.
0	BCK0	1	001: Input clock × 2

- Module Stop Control Register A (MSTPCRA) Address: H'FFFDC8

Bit	Bit Name	Setting	Function
15	ACSE	0	All-module-clock-stop mode enable Enables or disables all-module-clock-stop mode to reduce current consumption by also stopping the bus controller and I/O ports operations when the CPU executes a SLEEP instruction after module stop mode has been set for all the on-chip peripheral modules under control of MSTPCR. 0: Disables all-module-clock-stop mode. 1: Enables all-module-clock-stop mode.
13	MSTPA13	0	DMA controller (DMAC) 0: Cancels module stop mode. 1: Sets module stop mode.
12	MSTPA12	0	Data transfer controller (DTC) 0: Cancels module stop mode. 1: Sets module stop mode.
9	MSTPA9	0	8-bit timers (TMR3, TMR2) 0: Cancels module stop mode. 1: Sets module stop mode.
8	MSTPA8	0	8-bit timers (TMR1, TMR0) 0: Cancels module stop mode. 1: Sets module stop mode.
5	MSTPA5	0	D/A converter (channels 1, 0) 0: Cancels module stop mode. 1: Sets module stop mode.
3	MSTPA3	0	A/D converter (unit 0) 0: Cancels module stop mode. 1: Sets module stop mode.
0	MSTPA0	0	16-bit timer pulse unit (TPU channels 5 to 0) 0: Cancels module stop mode. 1: Sets module stop mode.

- Module Stop Control Register B (MSTPCRB) Address: H'FFFDCA

Bit	Bit Name	Setting	Function
15	MSTPB15	0	Programmable pulse generator (PPG) 0: Cancels module stop mode. 1: Sets module stop mode.
12	MSTPB12	0	Serial communication interface 4 (SCI_4) 0: Cancels module stop mode. 1: Sets module stop mode.
10	MSTPB10	0	Serial communication interface 2 (SCI_2) 0: Cancels module stop mode. 1: Sets module stop mode.
9	MSTPB9	0	Serial communication interface 1 (SCI_1) 0: Cancels module stop mode. 1: Sets module stop mode.
8	MSTPB8	0	Serial communication interface 0 (SCI_0) 0: Cancels module stop mode. 1: Sets module stop mode.

- Module Stop Control Register C (MSTPCRC) Address: H'FFFDCC

Bit	Bit Name	Setting	Function
2	MSTPC2	0	On-chip RAM 2 (H'FFF6000 to H'FFF7FFF) 0: Cancels module stop mode. 1: Sets module stop mode.
1	MSTPC1	0	On-chip RAM 1 (H'FFF8000 to H'FFF9FFF) 0: Cancels module stop mode. 1: Sets module stop mode.
0	MSTPC0	0	On-chip RAM 0 (H'FFFA000 to H'FFFBFFF) 0: Cancels module stop mode. 1: Sets module stop mode.

- DTC Vector Base Register (DTCVBR) Address: H'FFFD80
  - Function: 32-bit register that specifies the base address used in vector table address calculation
  - Setting: H'FF8000

- DTC Control Register (DTCCR) Address: H'FFFF30

Bit	Bit Name	Setting	Function
4	RRS	0	DTC transfer information read skip enable 0: Transfer information read skip is not performed. 1: Transfer information read skip is performed when the vector numbers match.
3	RCHNE	0	Chain transfer enable after DTC repeat transfer 0: Disables the chain transfer after repeat transfer. 1: Enables the chain transfer after repeat transfer.
0	ERR	0	Transfer stop flag 0: Address error nor NMI interrupt request has not occurred. 1: Address error or NMI interrupt request has occurred.

- DTC Enable Register B (DTCERB) Address: H'FFFF22

Bit	Bit Name	Setting	Function
13	DTCEB13	1	DTC activation enable 13 0: Disables DTC activation by TGI0A interrupts of the TPU_0. 1: Enables DTC activation by TGI0A interrupts of the TPU_0.

- PPG Output Control Register (PCR) Address: H'FFFF76

Bit	Bit Name	Setting	Function
1	G0CMS1	0	Group 0 compare match select 1, 0
0	G0CMS0	0	00: Output of pulse output group 0 is triggered by compare-match on TPU channel 0.

- PPG Output Mode Register (PMR) Address: H'FFFF77

Bit	Bit Name	Setting	Function
4	G0INV	1	Group 0 inversion 0: Inverted output 1: Direct output
0	G0NOV	1	Group 0 non-overlap 0: Normal operation 1: Non-overlap operation

- Next Data Enable Register L (NDERL) Address: H'FFFF79

Bit	Bit Name	Setting	Function
7	NDER7	0	Next data enable 7 to 0
6	NDER6	0	When a bit in this register is set to 1, data of the corresponding bit in NDRL is transferred to PODRL, triggered by the selected output trigger. Data transfer from NDRL to PODRL does not take place for the bits whose corresponding bits in this register are clear.
5	NDER5	0	
4	NDER4	0	
3	NDER3	1	
2	NDER2	1	
1	NDER1	1	
0	NDER0	1	

- Output Data Register L (PODRL) Address: H'FFFF7B

Bit	Bit Name	Setting	Function
7	POD7	0	Output data register 7 to 0
6	POD6	0	For the bits set to generate pulse outputs by NDERL, the values of the corresponding bits in NDRL are transferred to this register by the output trigger during PPG operation. While a bit in NDERL is set to 1, the CPU cannot write to the corresponding bit of this register. While a bit in NDERL is clear, the initial pulse output value can be set in the corresponding bit of this register.
5	POD5	0	
4	POD4	0	
3	POD3	1	
2	POD2	1	
1	POD1	0	
0	POD0	0	

- Next Data Register L (NDRL) Address: H'FFFF7F

Bit	Bit Name	Setting	Function
3	NDER3	1	Next data 3 to 0
2	NDER2	1	The contents of this register are transferred to the corresponding bits in the PODRL by the output trigger specified by PCR.
1	NDER1	0	
0	NDER0	0	

- Timer Start Register (TSTR) Address: H'FFFFBC

Bit	Bit Name	Setting	Function
0	CST0	1	Counter start 0 0: Stops counting by TCNT_0 of the TPU. 1: Starts counting by TCNT_0 of the TPU.

- Timer Control Register_0 (TCR_0) Address: H'FFFFC0

Bit	Bit Name	Setting	Function
7	CCLR2	0	Counter clear 2 to 0
6	CCLR1	1	010: Clear TCNT_0 on compare match or input capture by TGRB_0.
5	CCLR0	0	
4	CKEG1	0	Clock edge 1, 0
3	CKEG0	0	00: The counter counts the falling edges when an internal clock is input, or counts the rising edges when an external clock is input.
2	TPSC2	0	Timer prescaler 2 to 0
1	TPSC1	1	010: The counter clock source is the internal clock Pϕ/16.
0	TPSC0	0	

- Timer I/O Control Register H_0 (TIORH_0) Address: H'FFFFC2

Bit	Bit Name	Setting	Function
7	IOB3	0	I/O control B3 to B0
6	IOB2	0	0000: TGRB_0 operates as an output compare register and the
5	IOB1	0	TIOCB0 pin output is disabled.
4	IOB0	0	
3	IOA3	0	I/O control A3 to A0
2	IOA2	0	0000: TGRA_0 operates as an output compare register and the
1	IOA1	0	TIOCA0 pin output is disabled.
0	IOA0	0	

- Timer Interrupt Enable Register_0 (TIER_0) Address: H'FFFFC4

Bit	Bit Name	Setting	Function
0	TGIEA	1	TGR interrupt enable A 0: Disables interrupt request (TGIA) generation by the TGFA bit. 1: Enables interrupt request (TGIA) generation by the TGFA bit.

- Timer Status Register_0 (TSR_0) Address: H'FFFFC5

Bit	Bit Name	Setting	Function
1	TGFB	0	Input capture/output compare flag B Indicates the occurrence of TGRB input capture or compare match. 0: Input capture or compare match has not occurred. 1: Input capture or compare match has occurred.
0	TGFA	0	Input capture/output compare flag A Indicates the occurrence of TGRA input capture or compare match. 0: Input capture or compare match has not occurred. 1: Input capture or compare match has occurred.

- Timer Counter_0 (TCNT_0) Address: H'FFFFC6
  - Function: A 16-bit readable/writable register that is incremented according to the setting of TCR_0.
  - Setting value: H'0065

- Timer General Register A_0 (TGRA_0) Address: H'FFFFC8
  - Function: A 16-bit register that is compared with the counter in output compare operation.
  - Setting value: H'0064
- Timer General Register B_0 (TGRB_0) Address: H'FFFFCA
  - Function: A 16-bit register that is compared with the counter in output compare operation.
  - Setting value: H'FF00

5.5 DTC Transfer Information Settings

5.5.1 PTN0

PTN0 is the motor output pattern transfer information. The addresses given below are those of the RAM area to which PTN0 is allocated.

- DTC Mode Register A (MRA) Address: H'FF6000

Bit	Bit Name	Setting	Function
7	MD1	0	DTC mode 1, 0
6	MD0	1	00: Normal mode 01: Repeat mode
5	Sz1	0	DTC data transfer size 1, 0
4	Sz0	0	00: Byte-size transfer 01: Word-size transfer
3	SM1	1	Source address mode 1, 0
2	SM0	0	0X: SAR is fixed. 10: SAR is incremented after transfer. 11: SAR is decremented after transfer.

Note: X = Don't care

- DTC Mode Register B (MRB) Address: H'FF6004

Bit	Bit Name	Setting	Function
7	CHNE	1	DTC chain transfer enable 0: Disables chain transfer. 1: Enables chain transfer.
6	CHNS	0	DTC chain transfer select 0: Chain transfer every time. 1: Chain transfer only when transfer counter value = 0.
4	DTS	1	DTC transfer mode select 0: Specifies the destination as repeat or block area. 1: Specifies the source as repeat or block area.
3	DM1	0	Destination address mode 1, 0
2	DM0	0	0X: DAR is fixed.

Note: X = Don't care

- DTC Source Address Register (SAR) Address: H'FF6000
  - Function: A 32-bit register that specifies the source address of data to be transferred by the DTC. The lower 24 bits are valid in short address mode.
  - Setting value: pattbl
- DTC Destination Address Register (DAR) Address: H'FF6004
  - Function: A 32-bit register that specifies the destination address to which data is transferred by the DTC. The lower 24 bits are valid in short address mode.
  - Setting value: &NDRL_B
- DTC Transfer Count Register A (CRA) Address: H'FF6008
  - Function: A 16-bit register that specifies the number of DTC data transfers.
  - Setting value: H'0404

5.5.2 CYC0

CYC0 is the motor period data transfer information. The addresses given below are those of the RAM area to which CYC0 is allocated.

- DTC Mode Register A (MRA) Address: H'FF600C

Bit	Bit Name	Setting	Function
7	MD1	0	DTC mode 1, 0
6	MD0	0	00: Normal mode 01: Repeat mode
5	Sz1	0	DTC data transfer size 1, 0
4	Sz0	1	00: Byte-size transfer 01: Word-size transfer
3	SM1	1	Source address mode 1, 0
2	SM0	0	0X: SAR is fixed. 10: SAR is incremented after transfer. 11: SAR is decremented after transfer.

Note: X = Don't care

- DTC Mode Register B (MRB) Address: H'FF6010

Bit	Bit Name	Setting	Function
7	CHNE	0	DTC chain transfer enable 0: Disables chain transfer. 1: Enables chain transfer.
6	CHNS	0	DTC chain transfer select 0: Chain transfer every time. 1: Chain transfer only when transfer counter value = 0.
4	DTS	0	DTC transfer mode select 0: Specifies the destination as repeat or block area. 1: Specifies the source as repeat or block area.
3	DM1	0	Destination address mode 1, 0
2	DM0	0	0X: DAR is fixed.

Note: X = Don't care

- DTC Source Address Register (SAR) Address: H'FF600C
  - Function: A 32-bit register that specifies the source address of data to be transferred by the DTC. The lower 24 bits are valid in short address mode.
  - Setting value: uptbl
- DTC Destination Address Register (DAR) Address: H'FF6010
  - Function: A 32-bit register that specifies the destination address to which data is transferred by the DTC. The lower 24 bits are valid in short address mode.
  - Setting value: &TGRB_0
- DTC Transfer Count Register A (CRA) Address: H'FF6014
  - Function: A 16-bit register that specifies the number of DTC data transfers.
  - Setting value: UPTIME

5.6 RAM Usage

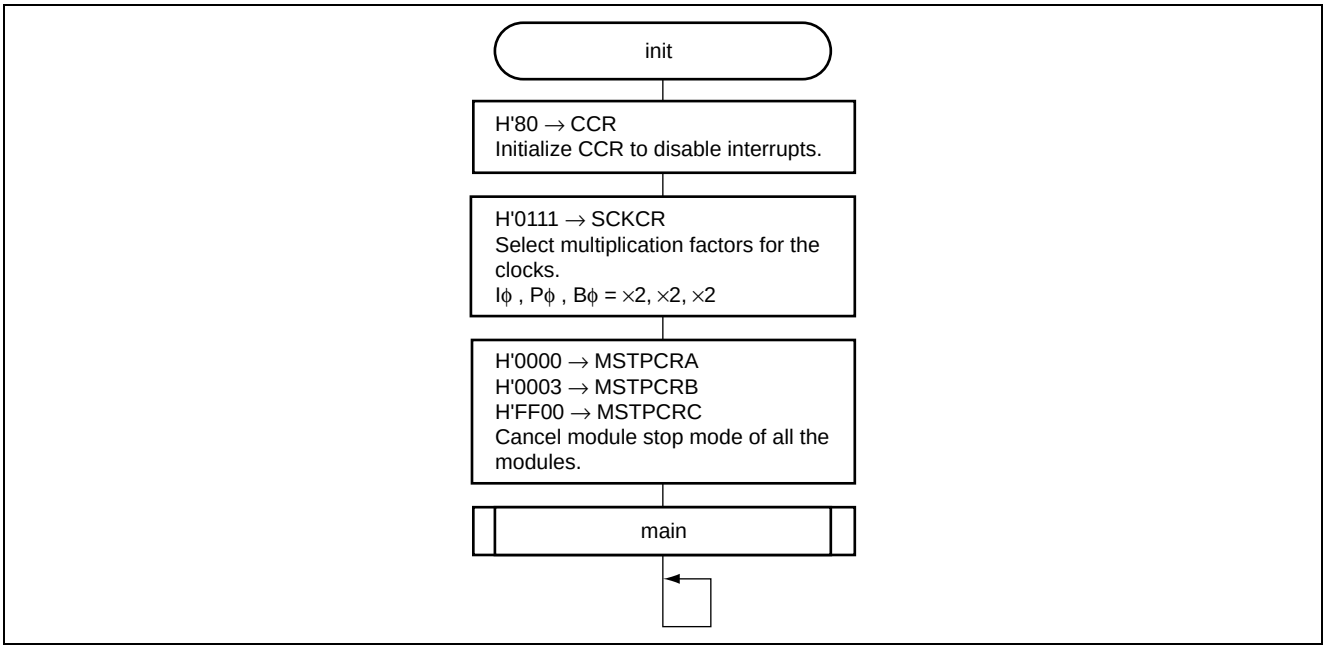
Table 6 describes the RAM usage in this sample task.

Table 6 Description of RAM

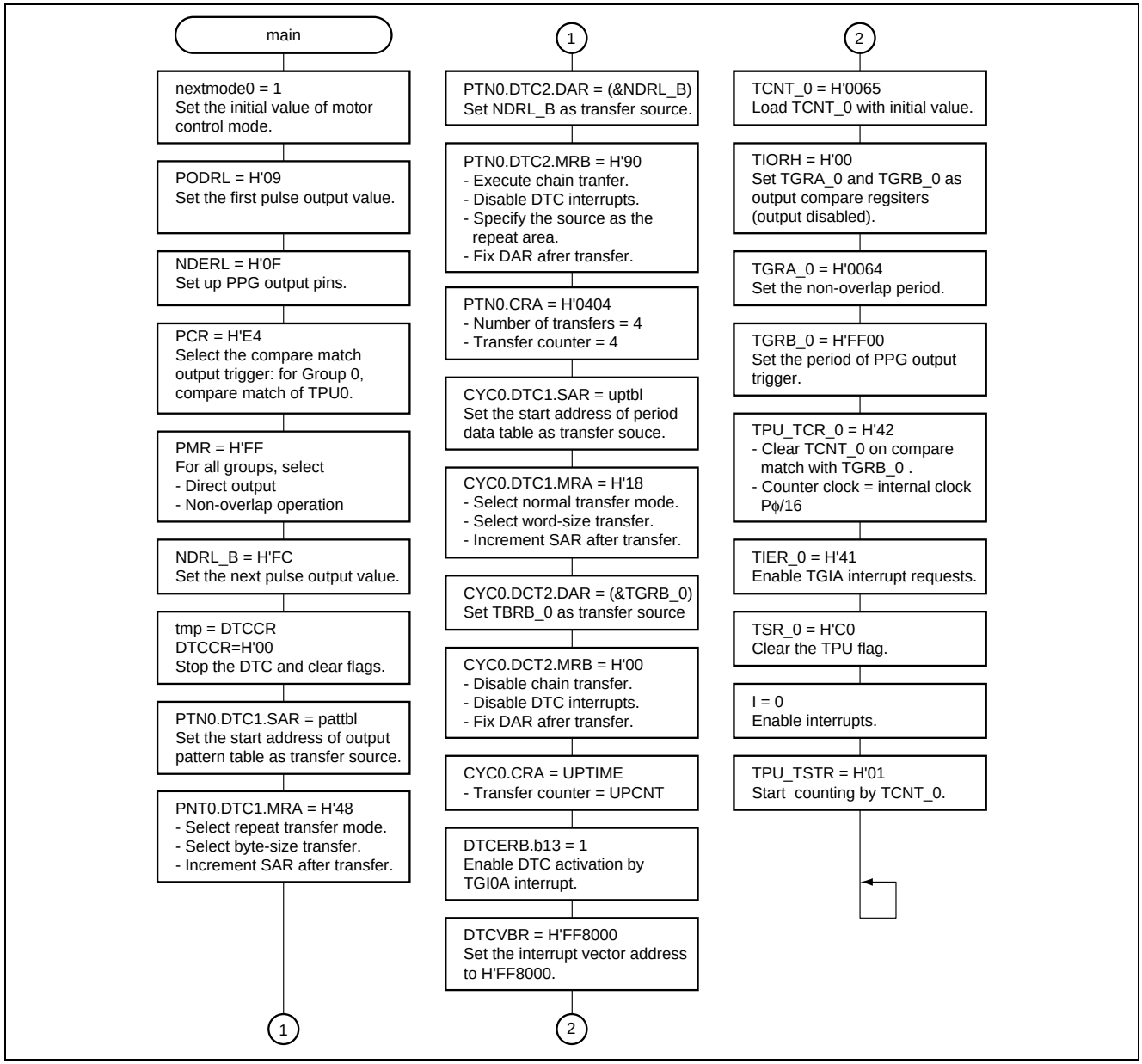
Type	Variable Name	Description
DTC_tag	PTN0	Output pattern transfer information for the motor
DTC_tag	CYC0	Period data transfer information for the motor
unsigned char	nextmode0	Sets stepping motor operating mode. 0: Forward speed-up control 1: Forward constant-speed control 2: Forward slow-down control 3: Stop control 4: Reverse speed-up control 5: Reverse constant-speed control 6: Reverse slow-down control 7: Stop control

6. Flowchart

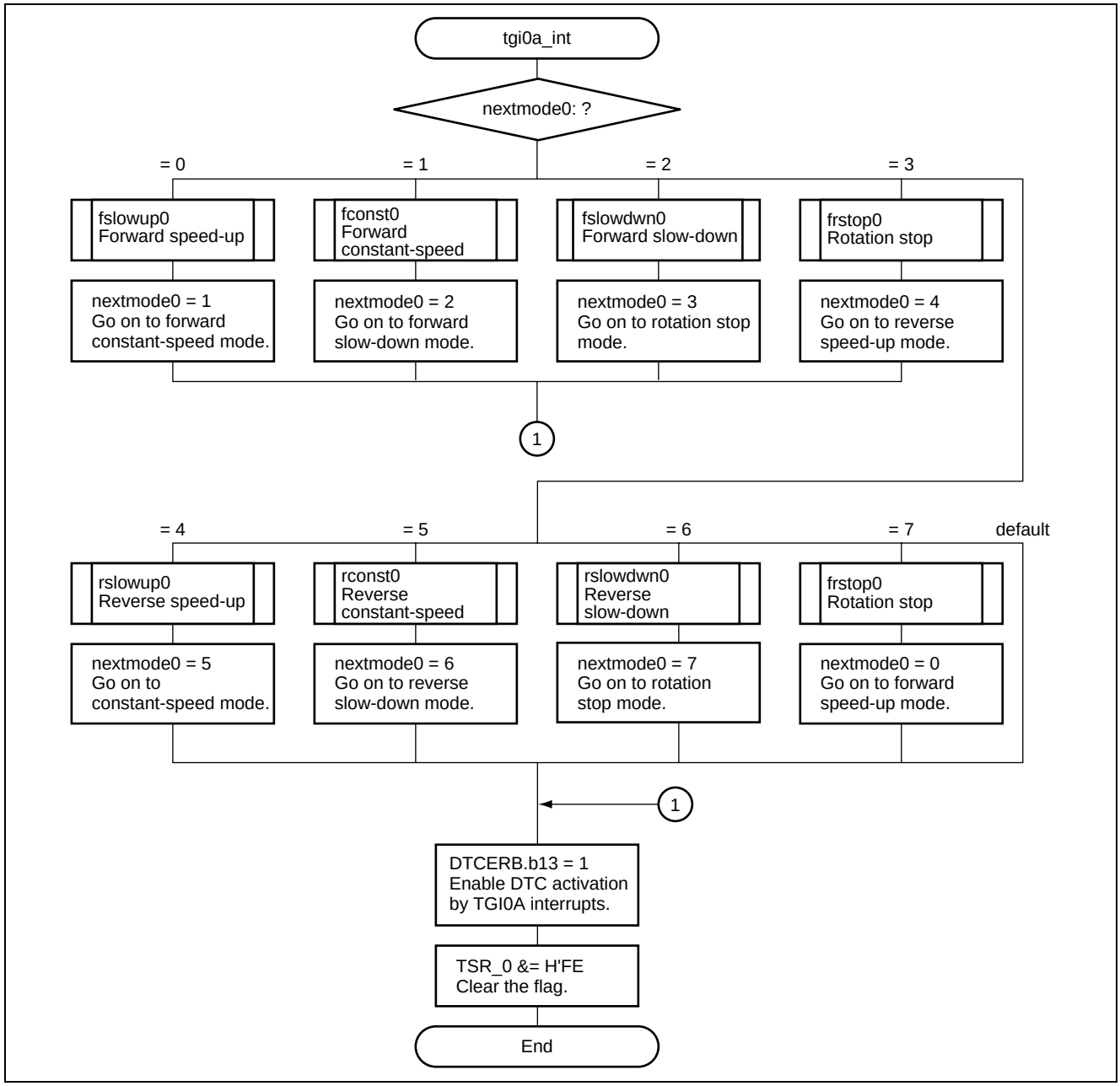
6.1 init Function



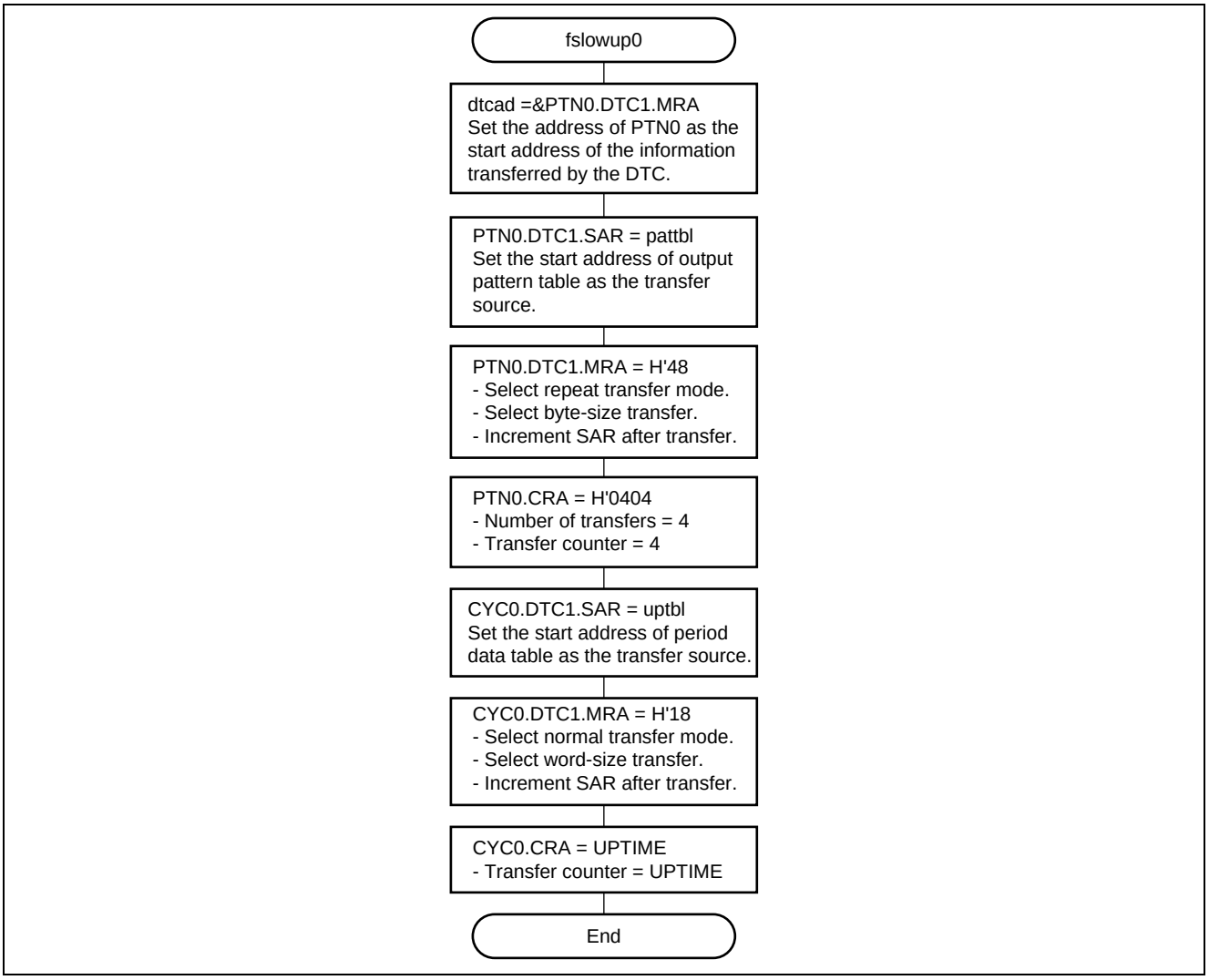
6.2 Main Function



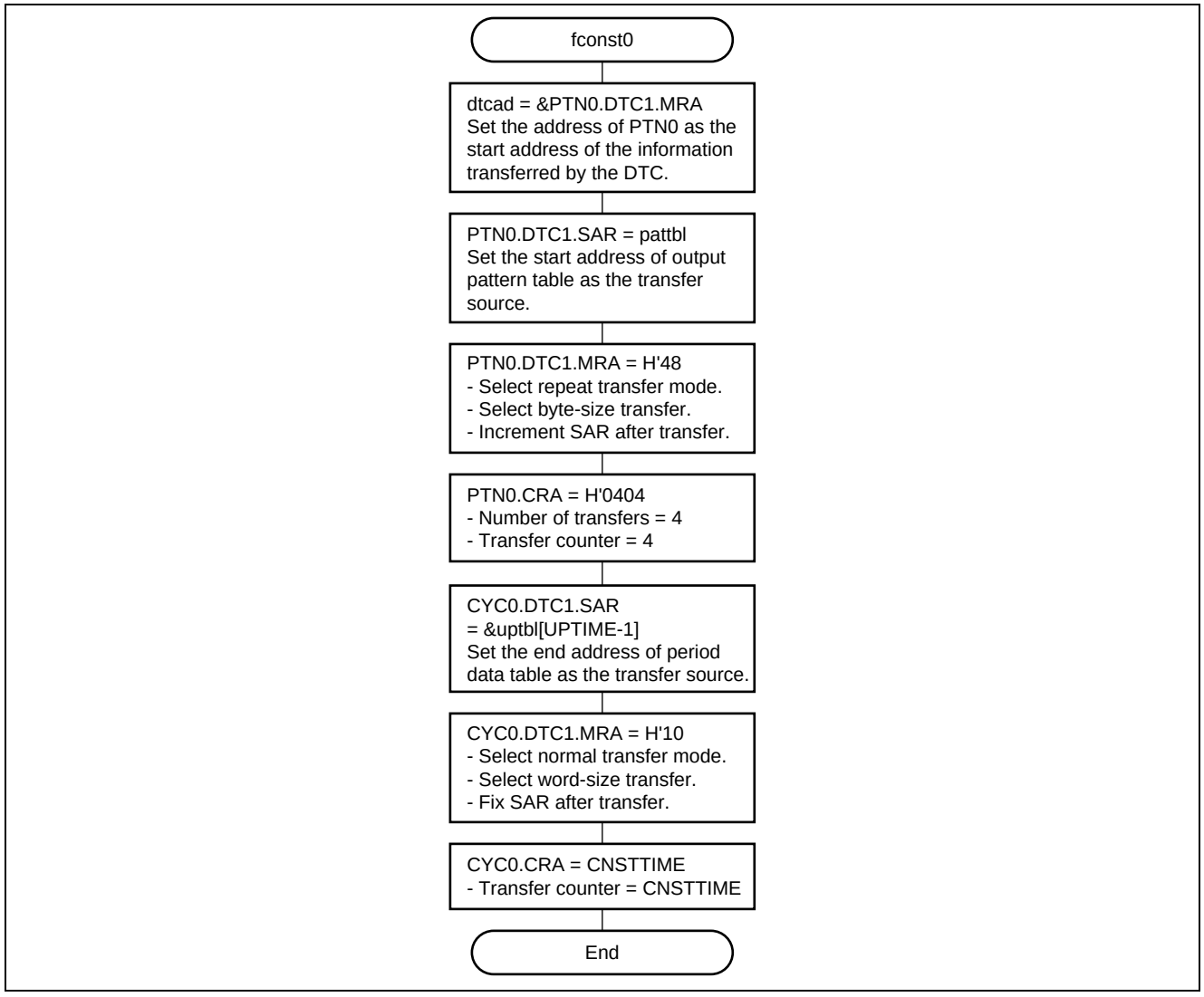
6.3 tgi0a_int Function



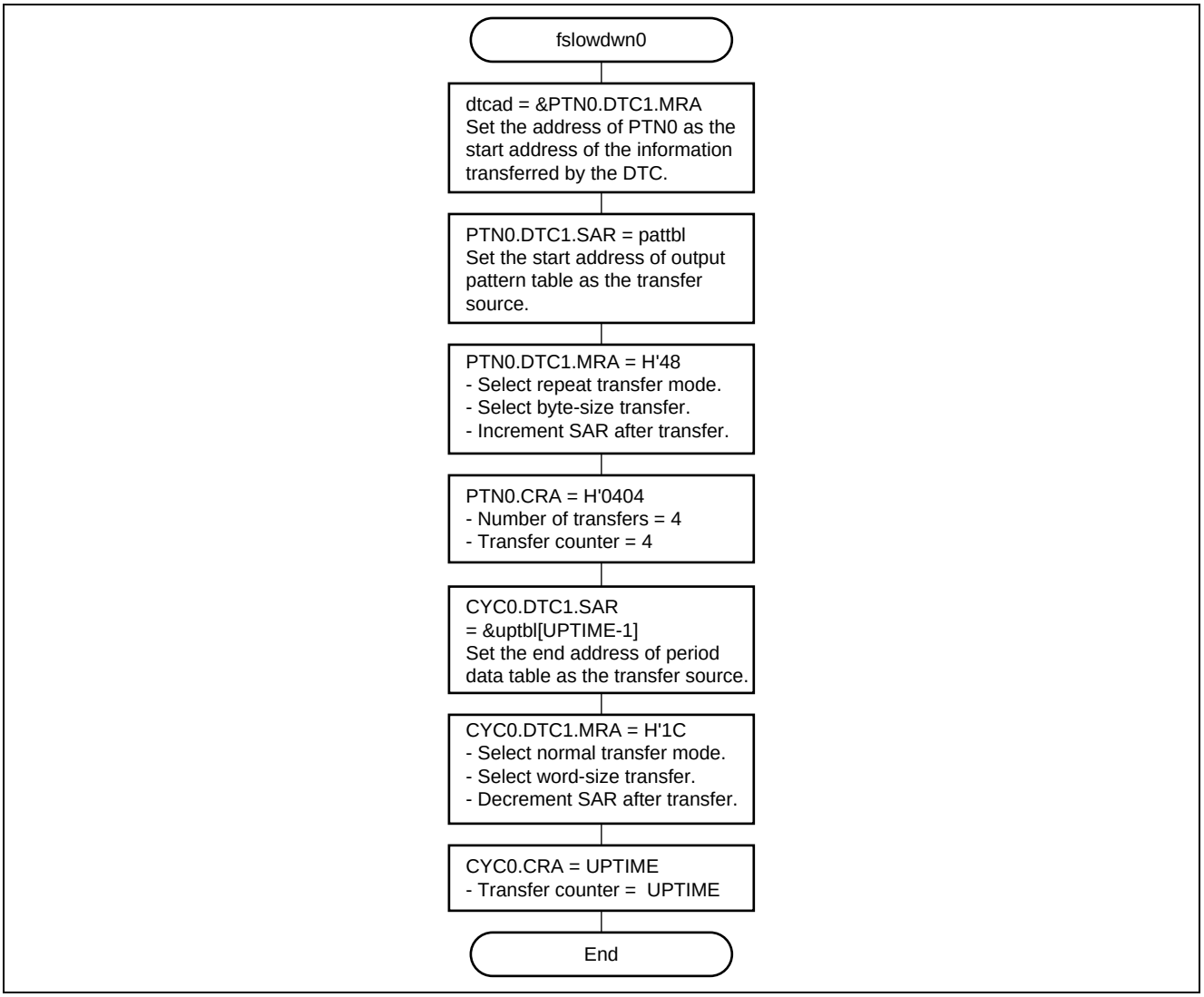
6.4 fslowup0 Function



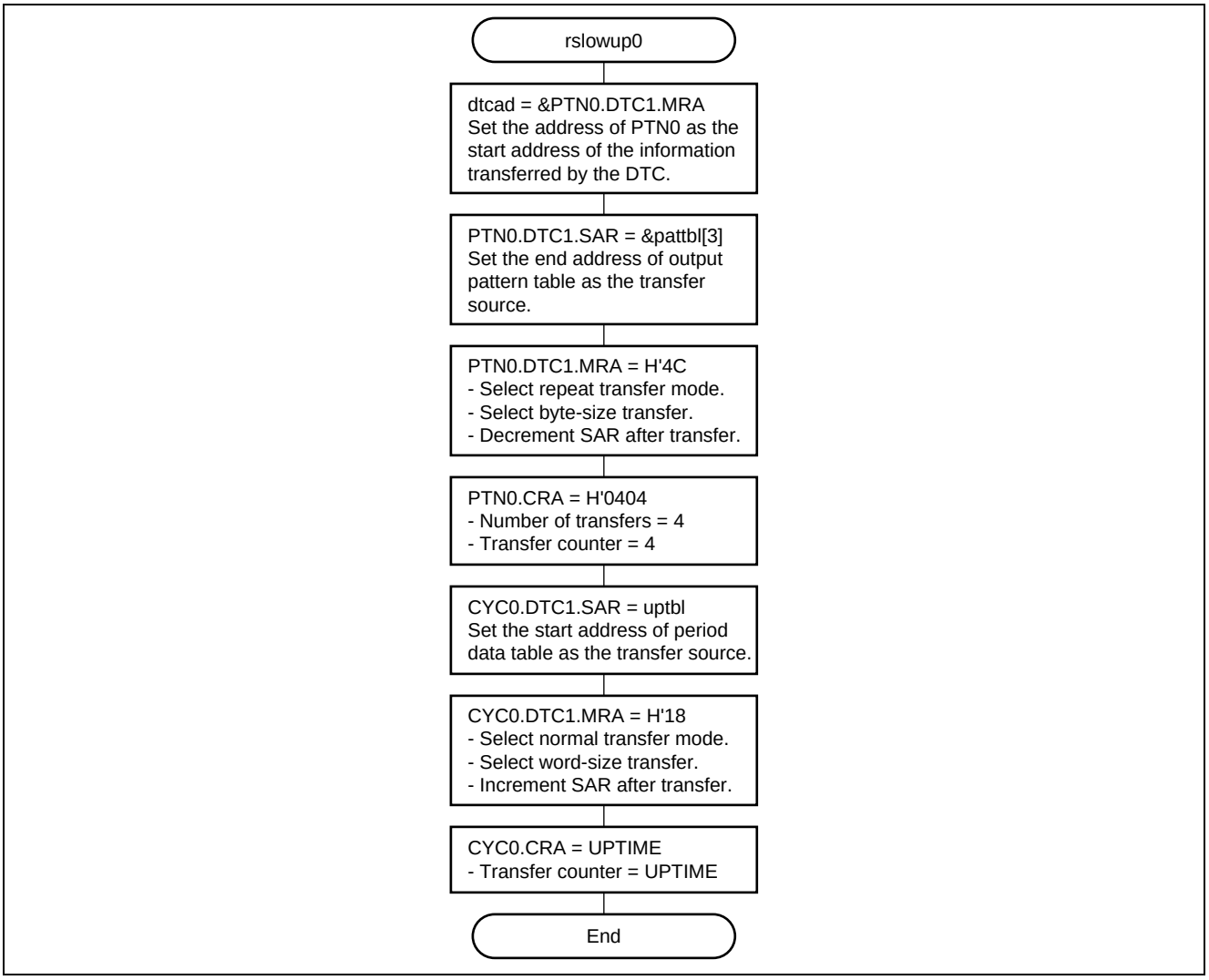
6.5 fconst0 Function



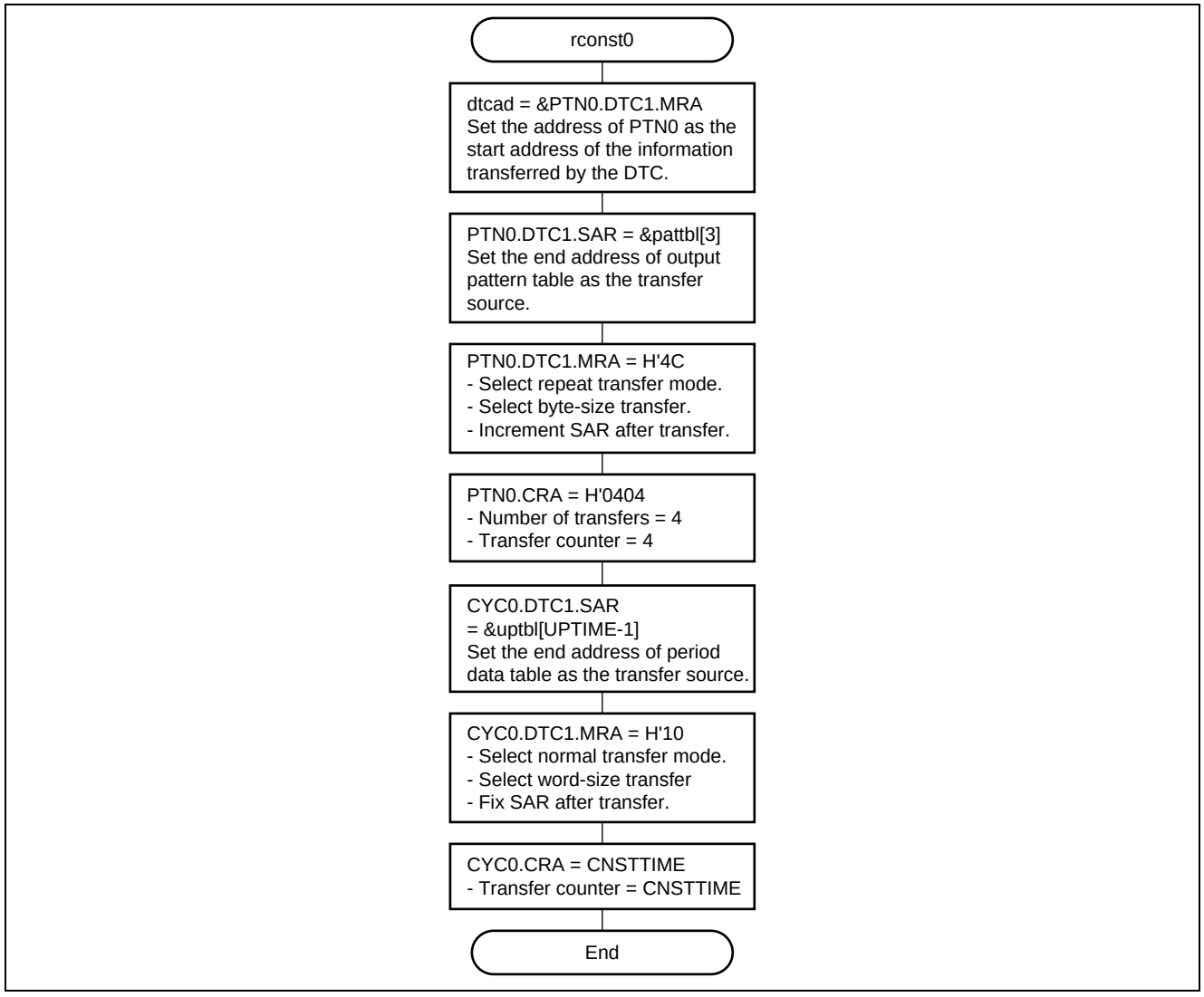
6.6 fslowdwn0 Function



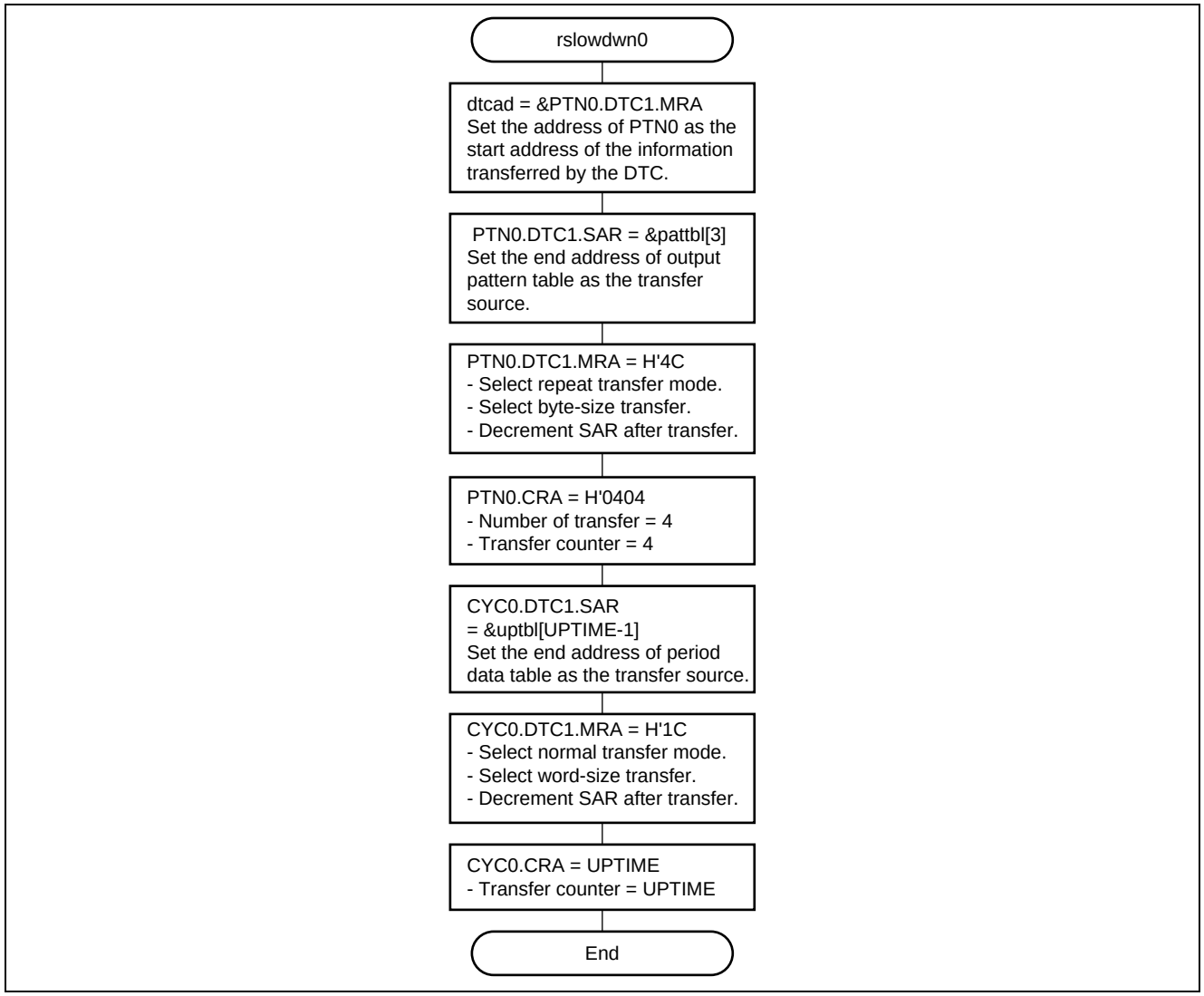
6.7 rslowup0 Function



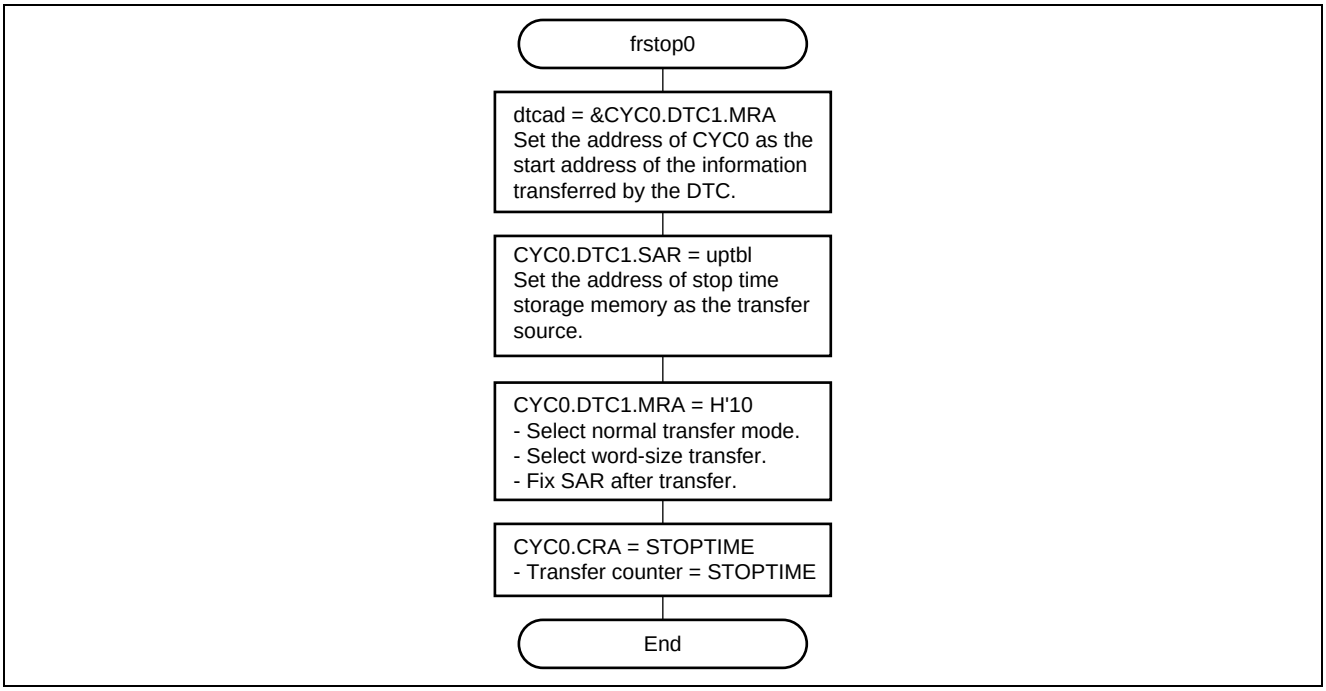
6.8 rconst0 Function



6.9 rslowdwn0 Function



6.10 frstop0 Function



Revision Record

Rev.	Date	Description	
		Page	Summary
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