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H8SX Family

RTE/L Return from Exception Handling with Data Restoration

Introduction

Shows an example of C compiler use of the RTE/L instruction.

Contents

1. Specifications

- The H8SX family microcomputer RTE/L instruction performs the following processing.
  - Restores the saved data from the stack to the registers specified by the register list.
  - Restores EXR, CCR, and PC from the stack.
  - Performs processing from the address indicated by the restored PC.
- In this sample task, NMI interrupt processing is performed, and the assembly language code generated by the C compiler is shown.

2. Functions Used

This sample task shows an example of use of the RTE/L instruction by the C compiler.

3. Principles of Operation

Table 1 shows an example of the assembly language code generated by the C compiler when a subroutine is called.

Table 1 RTE/L Code

Sample C Program	Sample Assembly Language Code Generated by the C compiler

`void main(void)`
`{`
`  .`
`  .`
`  while ()  /* Waiting for interrupt */`
`  .`
`}`
 	
`void sub_int (void)`
`{`
`  .`
`  .`
`  .`
`}  /* End of interrupt routine */`
	`_main:`
	`  .`
	`  .`
	`WT01:`
	`  BRA  WT01  ; Waiting for interrupt`
	
	`_sub_int:`
	`  STM.L  (ER0-ER3),@-SP  ; Save ER3 to stack`
	`  .`
	`  .`
	`  .`
	`  RTE/L  (ER0-ER3)  ; End of interrupt routine`
	`  ; Restore ER3`

4. Development Environment

4.1 Development Support Tool Versions

The development support tools of this sample task is shown in table 2.

Table 2 Development Support Tool Versions

Software Name	Version Used
CH38.EXE	C compiler (H8S, H8/300 series C/C++ compiler) Ver. 6.0.00.005
ASM38.EXE	Assembler (H8S, H8/300 series cross assembler) Ver. 6.0.01.005
OPTLNK.EXE	Linkage editor (optimizing linkage editor) Ver. 8.0.00.020
LBG38.EXE	Library configuration tool (H8S, H8/300 series C/C++ standard library generator) Ver. 2.0.00.000

4.2 C compiler Option Settings

C compiler option settings for this sample task are shown in table 3.

Table 3 C compiler Option Settings

Option	Set Value
CPu	H8SXA:24:MD
Code	Machinecode
OPtimize	1
REGParam	3
SPeed	Register, SHift, STruct, Expression

5. Description of Software

5.1 Modules

Modules used by this sample task are shown in table 4.

Table 4 Modules

Module Name	Function
main	Main routine Waits for the NMI interrupt.
nmi_int	RTE/L test program Writes data to RAM as dummy processing in the NMI interrupt routine.

5.2 Arguments

No arguments are used by this sample task.

5.3 Internal Registers Used

- INTCR Interrupt control register Address: H'0FFFFF32

Bit	Bit Name	Set Value	Function
3	NMIEG	0	NMI edge select 0: Interrupt request generated at falling edge of NMI input 1: Interrupt request generated at rising edge of NMI input

5.4 RAM Usage

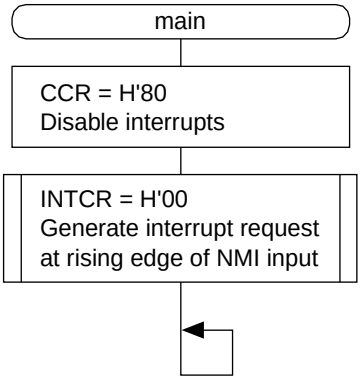
Table 5 describes RAM usage in this sample task.

Table 5 RAM Usage

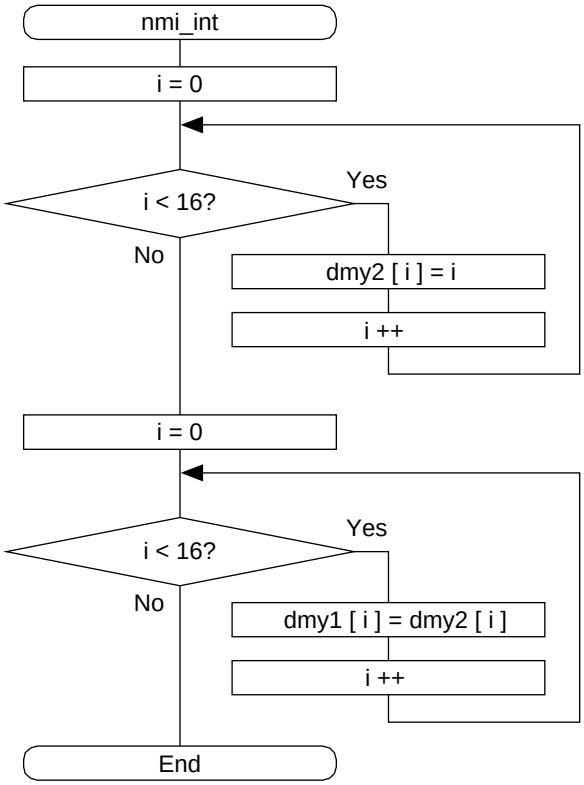
Label	Size	Function
dmy1[16]	16 × 4 bytes	For dummy processing

6. Flowcharts

6.1 Main Routine



6.2 RTE/L Test Program



6.3 Link Address Specifications

Section Name	Address
CV1	H'000000
CV2	H'00001C
P	H'001000
B	H'FEC000

7. Program Listing

7.1 C Program

```
/************************************************************/
/*                                                          */
/*  H8SX Family                                             */
/*  Application Note                                        */
/*                                                          */
/*  'RTE/L Test program'                                    */
/*                                                          */
/*  Function                                                */
/*  : RTE/L                                                 */
/*                                                          */
/*                                                          */
/*                                                          */
/*                                                          */
/************************************************************/

#include    <machine.h>

/************************************************************/
/*  Symbol Definition                                       */
/************************************************************/
#define INTCR       *(volatile unsigned char  *)0xFFFF32  /* Interrupt control
register       */

#pragma interrupt ( nmi_int )
/************************************************************/
/*  Function define                                         */
/************************************************************/
void main ( void );
void nmi_int ( void );

/************************************************************/
/*  RAM define                                              */
/************************************************************/
unsigned long dmy1[16];

/************************************************************/
/*  Vector Address                                          */
/************************************************************/
#pragma section     V1                      /* VECTOR SECTOIN SET              */
void (*const VEC_TBL1[])(void) = {
    main                                    /* 00 Reset                        */
};

#pragma section     V2                      /* VECTOR SECTOIN SET              */
void (*const VEC_TBL2[])(void) = {
    nmi_int
};

#pragma entry main(sp=0xFFC000)
#pragma section                             /* P                               */
```

```
/*********************************************************/
/*  Main Program                                         */
/*********************************************************/
void main ( void )
{
    set_ccr(0x80);                      /* Initialize CCR/Interrupt Disable */

    INTCR = 0x00;                       /* Interrupt request generated      */
                                        /*     at falling edge of NMI input */
    while(1);
}

/*********************************************************/
/*  RTE/L Test Program (NMI Interrupt)                   */
/*********************************************************/
void nmi_int ( void )
{
    unsigned char i;
    unsigned long dmy2[16];

    for ( i=0; i<16; i++)
        dmy2[i] = i;

    for ( i=0; i<16; i++)
        dmy1[i] = dmy2[i];
}
```

7.2 Assembly Language Code Generated by the C compiler

```
P                                                                   ; section
                          ;*** File main.c    , Line 53
  00000000                _main:                                    ; function: main
  00000000 7A0700FFC000       MOV.L       #16760832,SP
  00000006 F880               MOV.B       #128:8,R0L
  00000008 0308               LDC.B       R0L,CCR
  0000000A 6AF00FFFFF32       MOV.B       #0:4,@268435250:32
  00000010                L36:
  00000010 4000               BRA         L36:8


                          ;*** File main.c    , Line 65
  00000012                _nmi_int:                                 ; function: nmi_int
  00000012 01306DF0           STM.L       (ER0-ER3),@-SP
  00000016 7A3F0040           SUB.L       #64:16,SP
  0000001A 18AA               SUB.B       R2L,R2L
  0000001C                L39:
  0000001C 0CAB               MOV.B       R2L,R3L
  0000001E 1763               EXTU.L      #2,ER3
  00000020 0CA9               MOV.B       R2L,R1L
  00000022 01CC5041           MULXU.B     #4:4,R1
  00000026 0D10               MOV.W       R1,R0
  00000028 1770               EXTU.L      ER0
  0000002A 0AF0               ADD.L       SP,ER0
  0000002C 01006983           MOV.L       ER3,@ER0
  00000030 0A0A               INC.B       R2L
  00000032 AA10               CMP.B       #16:8,R2L
  00000034 4500               BLO         L39:8
  00000036 18AA               SUB.B       R2L,R2L
  00000038                L41:
  00000038 0CA9               MOV.B       R2L,R1L
  0000003A 01CC5041           MULXU.B     #4:4,R1
  0000003E 0D10               MOV.W       R1,R0
  00000040 1770               EXTU.L      ER0
  00000042 0AF0               ADD.L       SP,ER0
  00000044 010800DA00000000   MOV.L       @ER0,@(_dmy1:32,R2L.B)
  0000004C 0A0A               INC.B       R2L
  0000004E AA10               CMP.B       #16:8,R2L
  00000050 4500               BLO         L41:8
  00000052 7A1F0040           ADD.L       #64:16,SP
  00000056 5633               RTE/L       (ER0-ER3)
B                                                                   ; section
  00000000                _dmy1:                                    ; static: dmy1
  00000000 00000040           .RES.L      16
CV1                                                                 ; section
  00000000                _VEC_TBL1:                                ; static: VEC_TBL1
  00000000 00000000           .DATA.L     _main
CV2                                                                 ; section
  00000000                _VEC_TBL2:                                ; static: VEC_TBL2
  00000000 00000000           .DATA.L     _nmi_int
```

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Sep.15.04	—	First edition issued

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