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Renesas Electronics Corporation

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H8SX Family

BFST Bit Field Transfer

Introduction

Shows an example of C compiler use of the BFST instruction.

Contents

1. Specifications

- The H8SX family microcomputer BFST instruction performs the following processing.
  - Transfers a bit field specified by the source operand to the lower bits of a specified 8-bit general register Rd.
  - The bit field is indicated by bits of 8-bit immediate data for which 1 is set.
- In this sample task, bit transfer is performed using a C-language structure, and the assembly language code generated by the C compiler is shown.

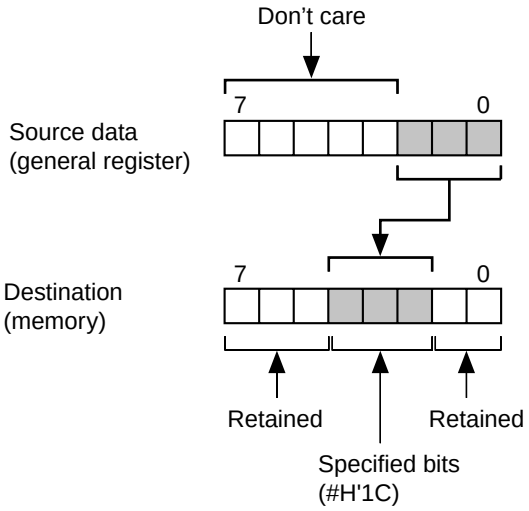


Figure 1 BFST Instruction Processing

2. Functions Used

This sample task shows an example of use of the BFST instruction by the C compiler.

3. Principles of Operation

(1) To confirm BFST instruction operation, a 1-byte RAM area (BFTST) is divided into three as a structure. The BFTST structure is shown in figure 2.

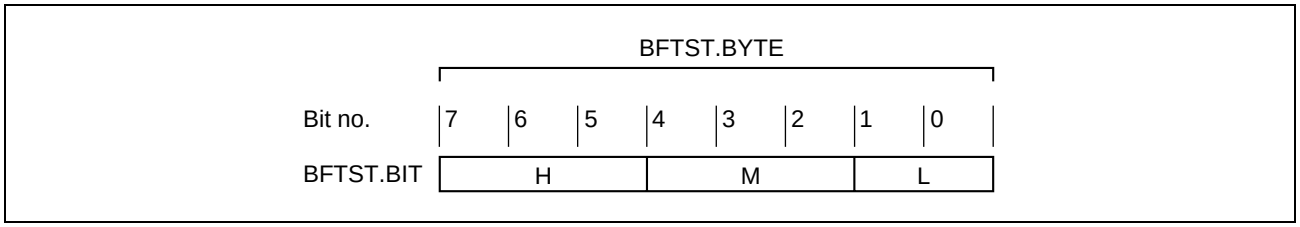


Figure 2 BFTST Structure

(2) Table 1 shows an example of a C program that writes data to the M area of the BFTST structure, and the assembly language code generated by the H8SX C compiler.

Table 1 BFST Code

Sample C Program	Sample Assembler Code Generated by the C compiler
`void main(void)`	`_main:`
`{`	`.`
`.`	`.`
`.`	`.`
`/* Write to bits 4 to 2 of BFTST memory */`	`; Write to bits 4 to 2 of BFTST memory`
`BFTST.BIT.M = 0x7;`	`MOV.B #H'07:8,R0L`
`.`	`BFST R0L,#H'1C,@_BFTST:32`
`}`	`.`

4. Development Environment

4.1 Development Support Tool Versions

The development environment support tools of this sample task is shown in table 2.

Table 2 Development Support Tool Versions

Software Name	Version Used
CH38.EXE	C compiler (H8S, H8/300 series C/C++ compiler) Ver. 6.0.00.005
ASM38.EXE	Assembler (H8S, H8/300 series cross assembler) Ver. 6.0.01.005
OPTLNK.EXE	Linkage editor (optimizing linkage editor) Ver. 8.0.00.020
LBG38.EXE	Library configuration tool (H8S, H8/300 series C/C++ standard library generator) Ver. 2.0.00.000

4.2 C compiler Option Settings

C compiler option settings for this sample task are shown in table 3.

Table 3 C compiler Option Settings

Option	Set Value
CPu	H8SXA:24:MD
Code	Machinecode
OPtimize	1
REGParam	3
SPeed	Register, SHift, STruct, Expression

5. Description of Software

5.1 Modules

Modules used by this sample task are shown in table 4.

Table 4 Modules

Module Name	Function
main	Main routine Writes data to BFTST.BIT.M.

5.2 Arguments

No arguments are used by this sample task.

5.3 Internal Registers Used

No internal registers are used by this sample task.

5.4 RAM Usage

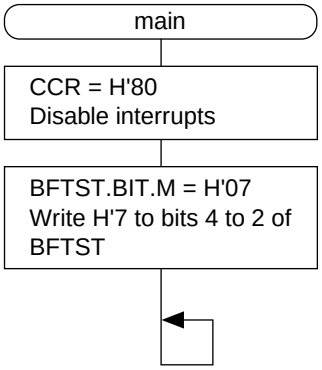
Table 5 describes RAM usage in this sample task.

Table 5 RAM Usage

Label	Size	Function
BFTST	1 byte	BFST test memory — BFTST.BIT.H: Bits 7 to 5 — BFTST.BIT.M: Bits 4 to 2 — BFTST.BIT.L: Bits 1, 0

6. Flowcharts

6.1 Main Routine



6.2 Link Address Specifications

Section Name	Address
CV1	H'000000
P	H'001000
B	H'FEC000

7. Program Listing

7.1 C Program

```
/************************************************************/
/*                                                          */
/*  H8SX Family                                             */
/*  Application Note                                        */
/*                                                          */
/*  'Bit Field STore'                                       */
/*                                                          */
/*  Function                                                */
/*  : BFST                                                  */
/*                                                          */
/*                                                          */
/*                                                          */
/*                                                          */
/************************************************************/

#include    <machine.h>

/************************************************************/
/*  Function define                                         */
/************************************************************/
void main ( void );

/************************************************************/
/*  RAM define                                              */
/************************************************************/
union {                                 /* Bit Field Test Memory        */
    unsigned char BYTE;
    struct {
        unsigned char   H :3;           /* bit7-5                       */
        unsigned char   M :3;           /* bit4-2                       */
        unsigned char   L :2;           /* bit1-0                       */
    } BIT;
}BFTST;

/************************************************************/
/*  Vector Address                                          */
/************************************************************/
#pragma section     V1                  /* VECTOR SECTOIN SET           */
void (*const VEC_TBL1[])(void) = {
    main                                /* 00 Reset                     */
};

#pragma entry main(sp=0xFFC000)
#pragma section                         /* P                            */
/************************************************************/
/*  Main Routine                                            */
/************************************************************/
void main ( void )
{
```

```
    set_ccr(0x80);                          /* Initialize CCR/Interrupt Disable */

    BFTST.BIT.M = 0x07;                     /* Set H'7 --> bit4-2               */

    while(1);
}
```

7.2 Assembly Language Code Generated by the C compiler

```
P                                                                   ; section
                            ;*** File main.c    , Line 48
  00000000                  _main:                                  ; function: main
  00000000 7A0700FFC000         MOV.L       #16760832,SP
  00000006 F980                 MOV.B       #128:8,R1L
  00000008 0309                 LDC.B       R1L,CCR
  0000000A F807                 MOV.B       #7:8,R0L
  0000000C 6A180000F81C     BFST        R0L,#28,@_BFTST:16
  00000014                  L40:
  00000014 4000                 BRA         L40:8
                            ;*** File main.c    , Line 54
B                                                                   ; section
  00000000                  _BFTST:                                 ; static: BFTST
  00000000 00000001             .RES.B      1
CV1                                                                 ; section
  00000000                  _VEC_TBL1:                              ; static: VEC_TBL1
  00000000 00000000             .DATA.L     _main
```

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Sep.15.04	—	First edition issued

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