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H8S/2400 Series

Transmit/Receive Operation of Serial Communication Interface with Integrated FIFOs

Introduction

This application note describes continuous transmission and reception using the serial communication interface (SCIF) function and its independent integrated 16-stage FIFO buffers for efficient high-speed continuous transmission and reception.

Target Devices

- H8S/2472, H8S/2463, H8S/2462 Group

Preface

This program can be used with other H8S Family MCUs that have the same internal I/O registers as the devices on which operation has been confirmed. Check the latest version of the manual for any additions and modifications to functions.

Careful evaluation is recommended before using this application note.

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2. Applicable Conditions 3
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1. Specifications

The specifications of this application note apply to the 16-stage FIFO buffers in the transmitter and receiver, respectively, of the SCIF. During transmission 256 bytes of data are transmitted continuously, and during reception data is received continuously. The SCIF is connected to an LPC interface, allowing it to be controlled directly by the LPC host. However, the SCIF is controlled by the CPU in the operations described in this application note.

The detailed specifications for the operations described in this application note are as follows:

- The transmit FIFO and receive FIFO of the SCIF are both enabled.
- The receive FIFO interrupt trigger level is set to 14 bytes.
- The 256 bytes of data transmitted are sent in the sequence H'00, H'01, H'02, …, H'FD, H'FE, H'FF.
- The received data is stored in a 16-byte area in the on-chip RAM.
- The modem control function is not used.
- The loopback test function is disabled.
- Operations stops when an error occurs.
- The SCIF supports asynchronous serial communication.
- The specifications for asynchronous serial communication are shown below.

Item	Set Value
Baud rate	9600bps
Data length	8 bits
Parity	None
Number of stop bits	1 bit

Figure 1 shows an overview of the operations described in this application note.

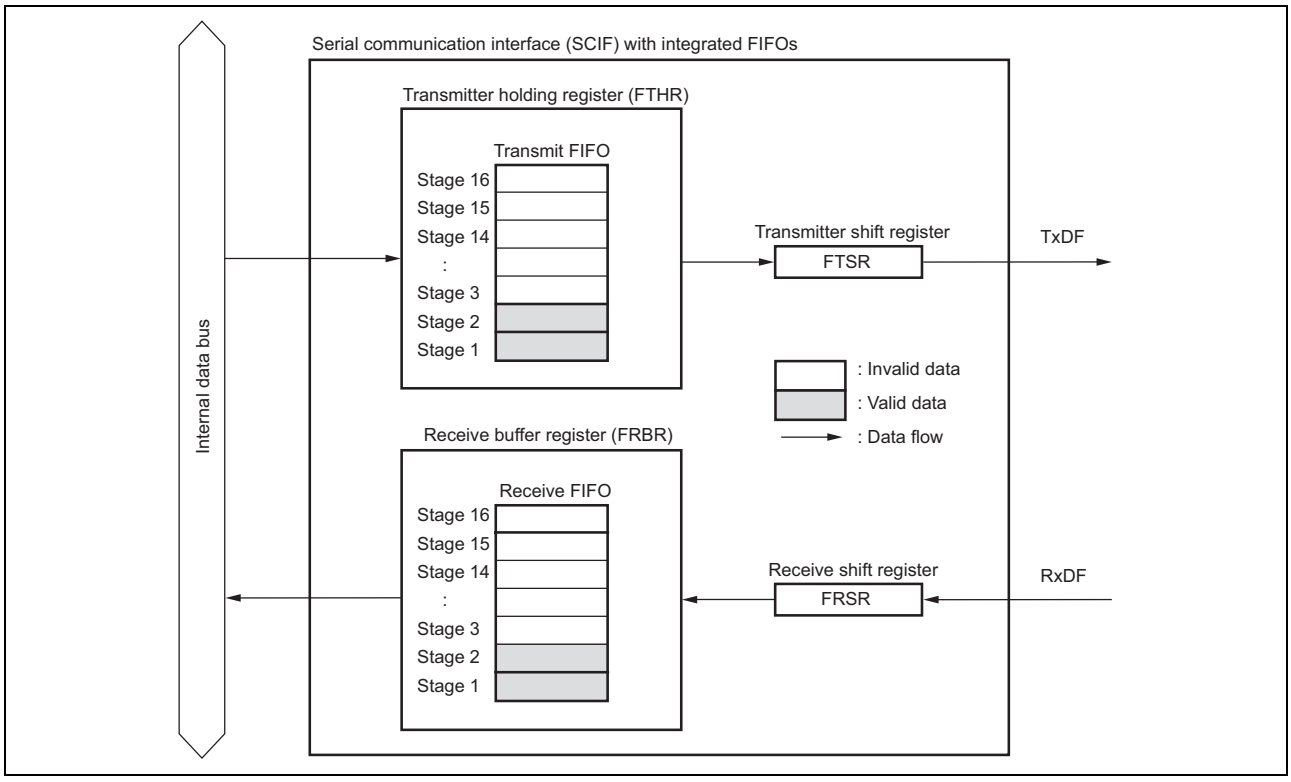

Figure 1 Operation Overview

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Description
Operating frequency	Input clock: 8.0 MHz System clock (ϕ): 32 MHz (8.0 MHz multiplied by 4*)
Operating voltage	3.3V
Operating mode	Mode 2 ($\overline{MD}$2 = 1, MD1 = 1)
Evaluation board	Renesas Technology R0K402472D000BR
Integrated development environment	High-performance Embedded Workshop (HEW) Ver.4.04.01.001
C/C++ compiler	Renesas Technology H8S,H8/300 C/C++ Compiler (V.6.02.00)
Compile options	-cpu=2600A:24, -optimize = 1
Optimizing linkage editor	Renesas Technology Optimizing Linkage Editor (V9.03.00)
Linker options	start = PResetPRG,PIntPRG/0400, P,C,C$DSEC,C$BSEC,D/0800, B,R/0FF0800, S/0FFEE0

Note: * The PLL multiplier circuit multiplies the externally input clock by 4.

3. Functions Used

The SCIF supports asynchronous serial communication.

Asynchronous mode enables serial data transfer to and from a standard asynchronous communication chip such as a universal asynchronous receiver/transmitter (UART). Separate integrated 16-stage FIFO buffers are provided for transmission and reception. The SCIF is connected to an LPC interface, allowing it to be controlled directly by the LPC host. Figure 2 is a block diagram of the SCIF.

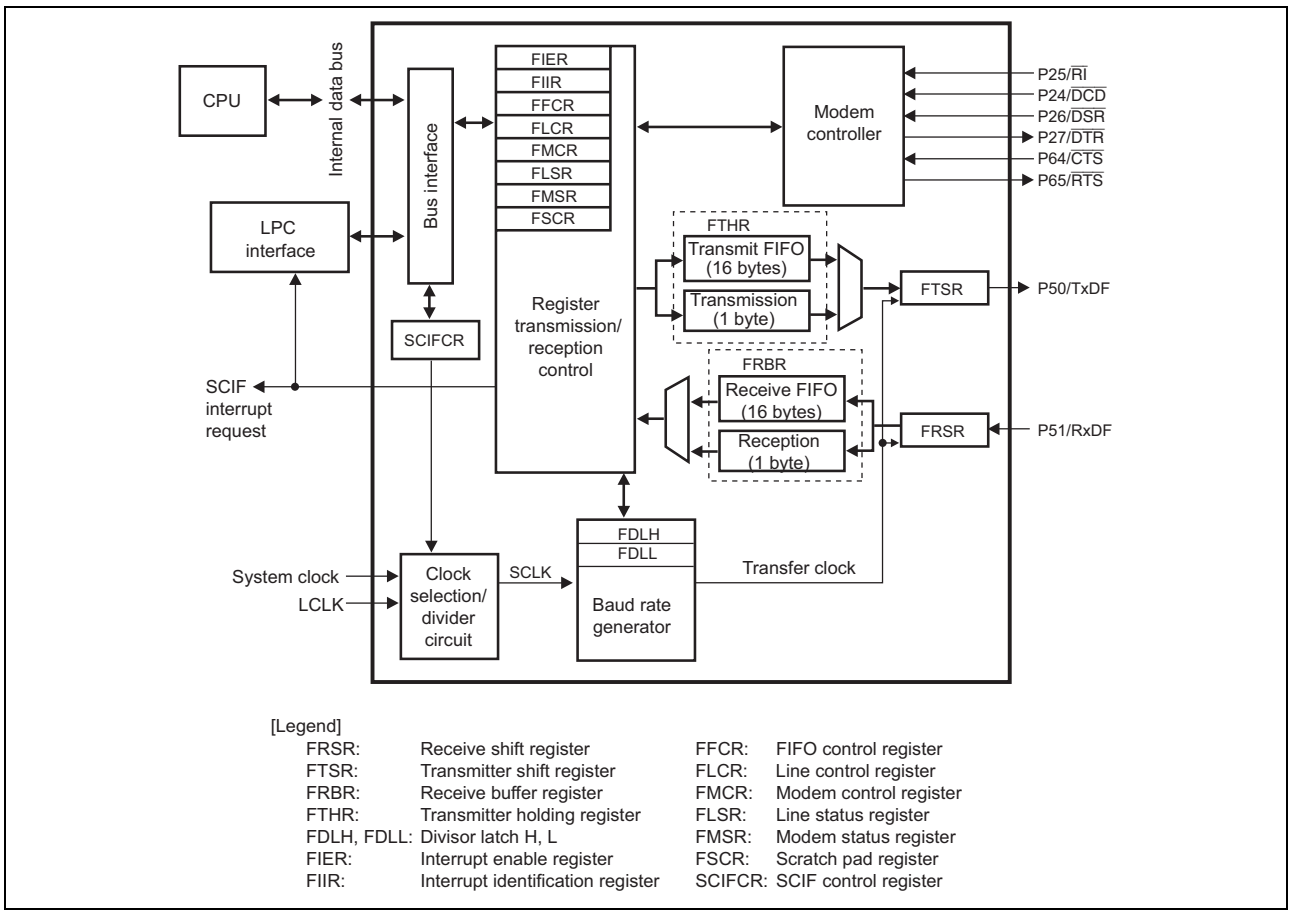

Figure 2 Block Diagram of SCIF

3.1 Baud Rate

The SCIF has an integrated baud rate generator that can be set to a user-defined baud rate by using FDLH, FDLL, and the CKSEL bit in SCIFCR. Table 2 lists baud rate setting examples.

Table 2 Baud Rate Setting Examples

	00		01	
CKSEL1, 0	**LCLK (33 MHz) Divided by 18**		**System Clock (34 MHz) Divided by 11**	
Baud Rate	**FDLH + FDLL (Divisor Value)**	**Error (%)**	**FDLH + FDLL (Divisor Value)**	**Error (%)**
50	H'0900	–0.54%	H'0F18	–0.01%
75	H'0600	–0.54%	H'0A10	–0.01%
110	H'0417	–0.51%	H'06DC	0.01%
300	H'0180	–0.54%	H'0284	–0.01%
600	H'00C0	–0.54%	H'0142	–0.01%
1200	H'0060	–0.54%	H'00A1	–0.01%
1800	H'0040	–0.54%	H'006B	0.30%
2400	H'0030	–0.54%	H'0050	0.62%
4800	H'0018	–0.54%	H'0028	0.62%
9600	H'000C	–0.54%	H'0014	0.62%
14400	H'0008	–0.54%	H'000D	—
19200	H'0006	–0.54%	H'000A	0.62%
38400	H'0003	–0.54%	H'0005	0.62%
57600	H'0002	–0.54%	H'0003	—
115200	H'0001	–0.54%	H'0002	—

The equation for calculating the baud rate is as follows:

Baud rate = (clock frequency input to baud rate generator) / (16 × divisor value)

3.2 Operation in Asynchronous Communication

Figure 3 illustrates the typical format for asynchronous serial communication. One frame consists of a start bit (low level), followed by transmit/receive data (LSB-first: from the least significant bit), a parity bit, and a stop bit (high level). In asynchronous serial communication, the transmission line is usually held high in the mark state (high level). The SCIF monitors the transmission line, and when it detects the space state (low level), recognizes a start bit and starts serial communication. Inside the SCIF, the transmitter and receiver are independent units, enabling full-duplex communication. Both of the transmitter and receiver also have a 16-stage FIFO buffered structure so that data can be read or written during transmission or reception, enabling continuous data transmission and reception.

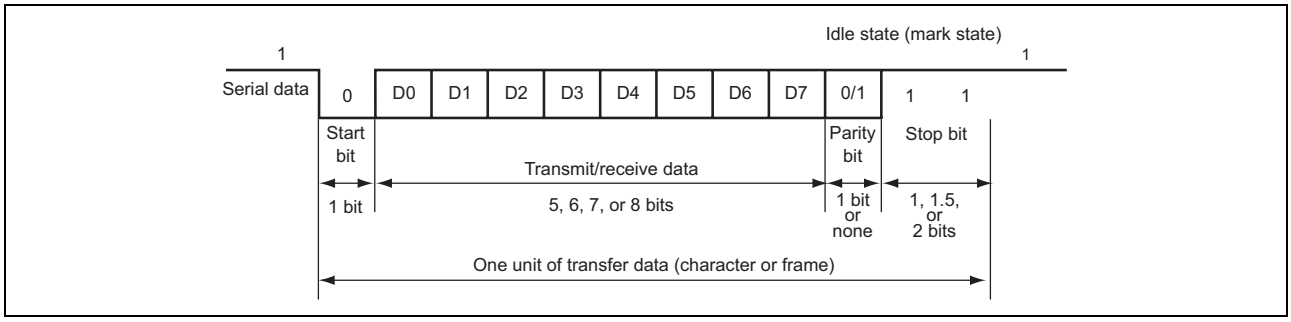

Figure 3 Data Format in Serial Transmission/Reception (Example with 8-Bit Data, Parity and 2 Stop Bits)

4. Operation

The transmission of 256 bytes of data and the reception of 30 bytes of data are described below, using figures 4 and 5 as examples. When no data is input to or output from the receive FIFO for a duration equivalent to 4 characters while one or more characters remain in the receive FIFO, a character timeout interrupt is generated.

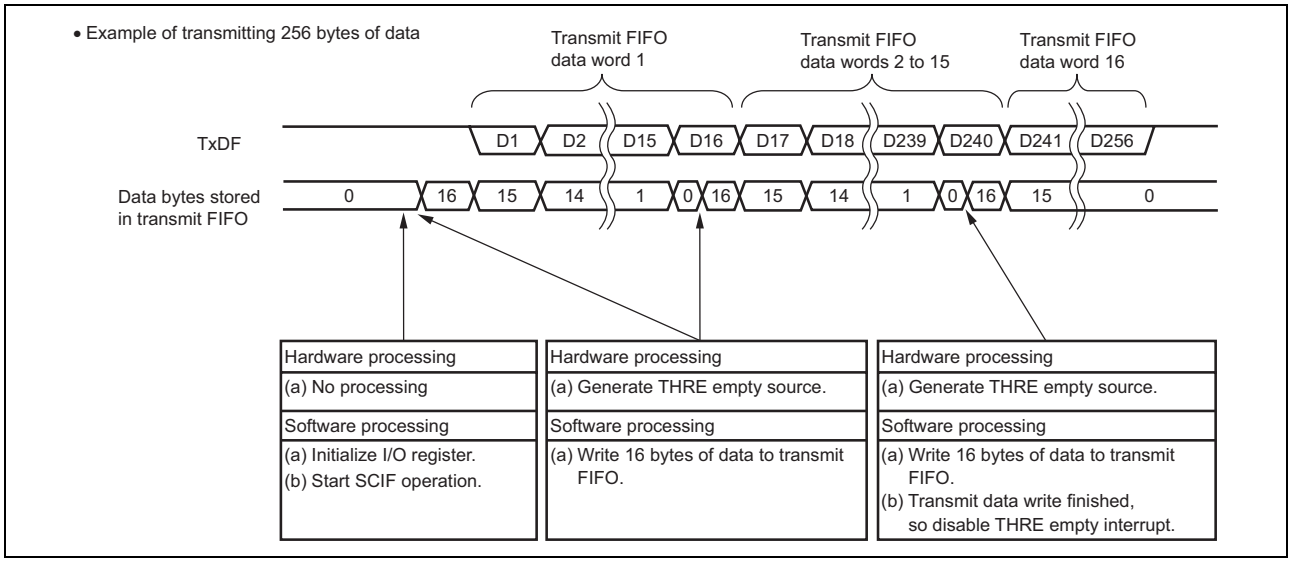

Figure 4 Transmit Operation

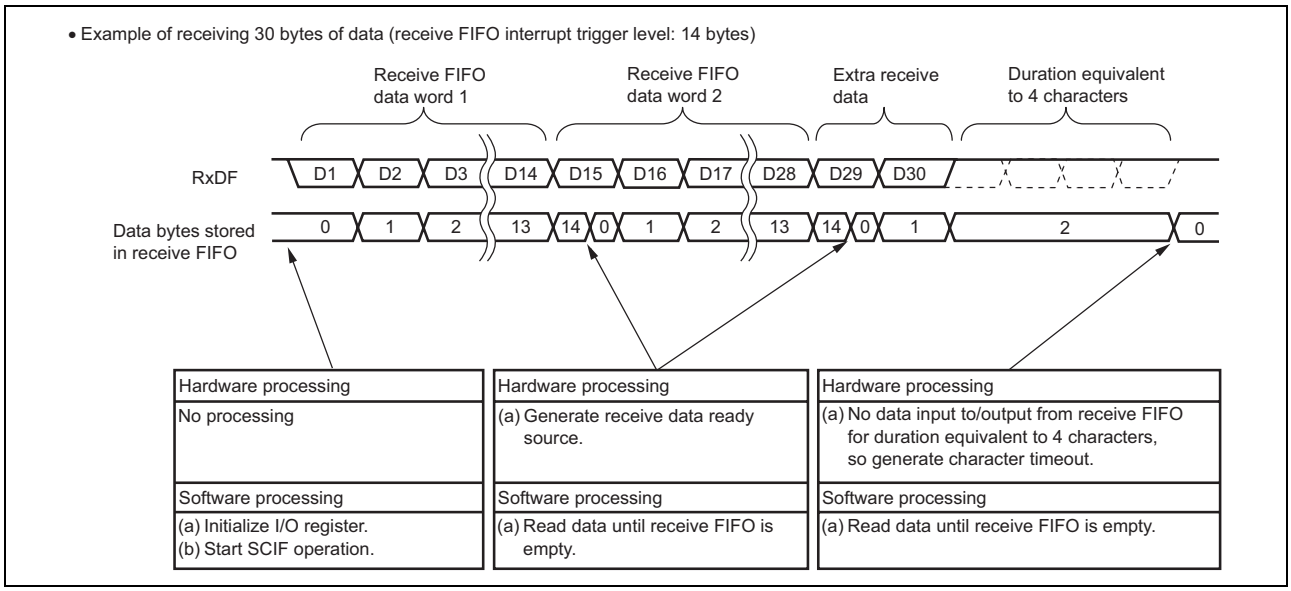

Figure 5 Receive Operation

5. Functions

5.1 Symbolic Constants

Table 3 List of Symbolic Constants

Constant Name	Set Value	Description	Used by Functions
MAX_SCIF_DATA_CNT	256	Maximum transmit data byte count	transmit_func
MODEM_STATUS	0	Identifier number when pending interrupt is modem status	INT_SCIFI
FTHR_EMPTY	1	Identifier number when pending interrupt is FTHR empty	INT_SCIFI
RECEIVE_DATA_READY	2	Identifier number when pending interrupt is receive data ready	INT_SCIFI
RECEIVE_LINE_STATIS	3	Identifier number when pending interrupt is receive line status	INT_SCIFI
CHARACTER_TIMEOUT	6	Identifier number when pending interrupt is character timeout	INT_SCIFI

5.2 Unions

Table 4 List of Unions

Type	Union Name	Type	Variable Name	Type	Variable Name	No. of Bits	Description	Used by Function
union	uFIIR	unsigned char	BYTE	—	—	8	Byte access variable	INT_SCIFI
		struct	BIT	unsigned char	FIFOE	2	Shows setting status of transmit and receive FIFOs.	
				unsigned char	—	2	—	
				unsigned char	INTID	3	Shows which pending interrupt has the highest priority.	
				unsigned char	INTPEND	1	Shows whether a pending interrupt is enabled or disabled.	

5.3 ROM Variables

Table 5 List of ROM Variables

Type	Variable Name	Set Value	Description	Used by Functions
const unsigned char	scif_transmit_data [MAX_SCIF_DATA_CNT]	0x00, 0x01, 0x02, …, …, 0xFD, 0xFE, 0xFF	Transmit data	transmit_func

5.4 RAM Variables

Table 6 List of RAM Variables

Type	Variable Name	Set Value	Description	Used by Functions
unsigned char	scif_receive_data[16]	All initialized to 0x00	Receive data storage	init receive_func
unsigned int	scif_transmit_count	0x00	Transmit byte count	init transmit_func
union uFIIR	SCIF_FIIR	FIIR register contents	FIIR register contents storage	INT_SCIFI

5.5 List of Functions

Table 7 List of Functions

Function Name	Description
PowerON_Reset	• Initial settings function Initializes status pointer (SP), sets interrupt mask bits, sets uninitialized/initialized data, calls main function.
main	• Main function Calls init function, starts SCI transmit/receive operation.
init	• I/O register initialization function Initializes registers.
receive_func	• Data transmit function Stores data in transmit FIFO in 16-byte units.
transmit_func	• Data receive function Stores receive data from receive FIFO in on-chip RAM.
INT_SCIFI	• SCIF interrupt handling function Performs receive processing, transmit processing, modem status processing, and error handling.

5.6 Functions

5.6.1 PowerON_Reset Function

(1) Functional Overview

The PowerON_Reset function initializes the status pointer (SP) and uses embedded functions and standard library functions to set interrupt mask bits and set uninitialized/initialized data. Then it calls the main function.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

None

(5) Flowchart

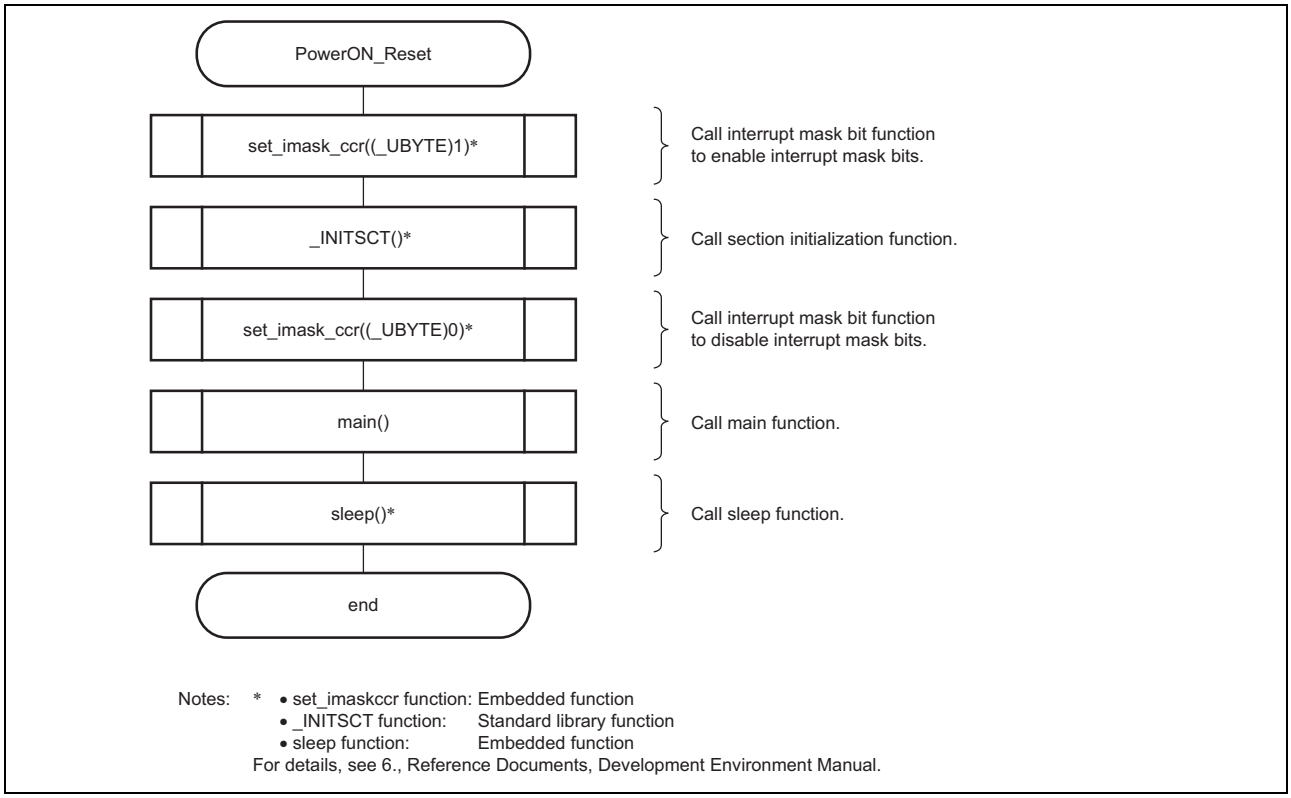

Figure 6 Power-On Reset Flowchart (PowerON_Reset)

5.6.2 main Function

(1) Functional Overview

The main function calls the init function to initialize the registers and start serial communication transmit and receive operation.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

None

(5) Flowchart

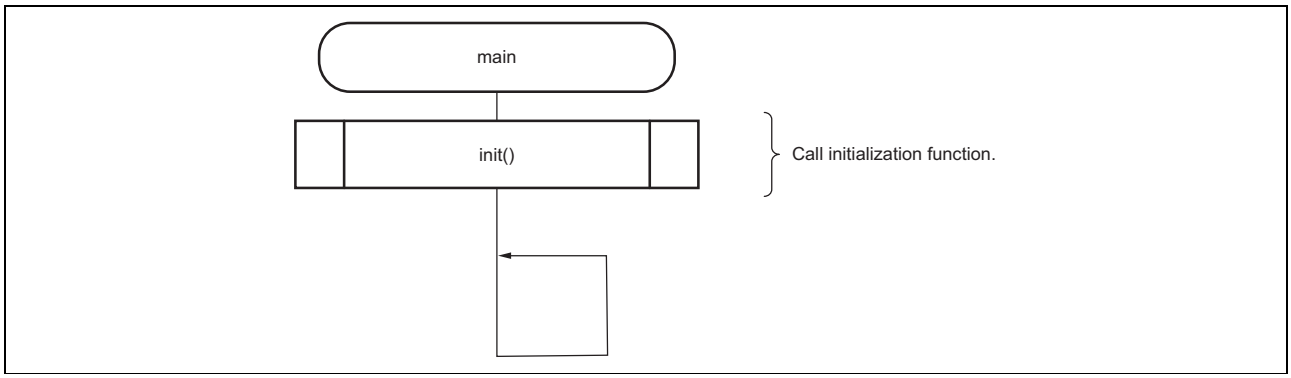

Figure 7 Main Flowchart (main)

5.6.3 init Function

(1) Functional Overview

The init function initializes the registers and starts serial communication transmit and receive operation.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

The internal I/O registers used by this function are shown below. Note that the setting values shown are those used for this sample task and differ from the initial values.

- Mode Control Register (MDCR) - Number of bits: 8, Address: H'FFFFC5

Bit	Bit Name	Set Value	R/W	Descriptions
2	MDS2	—	R	Mode Select 2 and 1
1	MDS1	—	R	These bits indicate the input levels at mode pins ($\overline{MD2}$ and MD1) (the current operating mode). Bits MDS2 and MDS1 correspond to the $\overline{MD2}$ and MD1 pins, respectively. MDS2 and MDS1 are read-only bits and writing to them has no effect. The mode pin ($\overline{MD2}$ and MD1) input levels are latched into these bits when MDCR is read. These latches are canceled by a reset.

- Standby Control Register (SBYCR) - Number of bits: 8, Address: H'FFFF84

Bit	Bit Name	Set Value	R/W	Descriptions
2	SCK2	0	R/W	System Clock Select
1	SCK1	0	R/W	These bits select the clock for the bus master in high-speed mode and medium-speed mode.
0	SCK0	0	R/W	000: High-speed mode (Initial value)

- SUBMSTPBL causes on-chip peripheral modules to shift to module stop mode in module units. Each module can be set to module stop mode by setting the corresponding bit to 1.

- Sub-Chip Module Stop Control Register BL (SUBMSTPBL) - Number of bits: 8, Address: H'FFFE3F

Bit	Bit Name	Set Value	R/W	Descriptions
3	SMSTPB3	0	R/W	Serial communication interface with FIFOs (SCIF)

- Host Interface Control Register 5 (HICR5) - Number of bits: 8, Address: H'FFFD09

Bit	Bit Name	Set Value	R/W	Descriptions
1	SCIFE	0	R/W	SCIF Enable Enables or disables access from the LPC host of the SCIF. 0: Disables access to the SCIF from the LPC host

- SCIF Control Register (SCIFCR) - Number of bits: 8, Address: H'FFFC88

Bit	Bit Name	Set Value	R/W	Descriptions
7	SCIFOE1	1	R/W	These bits enable or disable PORT output of the SCIF. The PORT function differs according to the combination with the SCIF bit in HICR5 of the LPC. 11: P65pin: PORT P27pin: PORT P50pin: TxDF
6	SCIFOE0	1	R/W	
3	CKSEL1	0	R/W	These bits select the clock (SCLK) to be input to the baud rate generator. 01: System clock divided by 11
2	CKSEL0	1	R/W	

- Line Control Register (FLCR) - Number of bits: 8, Address: H'FFFC83

Bit	Bit Name	Set Value	R/W	Descriptions
7	DLAB	0	R/W	Divisor Latch Address FDLL and FDLH are placed at the same addresses as the FRBR/FTHR and FIER addresses. This bit selects which register is to be accessed. 0: FRBR/FTHR and FIER access enabled 1: FDLL and FDLH access enabled
3	PEN	0	R/W	Parity Enable Selects whether to add a parity bit for data transmission and whether to perform a parity check for data reception. 0: No parity bit added/parity check enabled
2	STOP	0	R/W	Stop Bit Specifies the stop bit length for data transmission. For data reception, only the first stop bit is checked regardless of the setting. 0: 1 stop bit
1	CLS1	1	R/W	Character Length Select 0, 1
0	CLS0	1	R/W	These bits specify transmit/receive character data length. 11: Data length is 8 bits

- The FDLH and FDLL are registers used to set the baud rate. They are accessible when the DLAB bit in FLCR is 1. Frequency division ranging from 1 to (2^{16}-1) can be set with these registers. The frequency divider circuit stops when both of FDLH and FDLL are 0 (initial value).

- Divisor Latch H (FDLH) - Number of bits: 8, Address: H'FFFC81

Bit	Bit Name	Set Value	R/W	Descriptions
7 to 0	Bit 7 to bit 0	H'00	R/W	Upper 8 bits of divisor latch

- Divisor Latch L (FDLL) - Number of bits: 8, Address: H'FFFC80

Bit	Bit Name	Set Value	R/W	Descriptions
7 to 0	Bit 7 to bit 0	H'0D	R/W	Lower 8 bits of divisor latch

Baud rate = (Clock frequency input to baud rate generator) / (16 × divisor value)

- FIFO Control Register (FFCR) - Number of bits: 8, Address: H'FFFC82

Bit	Bit Name	Set Value	R/W	Descriptions
7	RCVRTRIG1	1	W	Receive FIFO Interrupt Trigger Level 1, 0
6	RCVRTRIG0	1	W	These bits set the trigger level of the receive FIFO interrupt. 11: 14 bytes
2	XMITFRST	1	W	Transmit FIFO Reset The transmit FIFO data is cleared when 1 is written. However, FTSR data is not cleared. This bit is automatically cleared.
1	RCVRFRST	1	W	Receive FIFO Reset The receive FIFO data is cleared when 1 is written. However, FRSR data is not cleared. This bit is automatically cleared.
0	FIFOE	1	W	FIFO Enable 1: Transmit/receive FIFOs enabled

- FIER is a register that enables or disables interrupts. It is accessible when the DLAB bit in FLCR is 0.
- Interrupt Enable Register (FIER) - Number of bits: 8, Address: H'FFFC81

Bit	Bit Name	Set Value	R/W	Descriptions
3	EDSSI	0	R/W	Modem Status Interrupt Enable 0: Modem status interrupt disabled
2	ELSI	1	R/W	Receive Line Status Interrupt Enable 1: Receive line status interrupt enabled
1	ETBEI	1	R/W	FTHR Empty Interrupt Enable 1: FTHR empty interrupt enabled
0	ERBFI	1	R/W	Receive Data Ready Interrupt Enable A character timeout interrupt is included when the FIFO is enabled. 1: Receive data ready interrupt enabled

- Modem Control Register (FMCR) - Number of bits: 8, Address: H'FFFC81

Bit	Bit Name	Set Value	R/W	Descriptions
4	LOOPBACK	0	R/W	Loopback Test The transmit data output is internally connected to the receive data input, and the transmit data output pin (RxDF) becomes 1. The receive data input pin is disconnected from external sources. The four modem control input pins ($\overline{DSR}$, $\overline{CTS}$, $\overline{RI}$, and $\overline{DCD}$) are disconnected from external sources, and the pins are internally connected to the four modem control output signals ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT1}$, and $\overline{OUT2}$), respectively. The transmit data is received immediately in loopback mode. Enabling/disabling of interrupts is set by the OUT2LOOP bit in SCIFCR and FIER. 0: Loopback function disabled
3	OUT2	1	R/W	Enables or disables the SCIF interrupt. 1: Interrupt enabled

(5) Flowchart

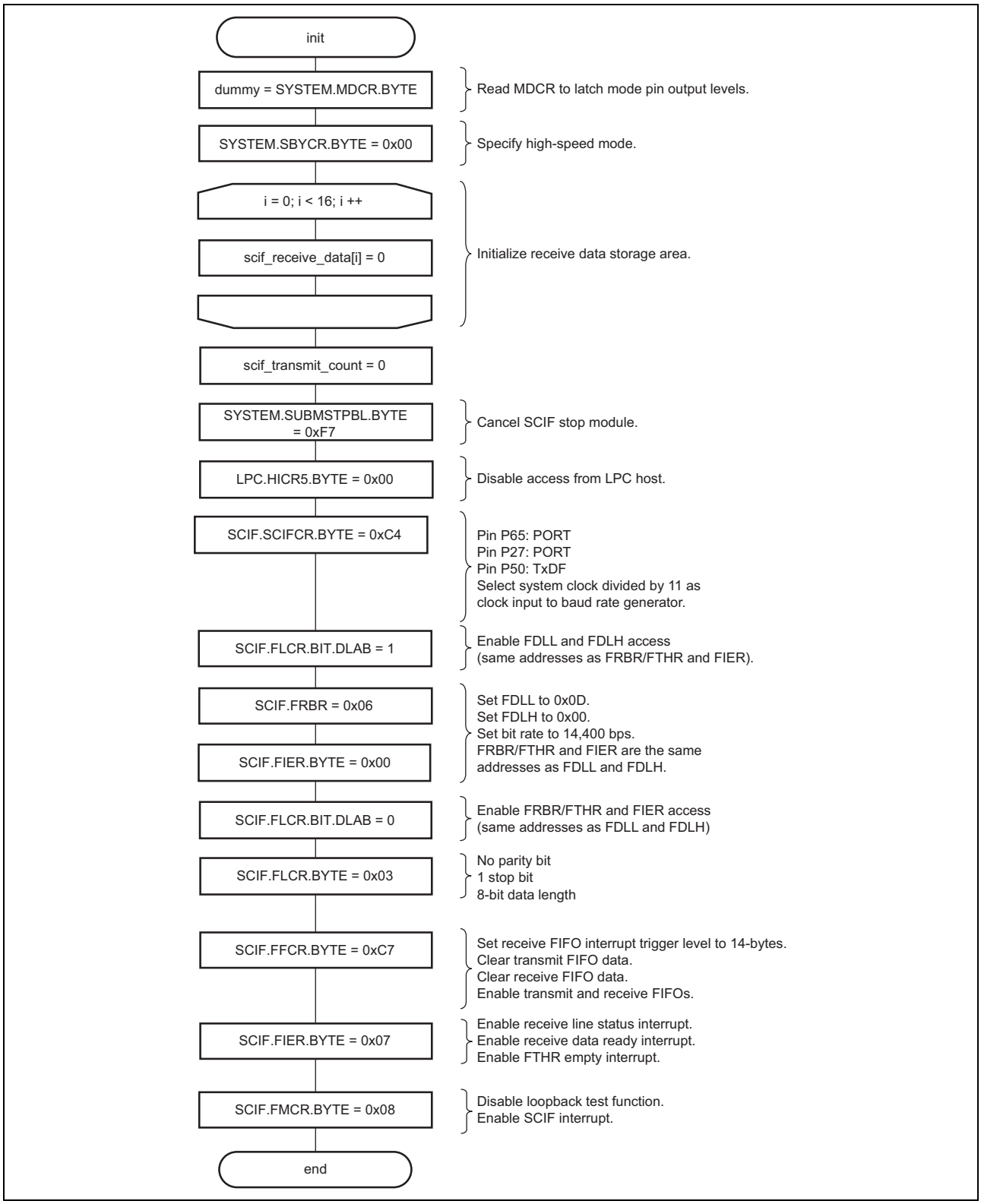

Figure 8 Initialization Flowchart (init)

5.6.4 receive_func Function

(1) Functional Overview

After confirming that there are no errors, the receive_func function transfers receive data from the receive FIFO to the on-chip RAM.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

The internal I/O registers used by this function are shown below. Note that the setting values shown are those used for this sample task and differ from the initial values.

- Line Status Register (FLSR) - Number of bits: 8, Address: H'FFFC85

Bit	Bit Name	Set Value	R/W	Descriptions
7	RXFIFOERR	—	R	Receive FIFO Error Indicates that at least one data error (parity error, framing error, or break interrupt) has occurred when the FIFO is enabled. 0: No receive FIFO error [Clearing condition] When FRBR is read or FLSR is read while there is no remaining data that could cause an error after an FIFO clear. 1: A receive FIFO error [Setting condition] When at least one data error (parity error, framing error, or break interrupt) has occurred in the FIFO
4	BI	—	R	Break Interrupt Indicates detection of the receive data break signal. When the FIFO is enabled, a break interrupt occurs in any receive data in the FIFO, and this bit is set when the receive data is in the first FIFO buffer. Reception of the next data starts after the input receive data becomes mark and a valid start bit is received. 0: Break signal not detected [Clearing condition] FLSR read 1: Break signal detected [Setting condition] When input receive data stays at space (low level) for a reception time exceeding the length of one frame

Bit	Bit Name	Set Value	R/W	Descriptions
3	FE	—	R	Framing Error Indicates that the stop bit of the receive data is invalid. When the FIFO is enabled, this error occurs in any receive data in the FIFO, and this bit is set when the receive data is in the first FIFO buffer. The UART attempts resynchronization after a framing error occurs. The UART, which assumes that the framing error is due to the next start bit, samples the start bit and treats it as a start bit. 0: No framing error [Clearing condition] FLSR read 1: A framing error [Setting condition] Invalid stop bit in the receive data
2	OE	—	R	Parity Error This bit indicates a parity error in the receive data when the PEN bit in FLCR is 1. When the FIFO is enabled, this error occurs in any receive data in the FIFO, and this bit is set when the receive data is in the first FIFO buffer. 0: No parity error [Clearing condition] FLSR read If this bit is set during an overrun error, read FLSR twice. 1: A parity error [Setting condition] Detection of parity error in receive data
1	PE	—	R	Overrun Error Indicates occurrence of an overrun error. • When the FIFO is disabled When reception of the next data has been completed without the receive data in FRBR having been read, an overrun error occurs and the previous data is lost. • When the FIFO is enabled When the FIFO is full and reception of the next data has been completed, an overrun error occurs. The FIFO data is retained, but the last received data is lost. 0: No overrun error [Clearing condition] FLSR read 1: An overrun error [Setting condition] Occurrence of an overrun error

Bit	Bit Name	Set Value	R/W	Descriptions
0	DR	—	R	Data Ready Indicates that receive data is stored in FRBR or the FIFO. 0: No receive data [Clearing condition] FRBR is read or all of the FIFO data is read. 1: Receive data remains. [Setting condition] Reception of data

- Receive Buffer Register (FRBR) - Number of bits: 8, Address: H'FFFC80

Bit	Bit Name	Set Value	R/W	Descriptions
7 to 0	Bit 7 to bit 0	—	R/W	These bits store received serial data. The data unit is 16 bytes when the FIFO is enabled.

(5) Flowchart

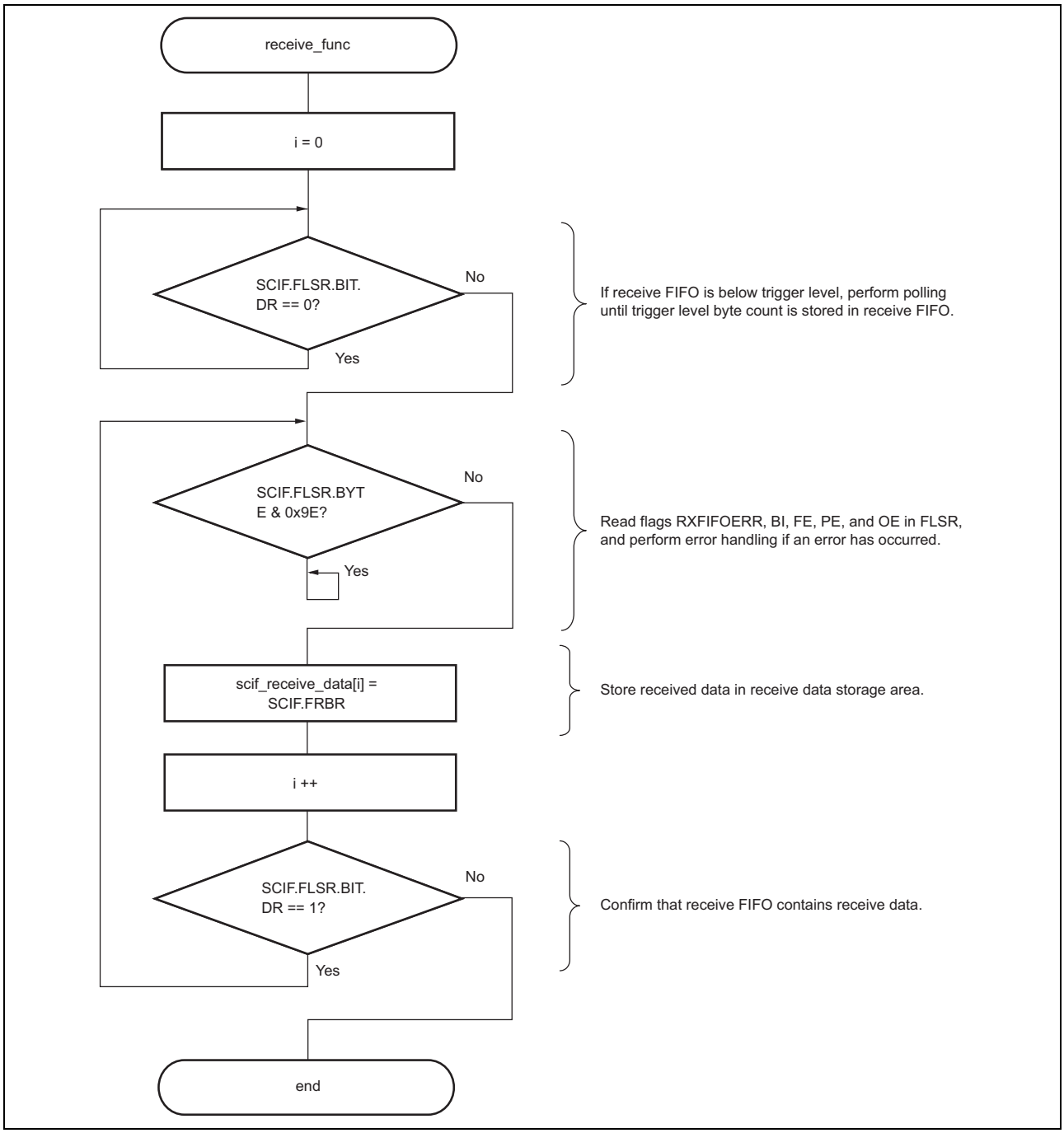

Figure 9 Data Receive Flowchart (receive_func)

5.6.5 transmit_func Function

(1) Functional Overview

The transmit_func Function writes 16 bytes of data to the transmit FIFO.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

The internal I/O registers used by this function are shown below. Note that the setting values shown are those used for this sample task and differ from the initial values.

- Line Status Register (FLSR) - Number of bits: 8, Address: H'FFFC85

Bit	Bit Name	Set Value	R/W	Descriptions
5	THRE	—	R	FTHR Empty Indicates that FTHR is ready to accept new data for transmission. • When the FIFO is enabled 0: Transmit data of one or more bytes remains in the transmit FIFO. [Clearing condition] Transmit data is written to FTHR. 1: No transmit data remains in the transmit FIFO. [Setting condition] When the transmit FIFO becomes empty • When the FIFO is disabled 0: Transmit data remains in FTHR. [Clearing condition] Transmit data is written to FTHR 1: No transmit data in FTHR [Setting condition] When data transfer from FTHR to FTSR is completed

- Transmitter Holding Register (FTHR) - Number of bits: 8, Address: H'FFFC80

Bit	Bit Name	Set Value	R/W	Descriptions
7 to 0	Bit 7 to bit 0	—	W	Stores serial data to be transmitted. The data is 16 bytes when the FIFO is enabled.

- Interrupt Enable Register (FIER) - Number of bits: 8, Address: H'FFFC81

Bit	Bit Name	Set Value	R/W	Descriptions
1	ETBEI	0	R/W	FTHR Empty Interrupt Enable 0: FTHR empty interrupt disabled

(5) Flowchart

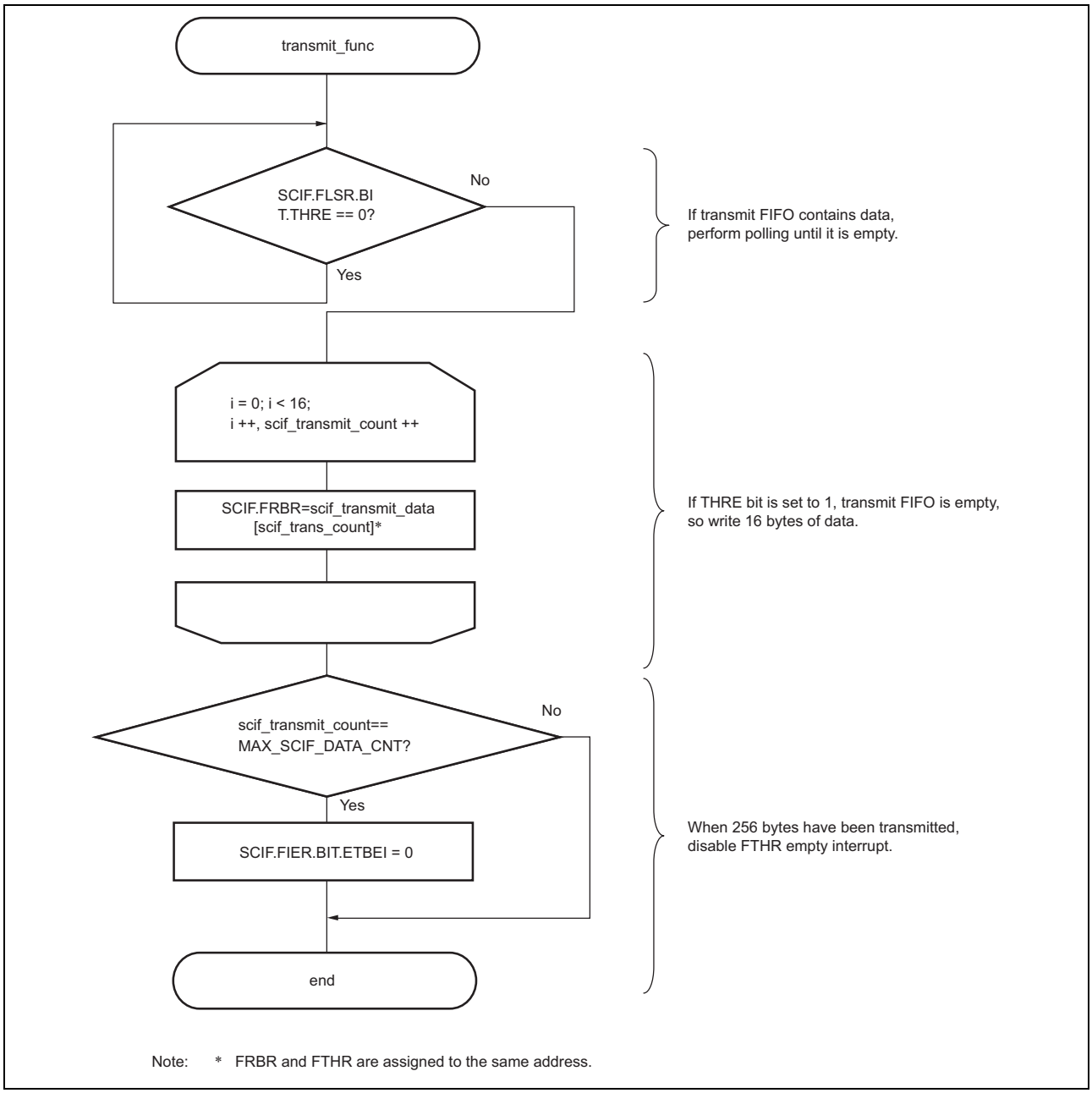

Figure 10 Data Transmit Flowchart (transmit_func)

5.6.6 INT_SCIFI Function

(1) Functional Overview

The INT_SCIFI function performs error handling (overrun errors, parity errors, framing errors, break interrupts) and handling when any of the following interrupts occur: receive data ready (receive data remaining, FIFO trigger level), character timeout (no data input to/output from receive FIFO for duration equivalent to 4 characters while one or more characters remain in receive FIFO), FTHR empty (FTHR empty), and modem status (CTS, DSR, RI, DCD).

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

The internal I/O registers used by this function are shown below. Note that the setting values shown are those used for this sample task and differ from the initial values.

- Interrupt Identification Register (FIIR) - Number of bits: 8, Address: H'FFFC82

Bit	Bit Name	Set Value	R/W	Descriptions
3	INTID2	—	R	Interrupt ID2, ID1, ID0
2	INTID1	—	R	These bits Indicate the interrupt of the highest priority among the
1	INTID0	—	R	pending interrupts. 000: Modem status 001: FTHR empty 010: Receive data ready 011: Receive line status 110: Character timeout (when the FIFO is enabled)
0	INTPEND	—	R	Interrupt Pending Indicates whether one or more interrupts are pending. 0: Interrupt pending 1: No interrupt pending

(5) Flowchart

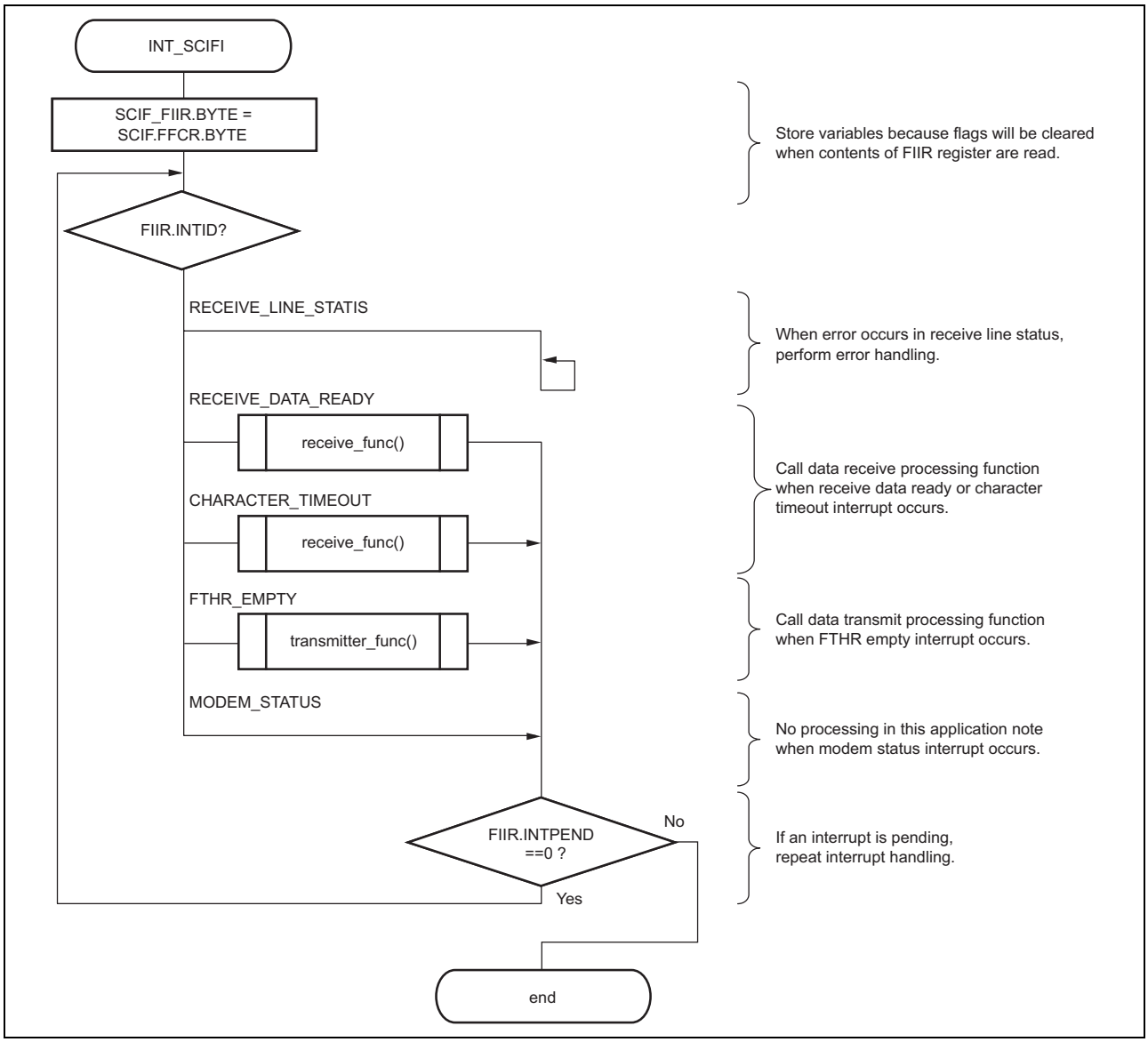

Figure 11 Interrupt Flowchart (INT_SCIFI)

6. Reference Documents

- Hardware Manual
  H8S/2472, H8S/2463, H8S/2462 Group Hardware Manual
  (The latest version can be downloaded from the Renesas Technology Web site.)
- Development Environment Manual
  H8S/300, H8/300 Series C/C++ Compiler Package User's Manual
  (The latest version can be downloaded from the Renesas Technology Web site.)
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