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H8S/2400 Series

Sine Wave Output Using 14-Bit PWM Timer

Introduction

This application note presents an example of using the 14-bit pulse width modulation (PWM) timer (PWMX) function to produce sine wave output.

The PWMX can be used as a 14-bit D/A converter by connecting a low-pass filter to an external pin of the device.

Target Devices

- H8S/2472, H8S/2463, H8S/2462 Group

Preface

This program can be used with other H8S Family MCUs that have the same internal I/O registers as the devices on which operation has been confirmed. Check the latest version of the manual for any additions and modifications to functions.

Careful evaluation is recommended before using this application note.

Contents

1. Specifications

The specifications of this application note cover using the compare match interrupt of the 16-bit free-running timer (FRT) to convert the PWMX duty value, and outputting a 1 Hz sine wave by connecting a low-pass filter to the external pin of the PWMX. The example presented in this application note covers PWMX operation before the connection with the low-pass filter.

The detailed specifications for the operations described in this application note are listed below. Figure 1 shows an overview of the operations described in this application note.

- The PWMX duty value is changed by using the FRT compare match interrupt.
- FRT compare matches are set to be generated with a period identical to one PWMX conversion cycle.
- The number of times the PWMX duty value changes per sine wave period is equal to the number of PWMX conversion cycles in one sine wave period.
- Data stored in the on-chip ROM is used as the basis for changing the PWMX duty value.
- The number of pulses (base cycles) generated during one PWMX conversion cycle is set at 64.
- The PWMX resolution (T) is set at one system clock cycle (tcyc).
- The PWMX output phase is set to inverted output.
- Pin PWX0 is used as the PWM output pin.

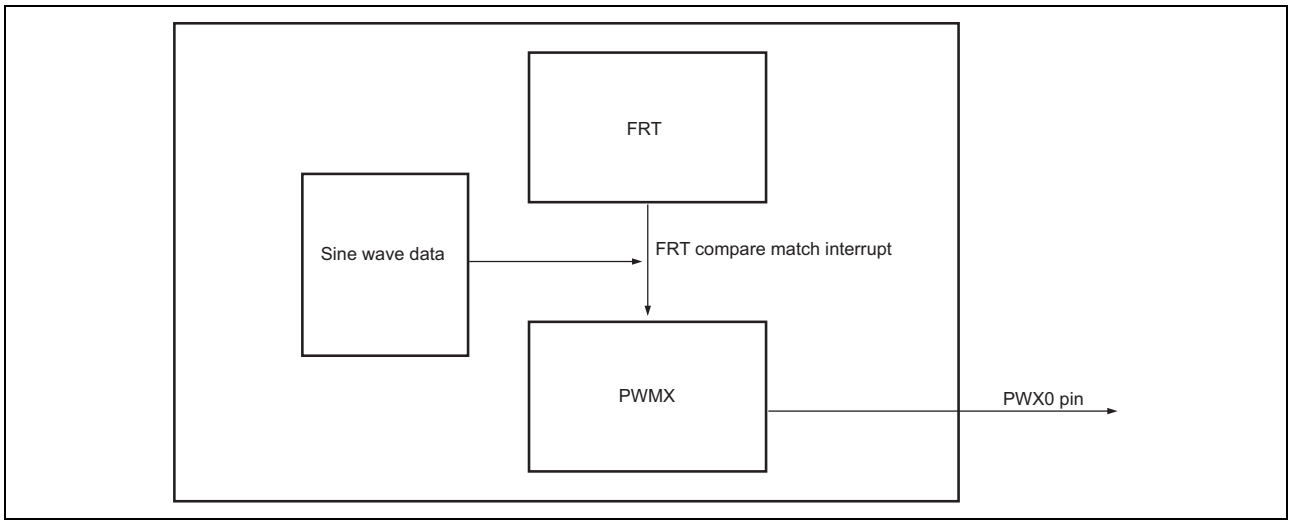


Figure 1 Operation Overview

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Description
Operating frequency	Input clock: 8.0 MHz System clock (ϕ): 32 MHz (8.0 MHz multiplied by 4*)
Operating voltage	3.3V
Operating mode	Mode 2 ($\overline{MD2}$ = 1, MD1 = 1)
Evaluation board	Renesas Technology R0K402472D000BR
Integrated development environment	High-performance Embedded Workshop (HEW) Ver.4.04.01.001
C/C++ compiler	Renesas Technology H8S,H8/300 C/C++ Compiler (V.6.02.00)
Compile options	-cpu=2600A:24, -optimize = 1
Optimizing linkage editor	Renesas Technology Optimizing Linkage Editor (V9.03.00)
Linker options	start = PResetPRG,PIntPRG/0400, P,C,C$DSEC,C$BSEC,D/0800, B,R/0FF0800, S/0FFEE00

Note: * The PLL multiplier circuit multiplies the externally input clock by 4.

3. Functions Used

A PWM waveform like the one shown in figure 2 is output from the PWX pin. The value of DA13 to DA0 in the PWMX (D/A) control register (DADR) corresponds to the total 0-level width (TL) of the pulses output in one conversion cycle (256 pulses when CFS = 0, 64 pulses when CFS = 1). When OS = 0, the waveform is output directly. When OS = 1, the output waveform is inverted. In this case, the value of DA13 to DA0 in DADR corresponds to the total 1-level width (TH) of the output pulses. Figures 3 and 4 show the types of waveform output available.

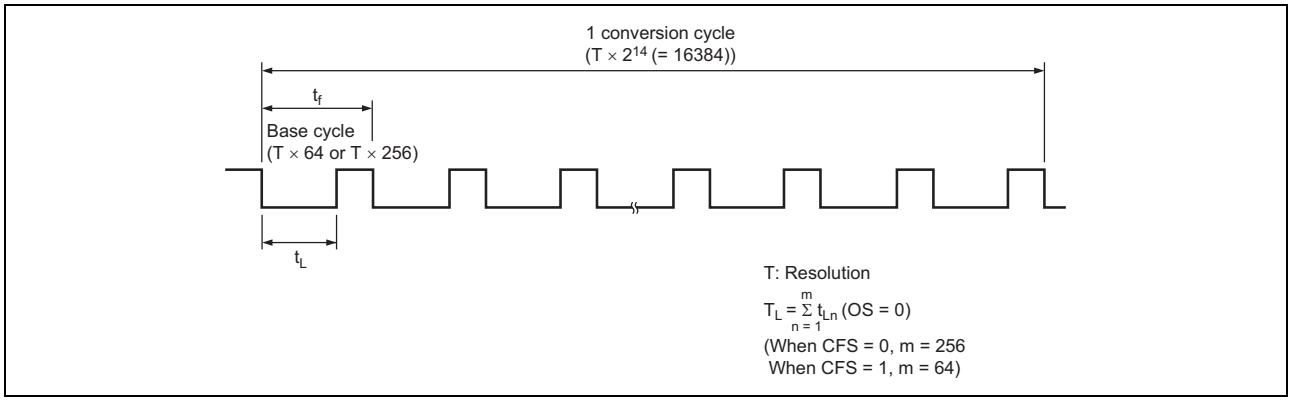


Figure 2 PWMX (D/A) Operation

The PWM output level remains fixed unless DA13 to DA0 in DADR contain at least a certain minimum value. The correspondence between the value of the OS bit and the output waveform is shown in figures 3 and 4.

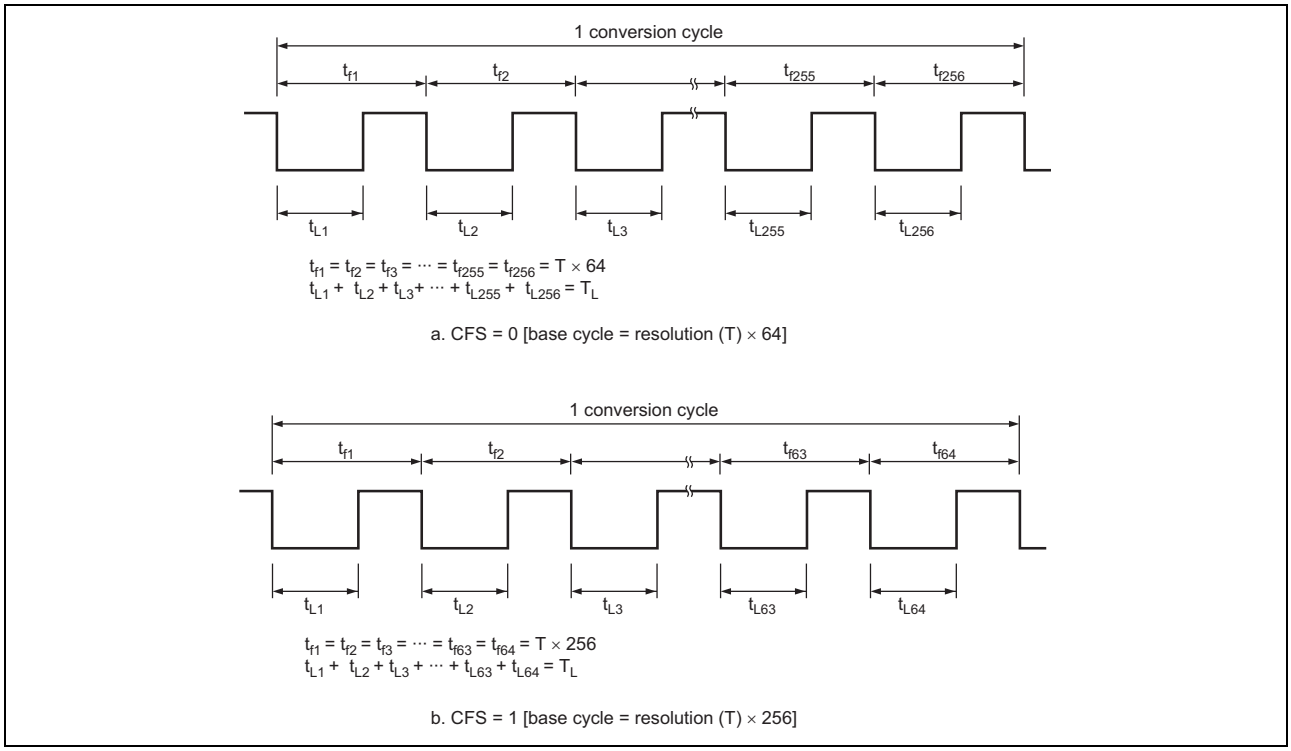
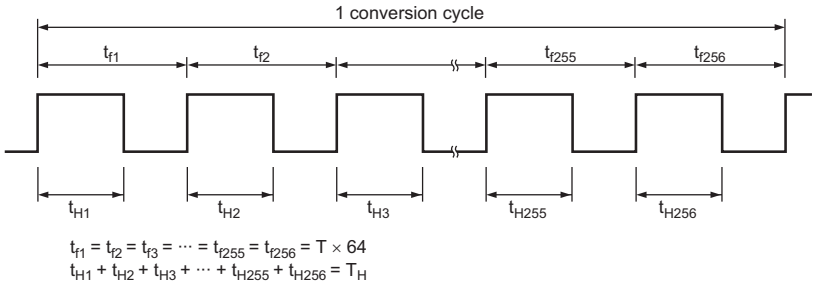
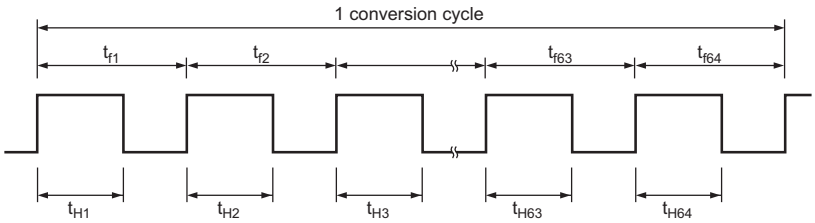


Figure 3 Output Waveform (OS = 0, DADR corresponds to T_L)



$t_{f1} = t_{f2} = t_{f3} = \cdots = t_{f255} = t_{f256} = T \times 64$
$t_{H1} + t_{H2} + t_{H3} + \cdots + t_{H255} + t_{H256} = T_H$

a. CFS = 0 [base cycle = resolution (T) × 64]



$t_{f1} = t_{f2} = t_{f3} = \cdots = t_{f63} = t_{f64} = T \times 256$
$t_{H1} + t_{H2} + t_{H3} + \cdots + t_{H63} + t_{H64} = T_H$

b. CFS = 1 [base cycle = resolution (T) × 256]

Figure 4 Output Waveform (OS = 1, DADR corresponds to T_H)

An example of the additional pulses when CFS = 1 (base cycle = resolution (T) × 256) and OS = 1 (inverted PWM output) is described below. When CFS = 1, the upper eight bits (DA13 to DA6) in DADR determine the duty ratio of the base pulse, and the next six bits (DA5 to DA0) determine the locations of the additional pulses as shown in figure 5.

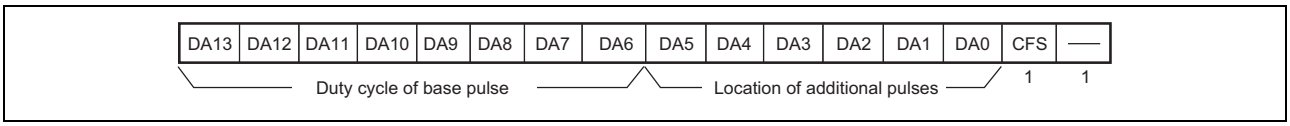


Figure 5 D/A Data Register Configuration when CFS = 1

In this example, DADR = H'0207 (B'0000 0010 0000 0111). Figure 6 shows the output waveform. Since CFS = 1 and the value of the upper eight bits is B'0000 0010, the base pulse has a duty ratio with a high width of 2 / 256 × (T).

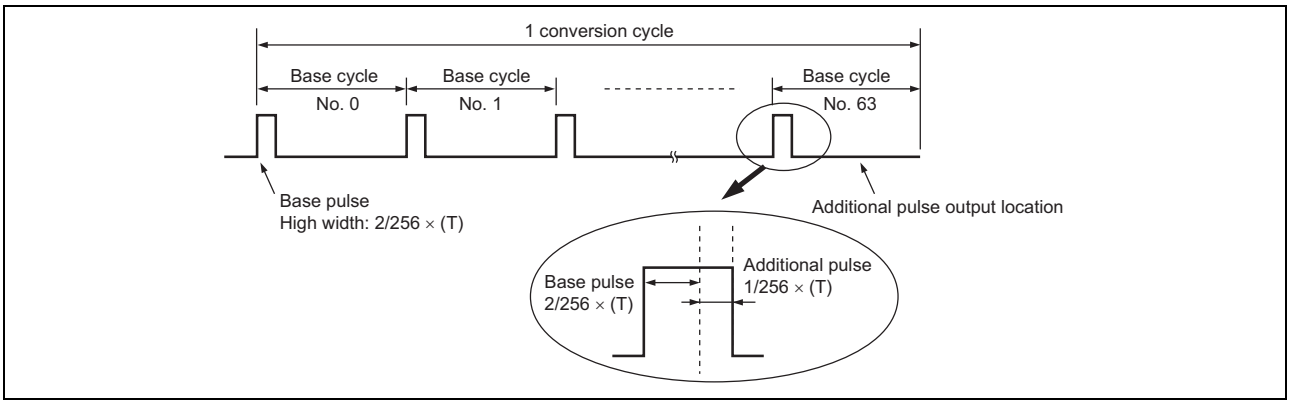


Figure 6 Output Waveform when DADR = H'0207 (OS = 1)

However, when CFS = 0 (base cycle = resolution (T) × 64), the duty ratio of the base pulse is determined by the upper six bits and the locations of the additional pulses by the next eight bits, in a manner similar to the above.

4. Operation

The example below illustrate calculating the number of PWMX duty changes in one sine wave period and generating sine wave data.

- Example: Calculating the Number of PWMX Duty Changes in One Sine Wave Period
  When the sine wave output resolution is equal to one PWMX conversion cycle ($T \times 2^{14}$):

  1 Hz / (tcyc × 16,384) = 1 Hz / 512 μs ≈ 1,953 points

Therefore, the number of PWMX duty changes in one sine wave period is 1,953.

Note that in the interests of efficient utilization of the available ROM capacity, the program presented in this application note uses 977 bytes of sine wave data, approximately half the available capacity, and the PWMX duty value is changed by shifting the sine wave data reference offset back and forth.

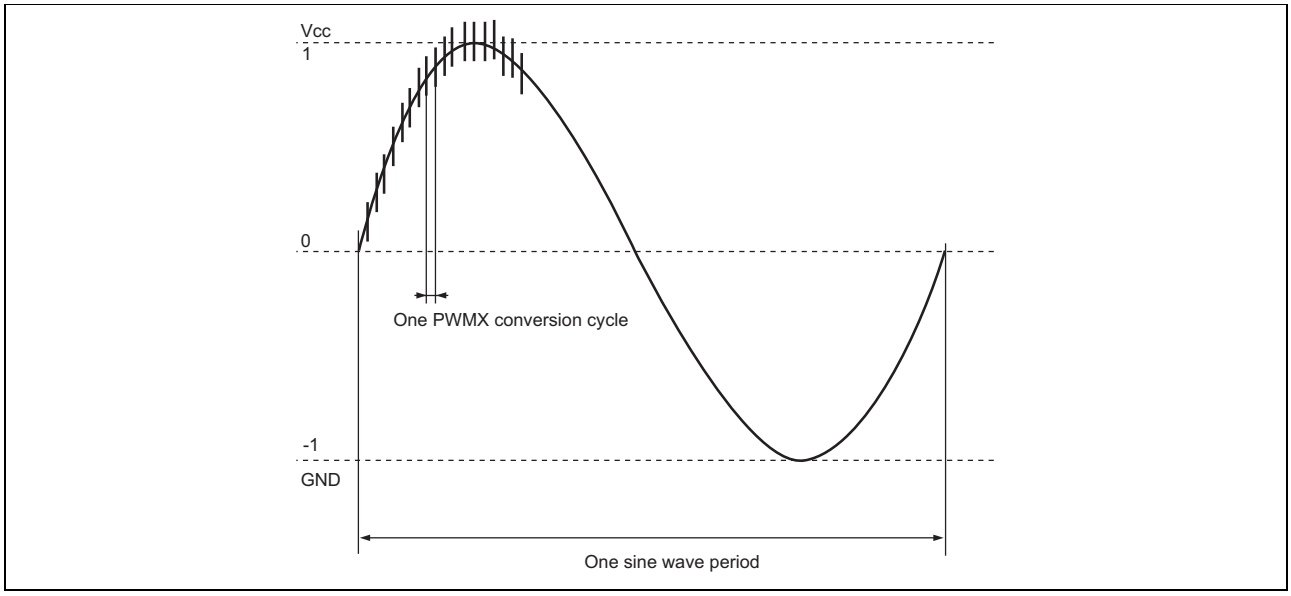


Figure 7 Sine Wave Conceptual View

- Example: Generating Sine Wave Data
  The sine wave data (14 bits) is set in DA13 to DA0 in PWMX (D/A) data register A (DADRA).
  Note that the PWM output level is fixed when bits DA13 to DA0 in DADRA are set to a value outside the range H'0040 to H'3FFF. Therefore, in this example setting values for bits DA13 to DA0 (sine wave data) are generates within the range H'003F to H'3FFF (H'3FC0).

  sin θ × (H'3FC0 / 2) + (H'3FC0 / 2) + H'3F = sine wave data

Figure 8 shows the operation described in this application note.

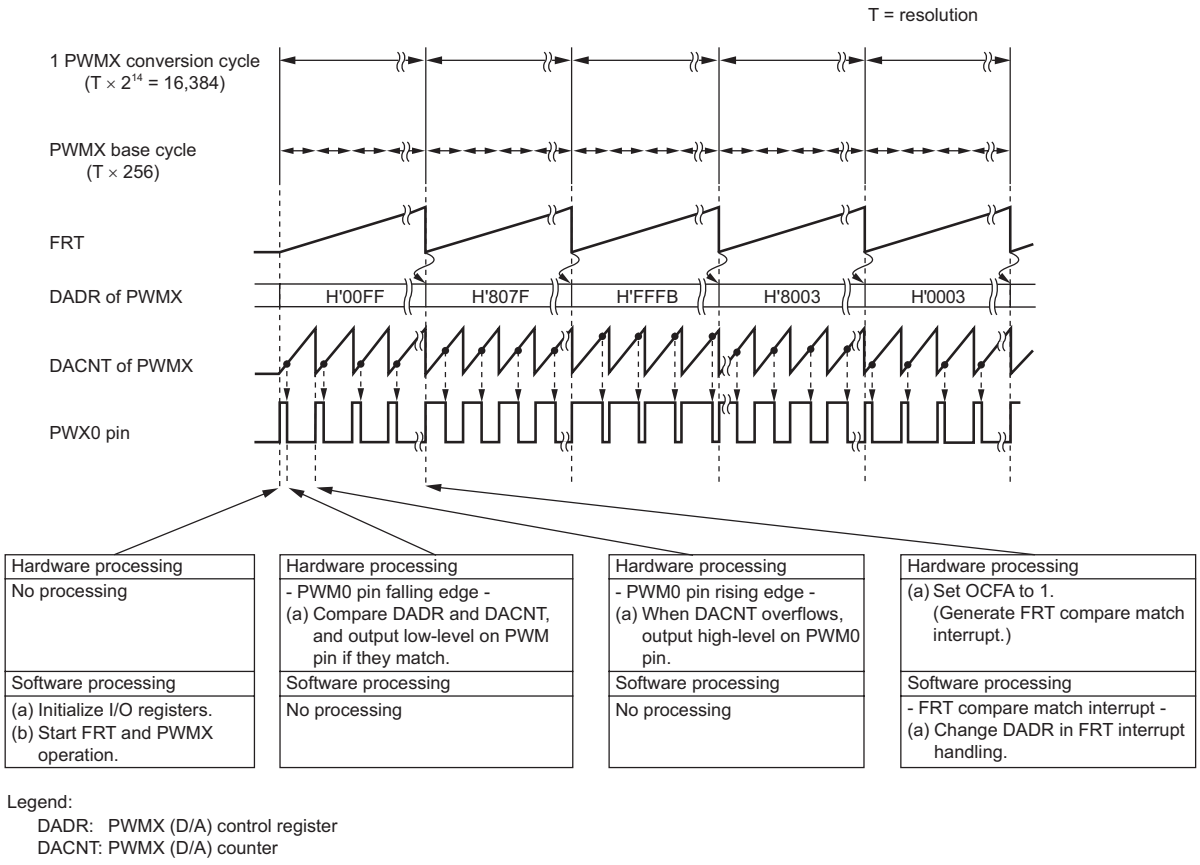


Figure 8 Operation

5. Functions

5.1 Symbolic Constants

Table 2 List of Symbolic Constants

Constant Name	Set Value	Description	Used by Functions
MAX_PWM_DATA_CNT	977	Number of data bytes in sine wave data table	INT_OCIA_FRT

5.2 ROM Variables

Table 3 List of ROM Variables

Type	Variable Name	Set Value	Description	Used by Functions
const unsigned int	pwm_table [MAX_PWM_DATA_CNT]	0x00FF, 0x00FF, …, …, 0xFFFB, 0xFFFB	Sine wave data table	INT_OCIA_FRT

5.3 RAM Variables

Table 4 List of RAM Variables

Type	Variable Name	Set Value	Description	Used by Functions
unsigned int	pwm_count	0x00	Sine wave data table reference count value	init INT_OCIA_FRT
signed int	pwm_add_value	0x01	Sine wave data table reference count change value	init INT_OCIA_FRT

5.4 List of Functions

Table 5 List of Functions

Function Name	Description
PowerON_Reset	• Initial settings function Initializes status pointer (SP), sets interrupt mask bits, sets uninitialized/initialized data, calls main function.
main	• Main function Calls init function and starts PWMX output.
init	• I/O register initialization function Initializes registers.
INT_OCIA_FRT	• FRT interrupt handling function Changes the PWMX output pulse duty.

5.5 Functions

5.5.1 PowerON_Reset Function

(1) Functional Overview

The PowerON_Reset function initializes the status pointer (SP) and uses embedded functions and standard library functions to set interrupt mask bits and set uninitialized/initialized data. Then it calls the main function.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

None

(5) Flowchart

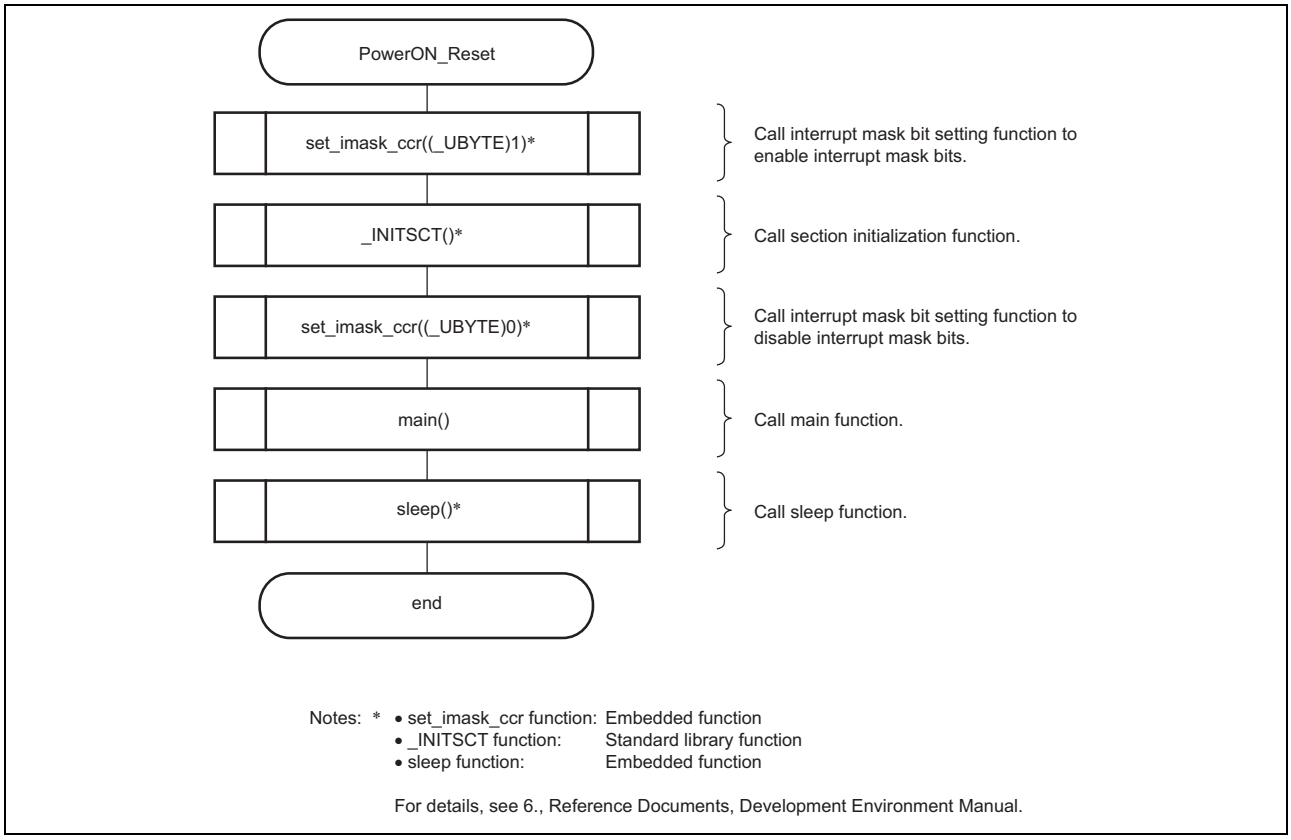


Figure 9 Power-On Reset Flowchart (PowerON_Reset)

5.5.2 main Function

(1) Functional Overview

The main function calls the init function to perform register initialization and start PWMX pulse output.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

None

(5) Flowchart

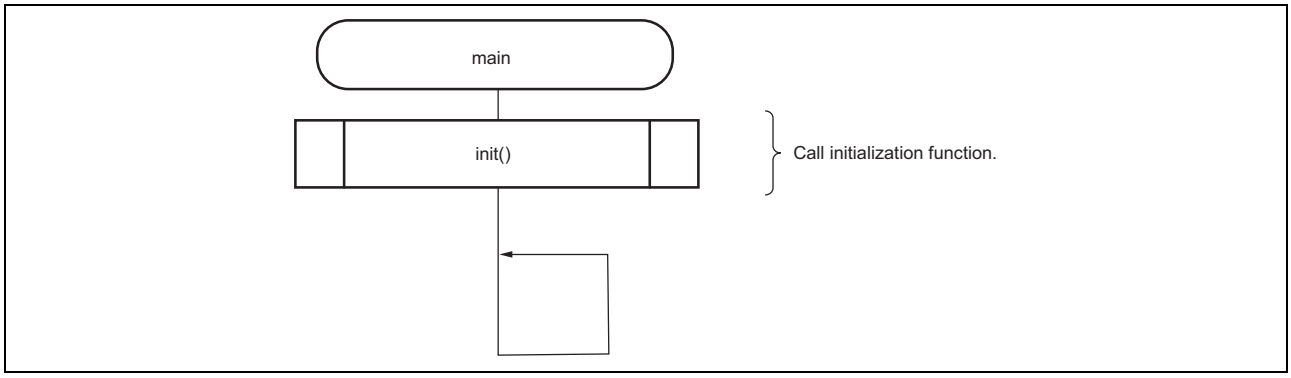


Figure 10 Main Flowchart (main)

5.5.3 init Function

(1) Functional Overview

The init function initializes registers and starts PWM pulse output.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

The internal I/O registers used by this function are shown below. Note that the setting values shown are those used in this application note and differ from the initial values.

- Mode Control Register (MDCR) - Number of bits: 8, Address: H'FFFFC5

Bit	Bit Name	Set Value	R/W	Descriptions
2	MDS2	—	R	Mode Select 2 and 1
1	MDS1	—	R	These bits indicate the input levels at mode pins ($\overline{MD2}$ and MD1) (the current operating mode). Bits MDS2 and MDS1 correspond to $\overline{MD2}$ and MD1, respectively. MDS2 and MDS1 are read-only bits and they cannot be written to. The mode pin ($\overline{MD2}$ and MD1) input levels are latched into these bits when MDCR is read. These latches are canceled by a reset.

- Standby Control Register (SBYCR) - Number of bits: 8, Address: H'FFFF84

Bit	Bit Name	Set Value	R/W	Descriptions
2	SCK2	0	R/W	System Clock Select
1	SCK1	0	R/W	Select a clock for the bus master in high-speed mode or medium-speed mode.
0	SCK0	0	R/W	000: High-speed mode

- MSTPCR is used to put individual on-chip peripheral modules into module stop mode. Setting a bit to 1 makes the corresponding module enter the module stop mode.
- Module Stop Control Register A (MSTPCRA) - Number of bits: 8, Address: H'FFFE43

Bit	Bit Name	Set Value	R/W	Descriptions
1	MSTPA1	0	R/W	14-bit PWM timer (PWMX_0)

- Module Stop Control Register H (MSTPCRH) - Number of bits: 8, Address: H'FFFF86

Bit	Bit Name	Set Value	R/W	Descriptions
5	MSTP13	0	R/W	16-bit free-running timer (FRT)
3	MSTP11	0	R/W	14-bit PWM timer (PWMX)

- Timer Interrupt Enable Register (TIER) - Number of bits: 8, Address: H'FFFF90

Bit	Bit Name	Set Value	R/W	Descriptions
3	OCIAE	1	R/W	Output Compare Interrupt A Enable Selects whether to enable output compare interrupt A request (OCIA) when output compare flag A (OCFA) in TCSR is set to 1. 1: OCIA requested by OCFA is enabled

- Timer Control/Status Register (TCSR) - Number of bits: 8, Address: H'FFFF91

Bit	Bit Name	Set Value	R/W	Descriptions
0	CCLRA	1	R/W	Counter Clear A Selects whether the FRC is to be cleared on compare-match A (when the FRC and OCRA values match). 1: FRC is cleared on compare-match A

- Timer Control Register (TCR) - Number of bits: 8, Address: H'FFFF96

Bit	Bit Name	Set Value	R/W	Descriptions
1	CKS1	0	R/W	Select clock source for FRC.
0	CKS0	0	R/W	00: ϕ/2 internal clock source

- Timer Output Compare Control Register (TOCR) - Number of bits: 8, Address: H'FFFF97

Bit	Bit Name	Set Value	R/W	Descriptions
6	OCRAMS	0	R/W	Output Compare A Mode Select Specifies whether OCRA is used in the normal operating mode or in the operating mode using OCRAR and OCRAF. 0: The normal operating mode is specified for OCRA
5	ICRS	0	R/W	Input Capture Register Select Controls the access to OCRAR and OCRAF. 0: Access is disabled
4	OCRS	0	R/W	Output Compare Register Select OCRA and OCRB share the same address. When this address is accessed, the OCRS bit selects which register is accessed. The operation of OCRA or OCRB is not affected. 0: OCRA is selected

- Output Compare Register A (OCRA) - Number of bits: 16, Address: H'FFFF92
  Function: Each OCR register is a 16-bit readable/writable register. The FRT has two OCR registers, and their contents are continually compared with the FRC value. When the values match (compare match), the OCFA or OCFB flag in TCSR is set to 1. The OCR registers cannot be accessed in 8-bit units. They should always be accessed in 16-bit units.
  Setting value: H'2000

- Port Control Register 0 (PTCNT0) - Number of bits: 8, Address: H'FFFEFE

Bit	Bit Name	Set Value	R/W	Descriptions
3	PWMXS	0	R/W	Selects pins for 14-bit PWM timer outputs. 0: P60/PWX0, P61/PWX1, P62/PWX2, P63/PWX3 are selected

- PWMX (D/A) Data Register A (DADRA) - Number of bits: 16, Address: H'FFFFA0

Bit	Bit Name	Set Value	R/W	Descriptions
15 to 2	DA13 to DA0	All 0	R/W	D/A Data 13 to 0 These bits set a digital value to be converted to an analog value. In each base cycle, the DACNT value is continually compared with the DADR value to determine the duty cycle of the output waveform, and to decide whether to output a fine-adjustment pulse equal in width to the resolution. To enable this operation, this register must be set within a range that depends on the CFS bit. If the DADR value is outside this range, the PWM output is held constant. A channel can be operated with 12-bit precision by fixing DA0 and DA1 to 0. The two data bits are not compared with UC12 and UC13 of DACNT.
1	CFS	1	R/W	Carrier Frequency Select 1: Base cycle = resolution (T) × 256 The range of DA13 to DA0: H'0040 to H'3FFF

- PWMX (D/A) Data Register B (DADRB) - Number of bits: 16, Address: H'FFFFA6

Bit	Bit Name	Set Value	R/W	Descriptions
0	REGS	0/1	R/W	Register Select DADRA and DACR, and DADRB and DACNT, are located at the same addresses. The REGS bit specifies which registers can be accessed. When changing the register to be accessed, set this bit in advance. 0: DADRA and DADRB can be accessed 1: DACR and DACNT can be accessed

- PWMX (D/A) Counter (DACNT) - Number of bits: 16, Address: H'FFFFA6

Bit	Bit Name	Set Value	R/W	Descriptions
15 to 8	UC7 to UC0	all 0	R/W	Lower Up-Counter
7 to 2	UC8 to UC13	all 0	R/W	Upper Up-Counter
0	REGS	0/1	R/W	Register Select DADRA and DACR, and DADRB and DACNT, are located at the same addresses. The REGS bit specifies which registers can be accessed. When changing the register to be accessed, set this bit in advance. 0: DADRA and DADRB can be accessed 1: DACR and DACNT can be accessed

- PWMX (D/A) Control Register (DACR) - Number of bits: 8, Address: H'FFFFA0

Bit	Bit Name	Set Value	R/W	Descriptions
6	PWME	0	R/W	PWMX Enable Starts or stops the PWM D/A counter (DACNT). 0: DACNT operates as a 14-bit up-counter
2	OEA	1	R/W	Output Enable A Enables or disables output on PWMX (D/A) channel A. 1: PWMX (D/A) channel A output (at the PWX0, PWX2 pins) is enabled
1	OS	1	R/W	Output Select Selects the phase of the PWMX (D/A) output. 1: Inverted PWMX (D/A) output
0	CKS	0	R/W	Clock Select Selects the PWMX (D/A) resolution. Eight kinds of resolution can be selected. 0: Operates at resolution (T) = system clock cycle time (t_{cyc})

(5) Flowchart

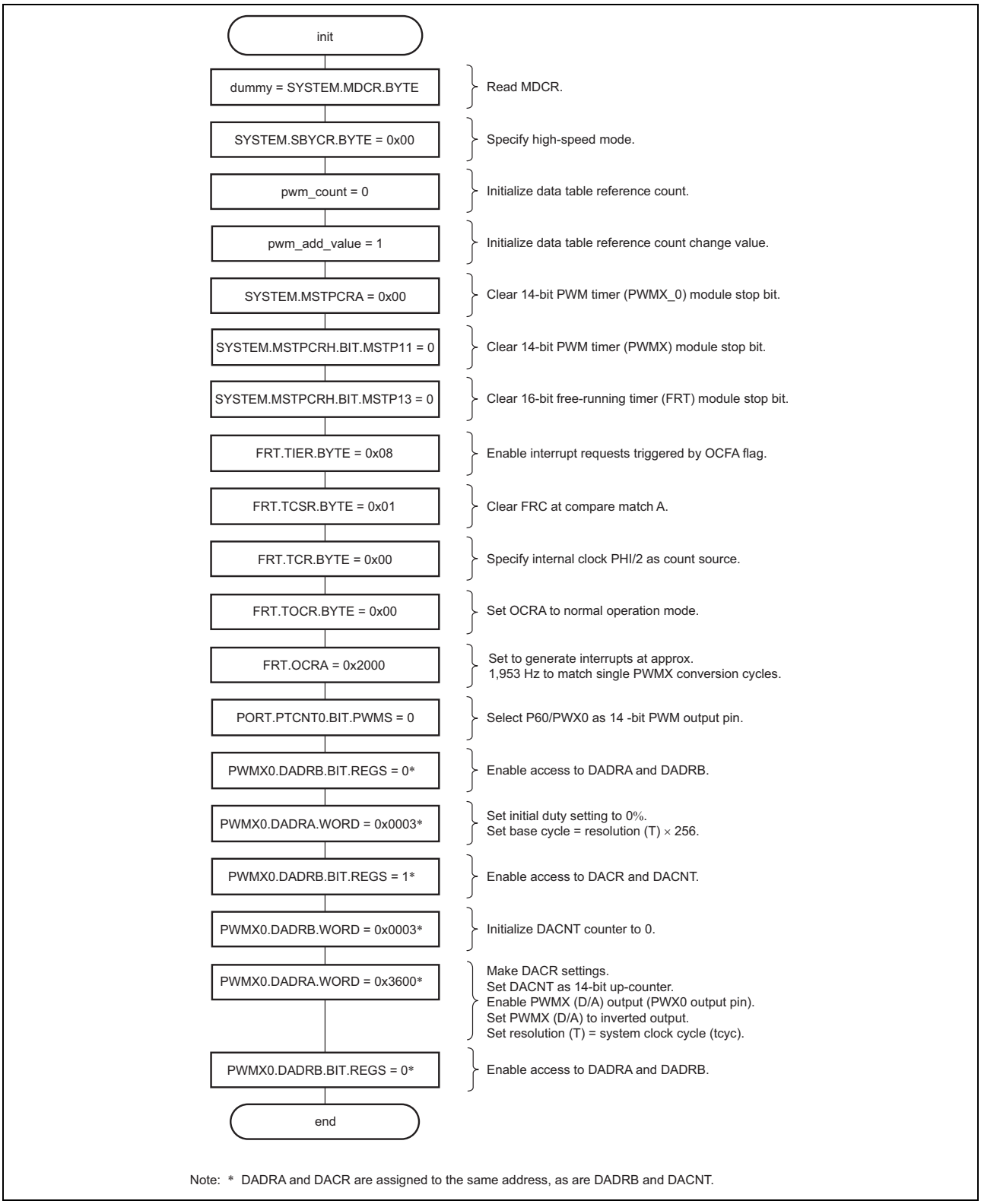


Figure 11 Initialization Flowchart (init)

5.5.4 INT_OCIA_FRT Function

(1) Functional Overview

The INT_OCIA_FRT function changes the PWMX output pulse duty.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

The internal I/O registers used by this function are shown below. Note that the setting values shown are those used in this application note and differ from the initial values.

- Timer Control/Status Register (TCSR) - Number of bits: 8, Address: H'FFFF91

Bit	Bit Name	Set Value	R/W	Descriptions
3	OCFA	0	R/(W)*	Output Compare Flag A Indicates that the FRC value matches the OCRA value. Only 0 can be written to clear the flag. [Setting condition] When FRC = OCRA [Clearing condition] Read OCFA when OCFA = 1, then write 0 to OCFA

Note: * Only 0 can be written to clear the flag.

- PWMX (D/A) Data Register A (DADRA) - Number of bits: 16, Address: H'FFFFA0

Bit	Bit Name	Set Value	R/W	Descriptions
15 to 2	DA13 to DA0	All 1	R/W	D/A Data 13 to 0 These bits set a digital value to be converted to an analog value. In each base cycle, the DACNT value is continually compared with the DADR value to determine the duty cycle of the output waveform, and to decide whether to output a fine-adjustment pulse equal in width to the resolution. To enable this operation, this register must be set within a range that depends on the CFS bit. If the DADR value is outside this range, the PWM output is held constant. A channel can be operated with 12-bit precision by fixing DA0 and DA1 to 0. The two data bits are not compared with UC12 and UC13 of DACNT.

(5) Flowchart

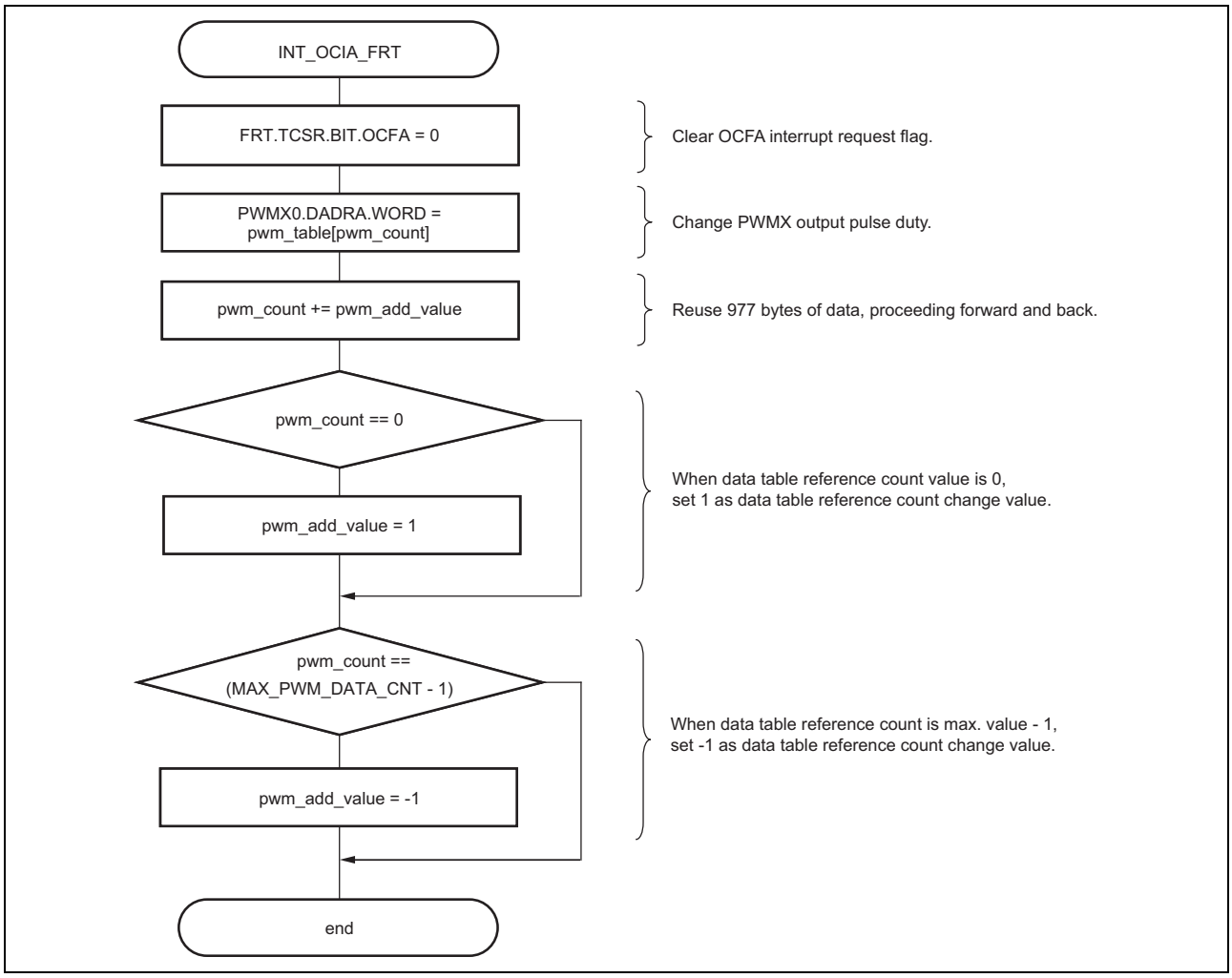


Figure 12 FRT OCIA Interrupt Flowchart (INT_OCIA_FRT)

6. Reference Documents

- Hardware Manual
  H8S/2472, H8S/2463, H8S/2462 Group Hardware Manual
  (The latest version can be downloaded from the Renesas Technology Web site.)
- Development Environment Manual
  H8S/300, H8/300 Series C/C++ Compiler Package User's Manual
  (The latest version can be downloaded from the Renesas Technology Web site.)
- Technical News/Technical Updates
  (The latest information can be downloaded from the Renesas Technology Web site.)

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