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H8S/2400 Series

EEPROM Connection Using Synchronous Serial Communication Unit

Introduction

This application note describes reading from and writing to externally connected SPI bus serial EEPROM by using the synchronous serial communication unit (SSU).

In SSU mode, the SSU uses a four-line bus comprising a clock line, data input line, data output line, and chip select line to implement data communication with the external device.

Target Devices

- H8S/2472, H8S/2463, H8S/2462 Group

Preface

This program can be used with other H8S Family MCUs that have the same internal I/O registers as the devices on which operation has been confirmed. Check the latest version of the manual for any additions and modifications to functions.

Careful evaluation is recommended before using this application note.

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1. Specifications

The specifications of this application note cover using the SSU to read and write 256 bytes of data from and to externally connected SPI bus serial EEPROM with a 256-byte capacity. The read operation accesses 256 bytes of data stored in the EEPROM starting at address H'00 and proceeds in ascending order. The write operation stores 256 bytes of data in the EEPROM at addresses H'00 to H'FF, starting from H'00 and proceeding in ascending order.

The detailed specifications for the operations described in this application note are listed below. Figure 1 shows an overview of the operations described in this application note.

- The SSU is set as the master device.
- The SSU is set to SSU mode and uses four pins to perform data communication: the clock output pin, data input pin, data output pin, and chip select output pin.
- The transfer clock rate of the SSU is set to the operating frequency divided by 16.
- The communication bit direction of the SSU is set to MSB first.
- The data latch timing of the SSU is set to clock first falling edge.
- The SSU's transmit and receive data length varies according to the number of bytes required by the EEPROM instruction code.
- Chip select (\overline{S}) signals are output to the EEPROM from an I/O port for read and write operations and from the \overline{SCS} pin of the SSU otherwise.

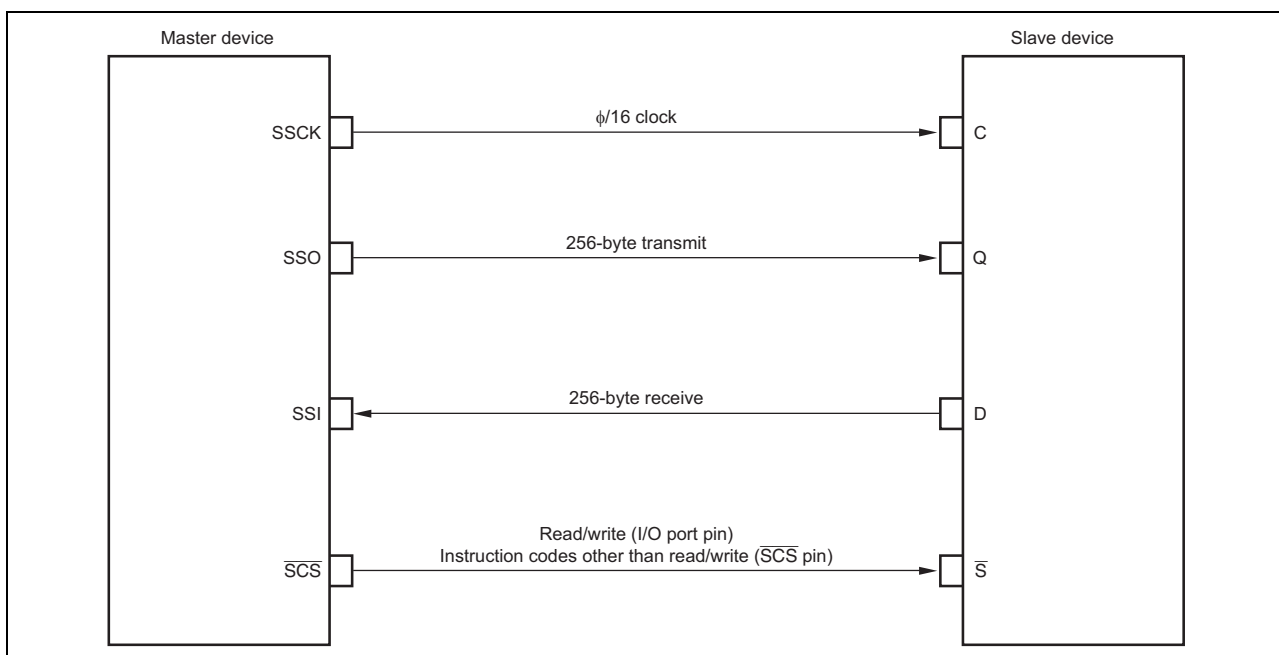


Figure 1 Operation Overview

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Description
Operating frequency	Input clock: 8.0 MHz System clock (ϕ): 32 MHz (8.0 MHz multiplied by 4*)
Operating voltage	3.3 V
Operating mode	Mode 2 = ($\overline{MD2} = 1, MD1 = 1$)
Evaluation board	Renesas Technology ROK402472D000BR
EEPROM	Renesas Technology HN58X2502I
Integrated development environment	High-performance Embedded Workshop (HEW) Ver.4.04.01.001
C/C++ compiler	Renesas Technology H8S,H8/300 C/C++ Compiler (V.6.02.00)
Compile options	-cpu = 2600A: 24, -optimize = 1
Optimizing linkage editor	Renesas Technology Optimizing Linkage Editor (V9.03.00)
Linker options	start = PResetPRG,PIntPRG/0400, P,C,C\$DSEC,C\$BSEC,D/0800, B,R/OFF0800, S/OFFEE00

Note: * The PLL multiplier circuit multiplies the externally input clock by 4.

3. Functions Used

The synchronous serial communication unit (SSU) supports master mode, in which the MCU functions as the master device and outputs a clock to an external device for synchronous serial communication, and slave mode, in which the clock is input from an external device for synchronous serial communication. Synchronous serial communication is also possible between devices using different clock polarities or clock phases.

3.1 Transfer Clock

A transfer clock can be selected from eight internal clocks and an external clock. To use this module, it is first necessary to set the SCKS bit in SS control register H (SSCRH) to 1 to select the SSCK pin as the serial clock. When the MSS bit in SSCRH is 1, an internal clock is selected and the SSCK pin is used as an output pin. When transfer is started, the clock with the transfer rate set by bits CKS2 to CKS0 in the SS mode register (SSMR) is output from the SSCK pin. When MSS = 0, an external clock is selected and the SSCK pin is used as an input pin.

3.2 Relationship of Clock Phase, Polarity, and Data

When the SSUMS bit in SS control register L (SSCRL) is cleared to 0, the relationship of clock phase, polarity, and transfer data depends on the combination of the CPOS and CPHS bits in SSMR. Figure 2 shows the relationship. When SSUMS = 1, the CPHS setting is invalid although the CPOS setting is valid.

Setting the MLS bit in SSMR selects that MSB or LSB first communication. When MLS = 0, data is transferred from the LSB to the MSB. When MLS = 1, data is transferred from the MSB to the LSB.

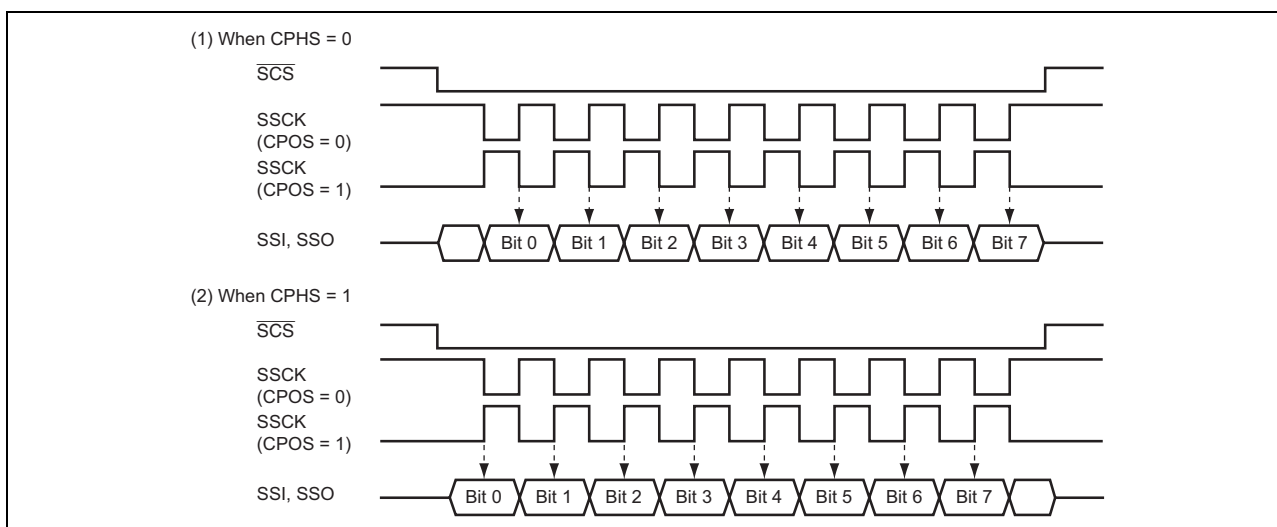


Figure 2 Relationship of Clock Phase, Polarity, and Data

3.3 SSU Mode

In SSU mode, data communications are performed via four lines: clock line (SSCK), data input line (SSI or SSO), data output line (SSI or SSO), and chip select line (\overline{SCS}).

In addition, the SSU supports bidirectional mode in which a single pin functions as data input and data output lines.

(1) Initial Settings in SSU Mode

Before transmitting or receiving data, clear the TE and RE bits in the SS enable register (SSER) 0 to set the initial values.

Note: Before changing operating modes and communications formats, clear both the TE and RE bits to 0. Although clearing the TE bit to 0 sets the TDRE bit to 1, clearing the RE bit to 0 does not change the values of the RDRF and ORER bits and SSRDR. Those bits retain the previous values.

(2) Data Transmission

Figure 3 shows an example of transmission operation. When transmitting data, the SSU operates as shown below.

In master mode, the SSU outputs a transfer clock and data. In slave mode, when a low level signal is input to the \overline{SCS} pin and a transfer clock is input to the SSCK pin, the SSU outputs data in synchronization with the transfer clock.

Writing transmit data to the SS transmit data register SSTDR after setting the TE bit in SSER to 1 automatically clears the TDRE bit in the SS status register (SSSR) to 0, and causes the SSU to transfer data from SSTDR to the SS shift register (SSTRSR).

When 1-frame data has been transferred with TDRE = 0, the SSTDR contents are transferred to SSTRSR to start the next frame transmission. When the 8th bit of transmit data has been transferred with TDRE = 1, the TEND bit in SSSR is set to 1 and the state is retained. At this time, if the TEIE bit is set to 1, a TEI interrupt is generated. After transmission, the output level of the SSCK pin is fixed high when CPOS = 0 and low when CPOS = 1.

While the ORER bit in SSSR is set to 1, transmission is not performed. Check that the ORER bit is cleared to 0.

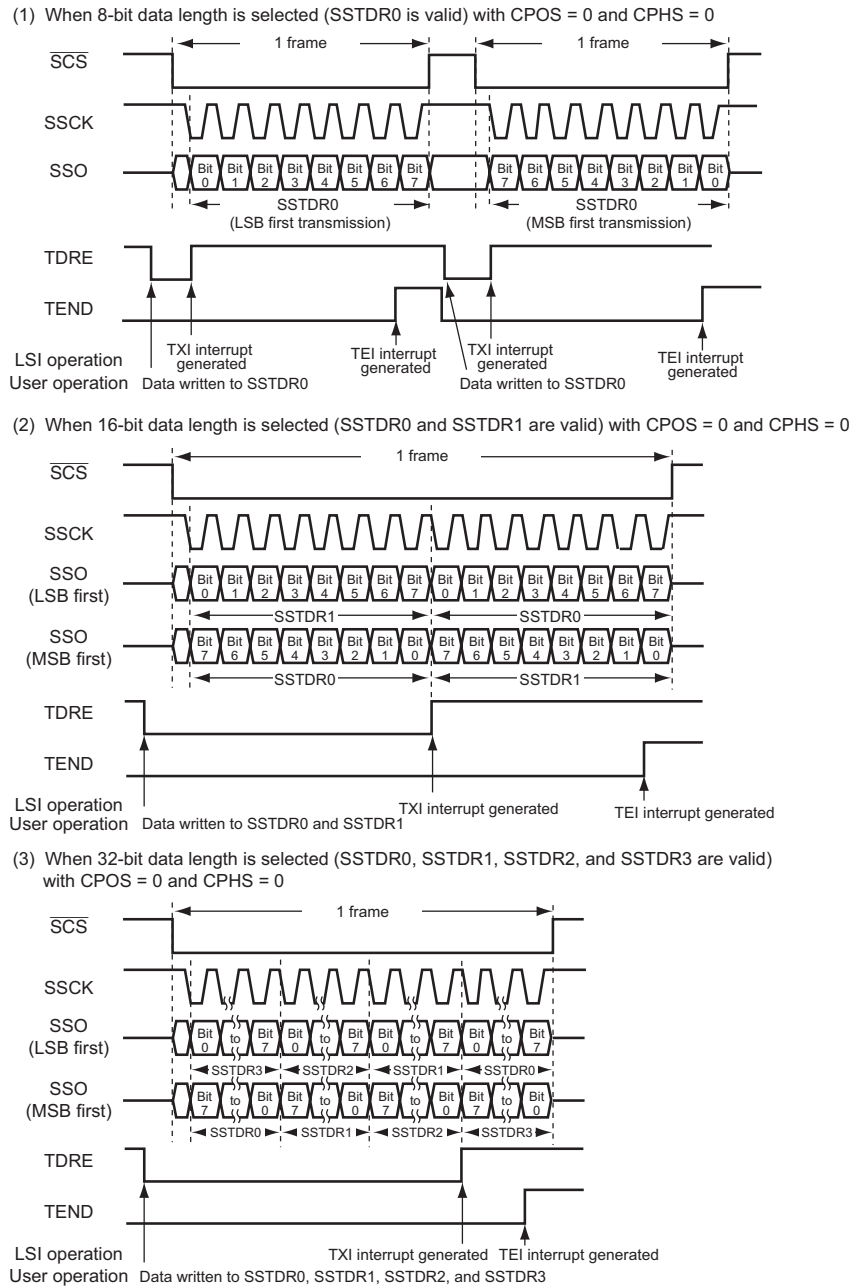


Figure 3 Example of Transmission Operation (SSU Mode)

(3) Data Reception

Figure 4 shows an example of reception operation. When receiving data, the SSU operates as shown below.

After setting the RE bit to 1 and dummy-reading SSRDR, the SSU starts data reception.

In master mode, the SSU outputs a transfer clock and receives data. In slave mode, when a low level signal is input to the $\overline{\text{SCS}}$ pin and a transfer clock is input to the SSCK pin, the SSU receives data in synchronization with the transfer clock.

When 1-frame data has been received, the RDRF bit in SSSR is set to 1 and the receive data is stored in SSRDR. At this time, if the RIE bit in SSER is set to 1, an RXI interrupt is generated. The RDRF bit is automatically cleared to 0 by reading SSRDR.

When the RDRF bit has been set to 1 at the 8th rising edge of the transfer clock, the ORER bit in SSSR is set to 1. This indicates that an overrun error (OEI) has occurred. At this time, data reception is stopped. While the ORER bit in SSSR is set to 1, reception is not performed. To resume the reception, clear the ORER bit to 0.

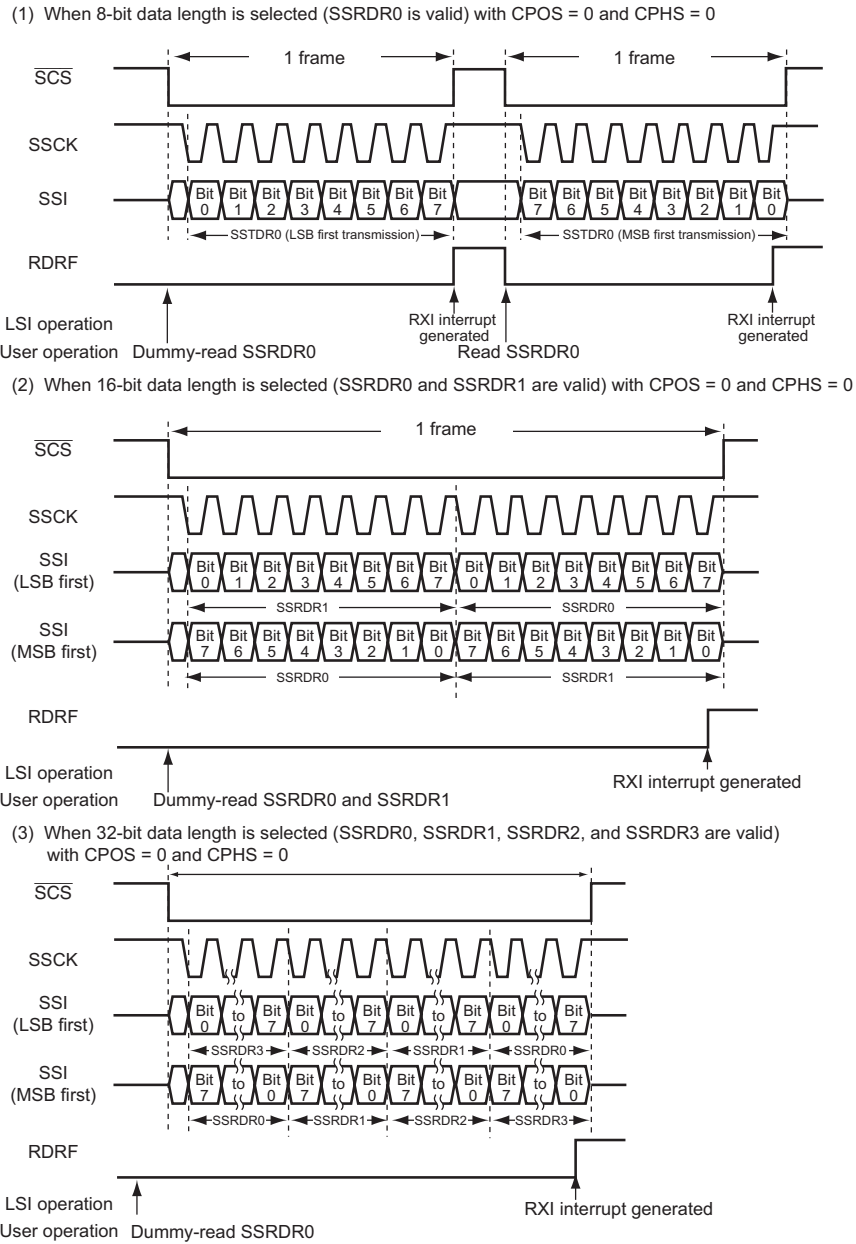


Figure 4 Example of Reception Operation (SSU Mode)

4. Operation

The EEPROM instruction codes used in this application note are listed below. The operation of the individual instructions is shown in figures 5 to 9.

Table 2 EEPROM instruction codes

No.	Instruction	Description	Instruction Format
1.	WRSR	Write status register	0000 X001
2.	RDSR	Read status register	0000 X101
3.	WREN	Write enable	0000 X110
4.	WRITE	Write to memory array	0000 A010
5.	READ	Read from memory array	0000 A011

Note: X stands for any value. A stands for A8 in the case of the HN58X2504I.

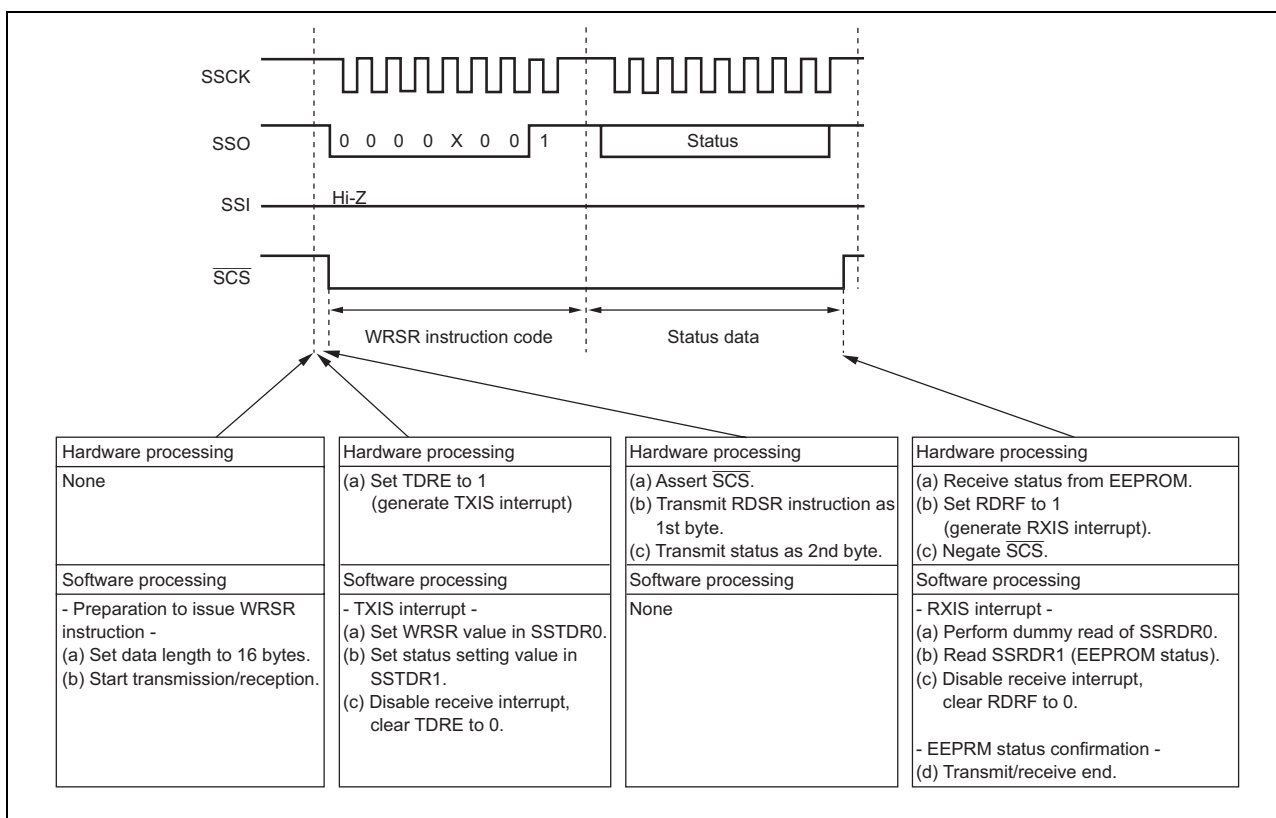


Figure 5 1. WRSR Operation

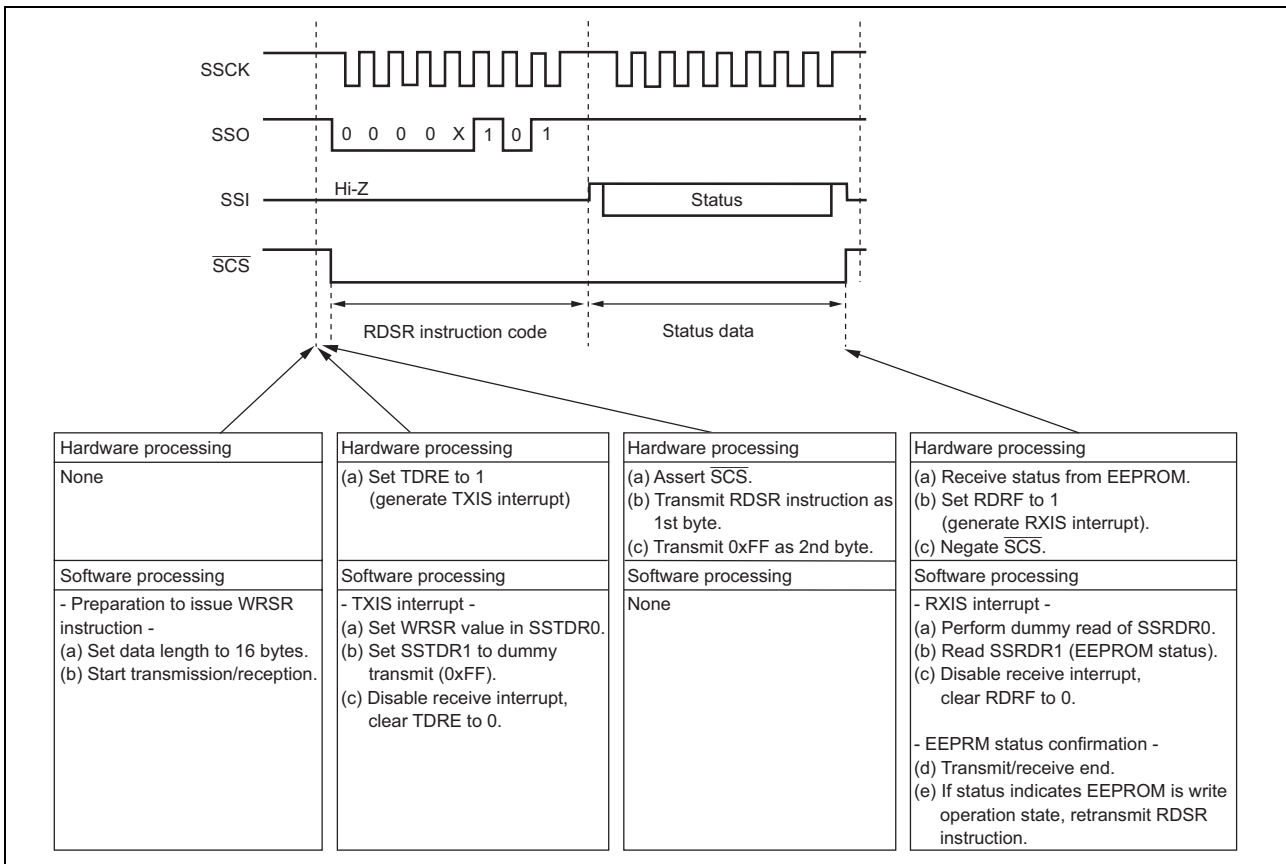


Figure 6 2. RDSR Operation

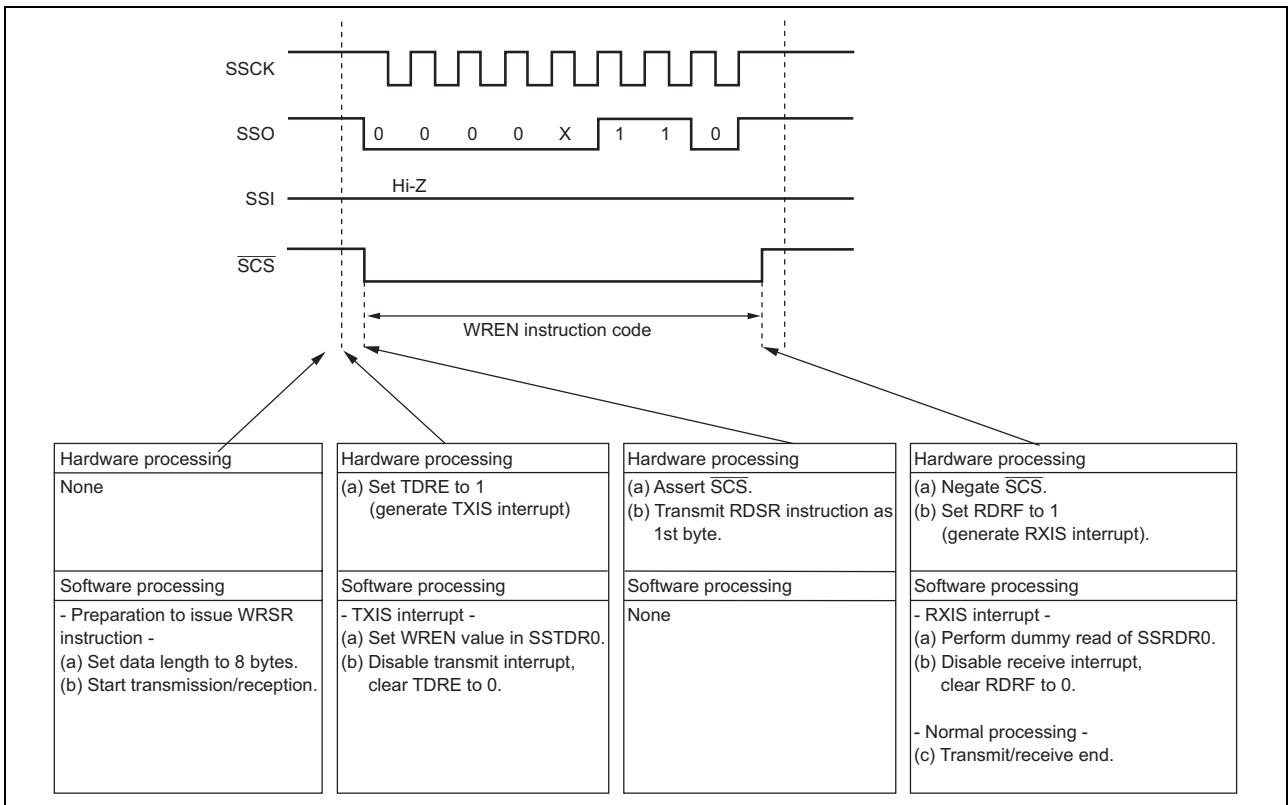


Figure 7 3. WREN Operation

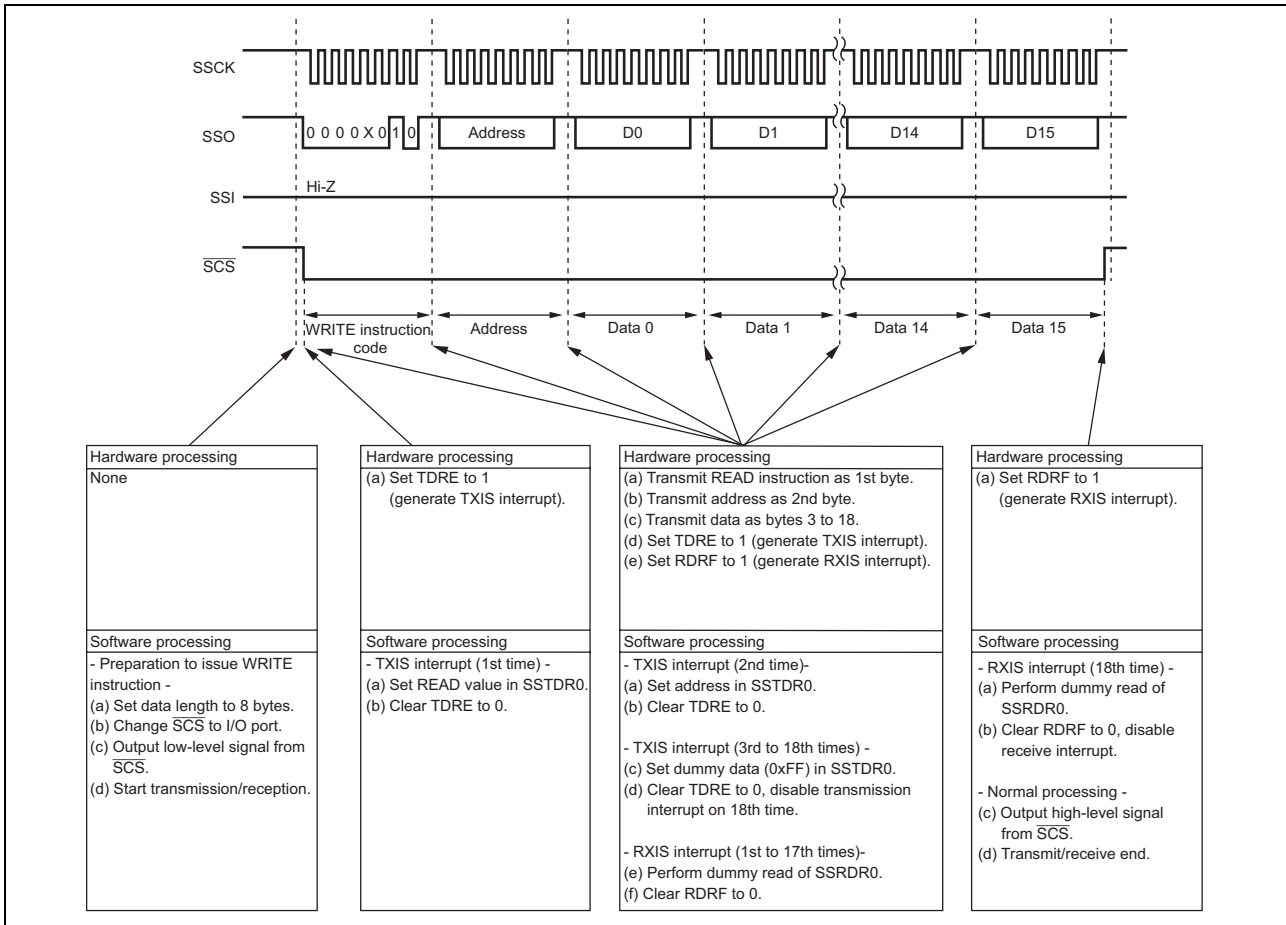


Figure 8 4. WRITE Operation

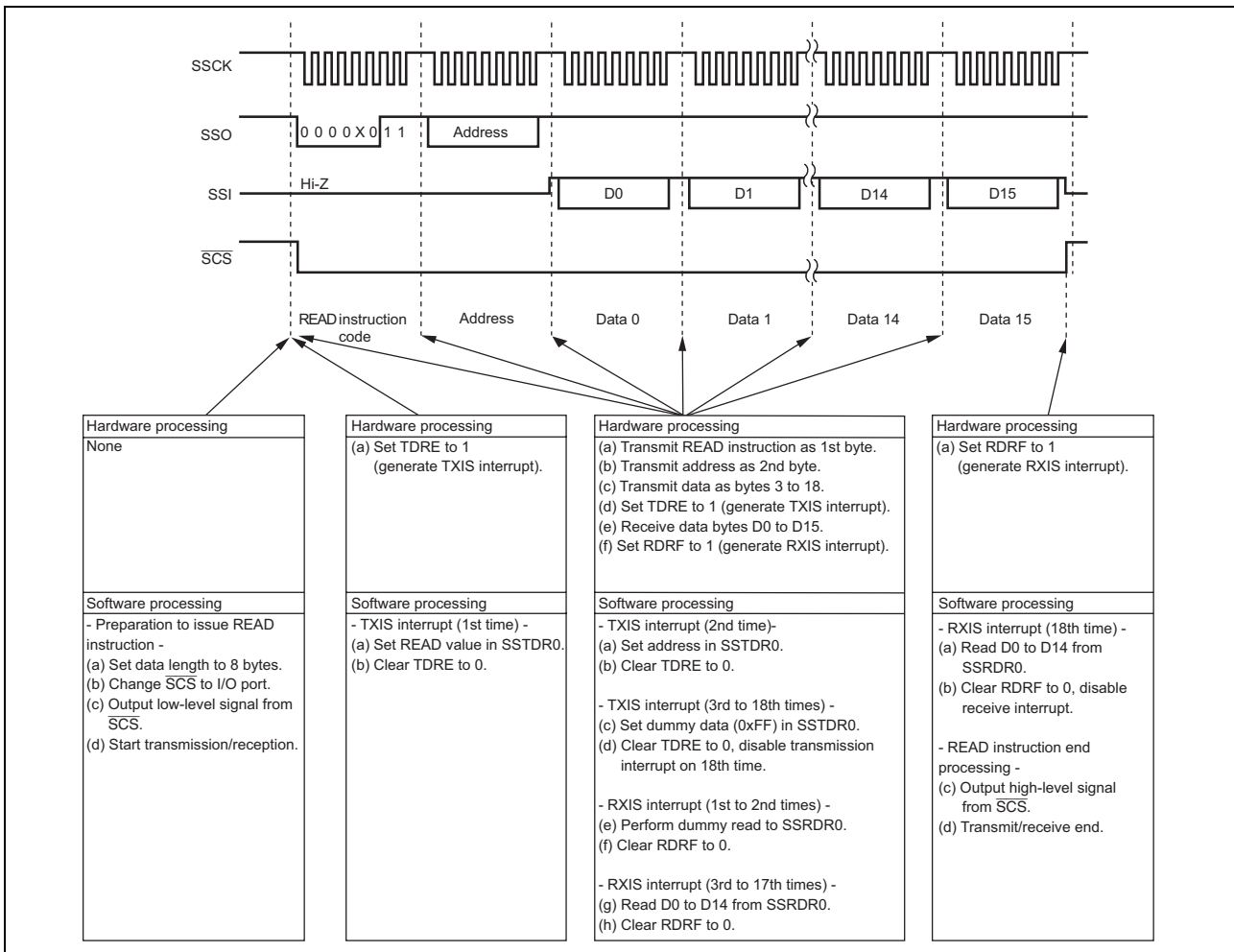


Figure 9 5. READ Operation

As examples, figure 10 shows operation when setting the EEPROM status register, figure shows operation when writing 16 bytes of data to the EEPROM, and figure 12 shows operation when reading 16 bytes of data from the EEPROM.

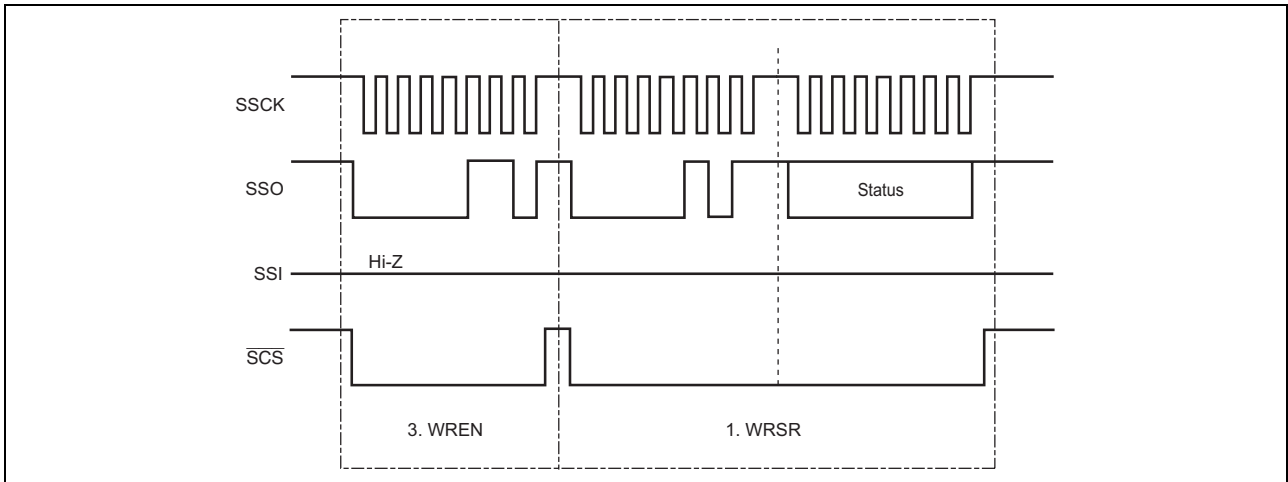


Figure 10 Status Register Setting Operation

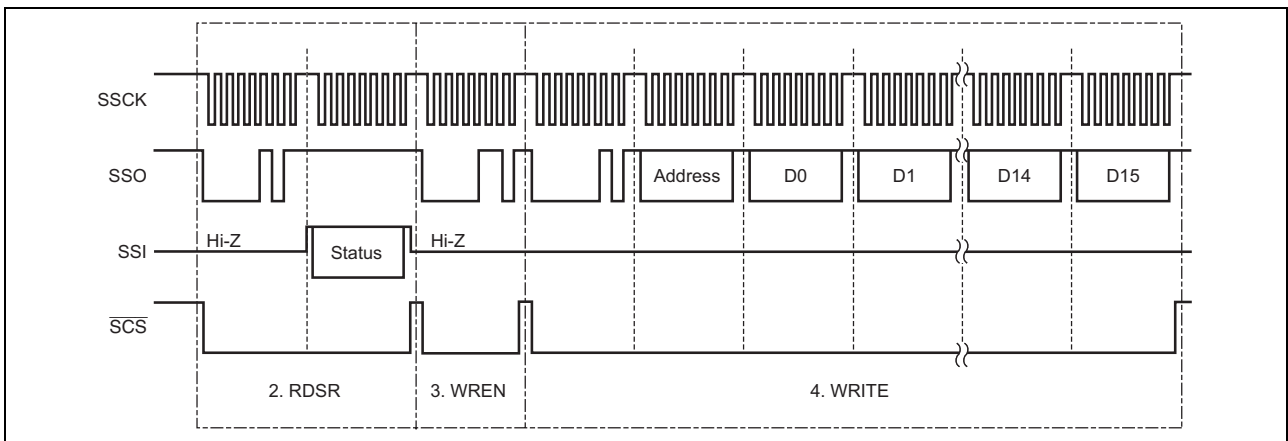


Figure 11 Data Write Overall Operation

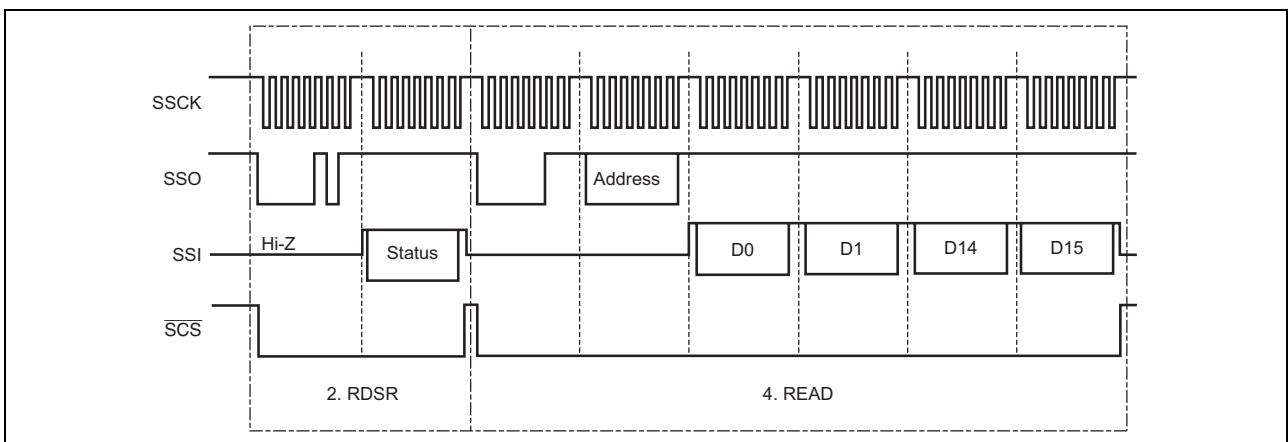


Figure 12 Data Read Overall Operation

5. Functions

5.1 Symbolic Constants

Table 3 List of Symbolic Constants

Constant Name	Set Value	Description	Used by Functions
EEPROM_SIZE	256	EEPROM data capacity size	main init
EEPROM_PAGESIZE	16	EEPROM page size	main
COMMAND_WRSR	0x01	EEPROM WRSR instruction code value	command_WRSR INT_RXIS_SSU INT_TXIS_SSU
COMMAND_RDSR	0x05	EEPROM RDSR instruction code value	command_RDSR INT_RXIS_SSU INT_TXIS_SSU
COMMAND_WREN	0x06	EEPROM WREN instruction code value	command_WREN INT_RXIS_SSU INT_TXIS_SSU
COMMAND_WRITE	0x02	EEPROM WRITE instruction code value	command_WRITE INT_RXIS_SSU INT_TXIS_SSU
COMMAND_READ	0x03	EEPROM READ instruction code value	command_READ INT_RXIS_SSU INT_TXIS_SSU
ACCESS_START	0x00	EEPROM access start	command_WRSR command_RDSR command_WREN command_WRITE command_READ
ACCESS_END	0x01	EEPROM access end	command_WRSR command_RDSR command_WREN command_WRITE command_READ INT_RXIS_SSU INT_TXIS_SSU

5.2 ROM Variables

Type	Variable Name	Set Value	Description	Used by Functions
const unsigned char	write_data[EEPROM_SIZE]	0x00, 0x01, 0x02, ..., ..., 0xFD, 0xFE, 0xFF	Data to be written to EEPROM	main

5.3 RAM Variables

Table 6 List of RAM Variables

Type	Variable Name	Set Value	Description	Used by Functions
unsigned char	read_data[EEPROM_SIZE]	All initialized to 0x00	Storage of data read from EEPROM	main init
unsigned char	eprom_command	0x00	Issue command storage	init command_WRSR command_RDSR command_WREN command_WRITE command_READ INT_RXIS_SSU INT_TXIS_SSU
unsigned char	eprom_state	0x00	EEPROM access state	init command_WRSR command_RDSR command_WREN command_WRITE command_READ INT_RXIS_SSU INT_TXIS_SSU
unsigned int	eprom_address	0x00	Write destination/ read source address storage	init command_WRITE command_READ INT_RXIS_SSU INT_TXIS_SSU
unsigned int	eprom_size	0x00	Write/read size storage	init command_WRITE command_READ INT_RXIS_SSU INT_TXIS_SSU
unsigned char *	eprom_data	0x00	Write/read data storage destination pointer	init command_WRITE command_READ INT_RXIS_SSU INT_TXIS_SSU
unsigned char	eprom_status	0x00	EEPROM status storage	init command_WRSR command_RDSR INT_RXIS_SSU INT_TXIS_SSU

Type	Variable Name	Set Value	Description	Used by Functions
unsigned int	eeeprom_transmit_cnt	0x00	Transmit counter	init command_WRSR command_RDSR command_WREN command_WRITE command_READ INT_RXIS_SSU INT_TXIS_SSU
unsigned int	eeeprom_receive_cnt	0x00	Receive counter	init command_WRSR command_RDSR command_WREN command_WRITE command_READ INT_RXIS_SSU INT_TXIS_SSU

5.4 List of Functions

Table 7 List of Functions

Function Name	Descriptions
PowerON_Reset	<ul style="list-style-type: none"> Initial settings function Initializes status pointer (SP), sets interrupt mask bits, sets uninitialized/initialized data, calls main function.
main	<ul style="list-style-type: none"> Main function Calls init and init_eeeprom functions, writes data to and reads data from EEPROM.
init	<ul style="list-style-type: none"> I/O register initialization function Initializes registers.
eeeprom_init	<ul style="list-style-type: none"> EEPROM initialization function Makes EEPROM status register settings.
eeeprom_write	<ul style="list-style-type: none"> EEPROM write function Writes data to EEPROM.
eeeprom_read	<ul style="list-style-type: none"> EEPROM read function Reads data from EEPROM.
command_WRSR	<ul style="list-style-type: none"> WRSR instruction code issue function Transmits WRSR instruction code, transmits status register value.
command_RDSR	<ul style="list-style-type: none"> RDSR instruction code issue function Transmits RDSR instruction code, receives status register value.
command_WREN	<ul style="list-style-type: none"> WREN instruction code issue function Transmits WREN instruction code.
command_WRITE	<ul style="list-style-type: none"> WRITE instruction code issue function Transmits WRITE instruction code, address, and data.
command_READ	<ul style="list-style-type: none"> READ instruction code issue function Transmits READ instruction code and address, receives data.

5.5 Functions

5.5.1 PowerON_Reset Function

(1) Functional Overview

The PowerON_Reset function initializes the status pointer (SP) and uses embedded functions and standard library functions to set interrupt mask bits and set uninitialized/initialized data. Then it calls the main function.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

None

(5) Flowchart

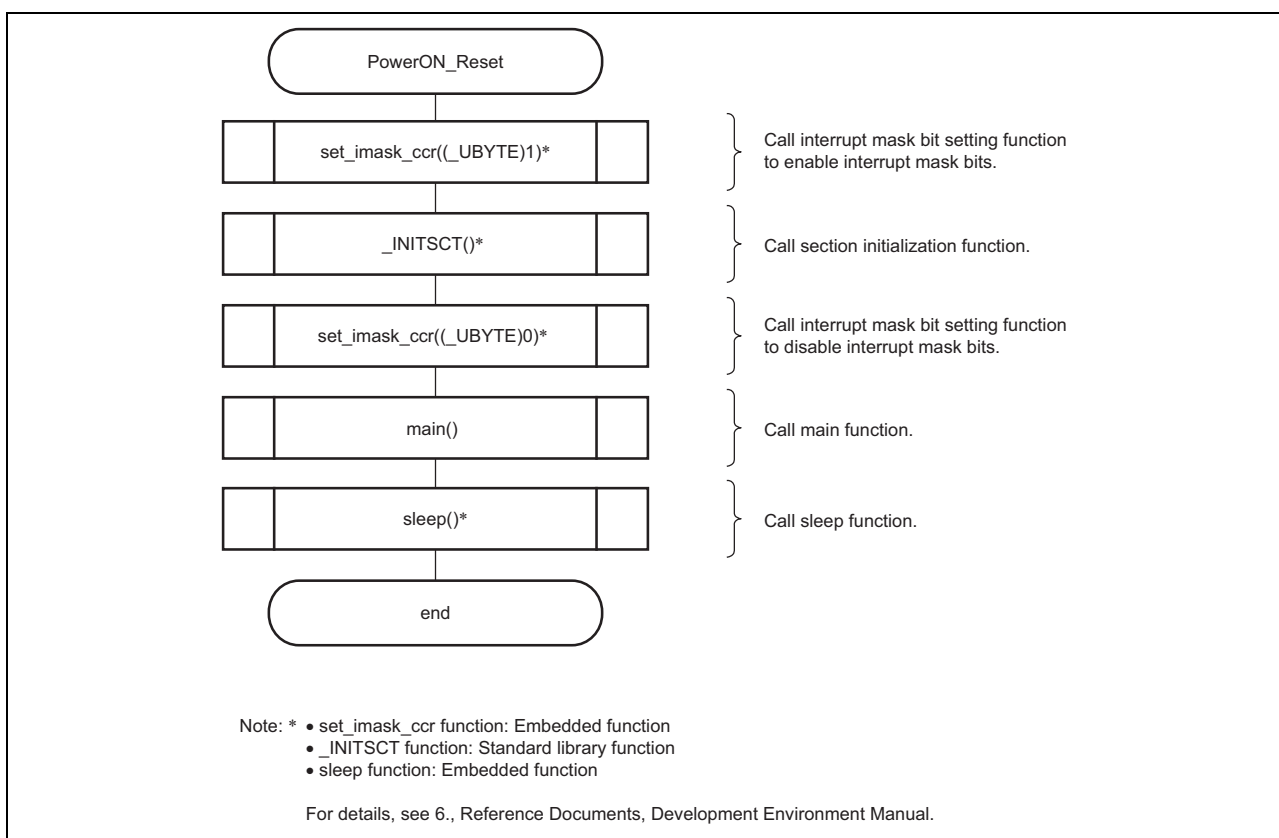


Figure 13 Power-On Reset Flowchart (PowerON_Reset)

5.5.2 main Function

(1) Functional Overview

The main function calls the init function, initializes registers, and reads from/writes to the EEPROM.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

None

(5) Flowchart

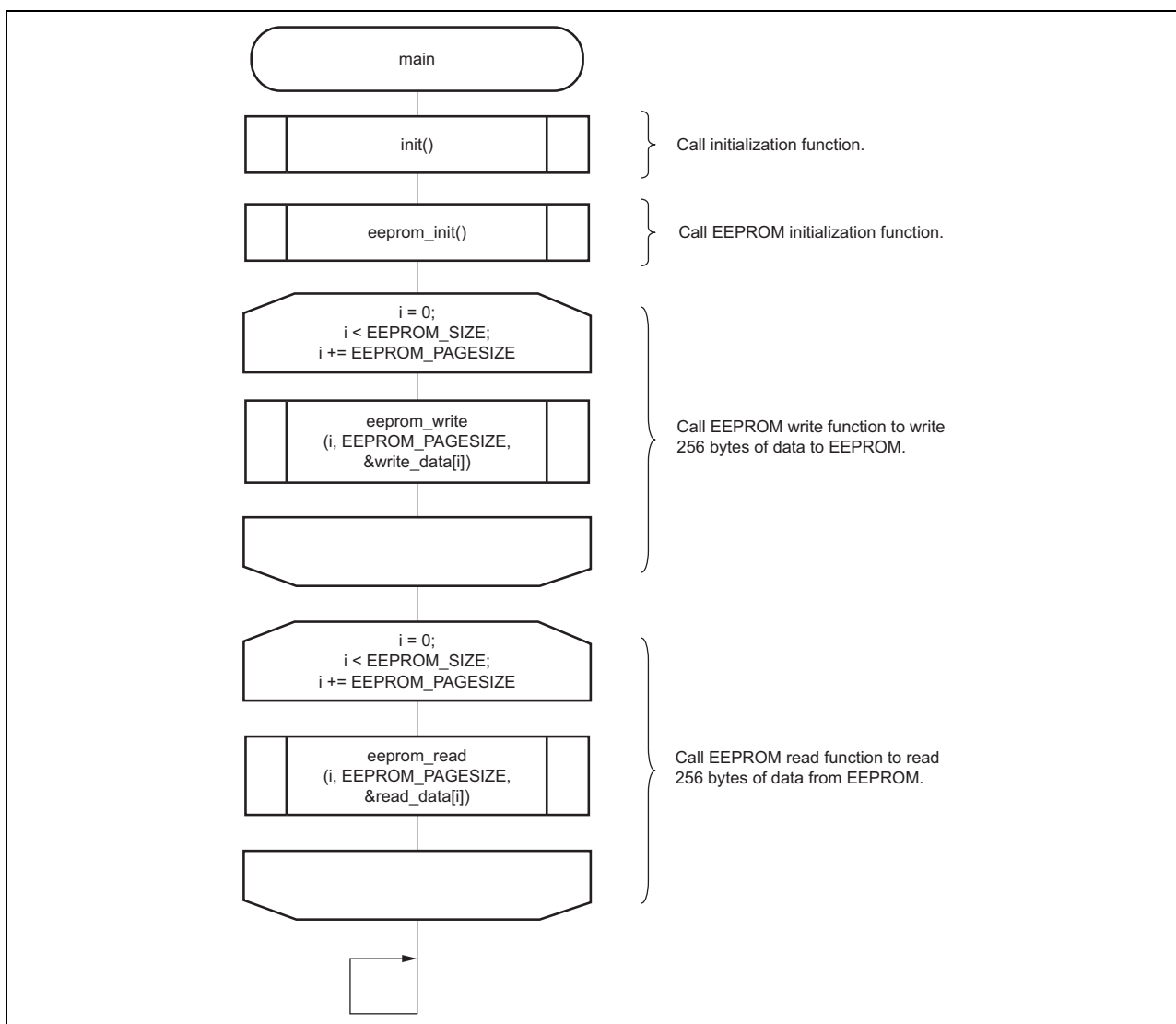


Figure 14 Main Flowchart (main)

5.5.3 init Function

(1) Functional Overview

The init function initializes various registers.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

The internal I/O registers used by this function are shown below. Note that the setting values shown are those used in this application note and differ from the initial values.

- Mode Control Register (MDCR) Number of bits: 8 Address: H'FFFFC5

Bit	Bit Name	Set Value	R/W	Description
2	MDS2	—	R	Mode Select 2 and 1
1	MDS1	—	R	These bits indicate the input levels at the mode pins (MD2 and MD1) (the current operating mode). Bits MDS2 and MDS1 correspond to the MD2 and MD1 pins, respectively. MDS2 and MDS1 are read-only bits and writing to them has no effect. The mode pin (MD2 and MD1) input levels are latched into these bits when MDCR is read. These latches are canceled by a reset.

- Standby Control Register (SBYCR) Number of bits: 8 Address: H' FFFF84

Bit	Bit Name	Set Value	R/W	Description
2	SCK2	0	R/W	System Clock Select
1	SCK1	0	R/W	These bits select the clock for the bus master in high-speed mode and medium-speed mode. 000: High-speed mode
0	SCK0	0	R/W	

- SUBMSTPBL causes on-chip peripheral modules to shift to module stop mode in module units. Each module can be set to module stop mode by setting the corresponding bit to 1.

- Sub-Chip Module Stop Control Register BL (SUBMSTPBL) Number of bits: 8 Address: H'FFFE3F

Bit	Bit Name	Set Value	R/W	Description
2	SMSTPB2	0	R/W	Synchronous serial communication unit (SSU)

- Port 6 Data Register (P6DR) Number of bits: 8 Address: H'FFFFBB

Bit	Bit Name	Set Value	R/W	Description
6	P66DR	1	R/W	This bit stores output data for a pin used as a general output port. When this register is read, the values for bits in P6DR corresponding to bits set to 1 in P6DDR are read, and for bits corresponding to bits cleared to 0 in P6DDR the pin states are read.

- Port 6 Data Direction Register (P6DDR) Number of bits: 8 Address: H'FFFFB9

Bit	Bit Name	Set Value	R/W	Description
6	P6DDR	1	W	When the general I/O port function is selected, the corresponding pin functions as an output port when this bit is set to 1 and as an input port when this bit is cleared to 0.

- SS Enable Register (SSER) Number of bits: 8 Address: H'FFFCC3

Bit	Bit Name	Set Value	R/W	Description
7	TE	0	R/W	Transmit Enable When this bit is set to 1, transmission is enabled.
6	RE	0	R/W	Receive Enable When this bit is set to 1, reception is enabled.
2	TIE	0	R/W	Transmit Interrupt Enable When this bit is set to 1, a TXI interrupt request is enabled.
1	RIE	0	R/W	Receive Interrupt Enable When this bit is set to 1, an RXI interrupt request and an OEI interrupt request are enabled.

- SS Control Register H (SSCRH) Number of bits: 8 Address: H'FFFCC0

Bit	Bit Name	Set Value	R/W	Description
7	MSS	1	R/W	<p>Master/Slave Device Select</p> <p>Selects that this module is used in master mode or slave mode. When master mode is selected, transfer clocks are output from the SSCK pin. When the CE bit in SSSR is set, this bit is automatically cleared.</p> <p>1: Master mode is selected.</p>
6	BIDE	0	R/W	<p>Bidirectional Mode Enable</p> <p>Selects that both serial data input pin and output pin are used or one of them is used. However, transmission and reception are not performed simultaneously when bidirectional mode is selected.</p> <p>0: Standard mode (two pins are used for data input and output)</p>
4	SOL	1	R/W	<p>Serial Data Output Value Select</p> <p>The serial data output retains its level of the last bit after completion of transmission. The output level before or after transmission can be specified by setting this bit. When specifying the output level, use the MOV instruction after clearing the SOLP bit to 0. Since writing to this bit during data transmission causes malfunctions, this bit should not be changed.</p> <p>1: Serial data output is changed to high.</p>
3	SOLP	1	R/W	<p>SOL Bit Write Protect</p> <p>When changing the output level of serial data, set the SOL bit to 1 or clear the SOL bit to 0 after clearing the SOLP bit to 0 using the MOV instruction. This bit is always read as 1.</p> <p>1: Output level cannot be changed by the SOL bit.</p>

- SS Control Register L (SSCRL) Number of bits: 8 Address: H'FFFCC1

Bit	Bit Name	Set Value	R/W	Description
6	SSUMS	0	R/W	<p>Selects transfer mode from SSU mode and clock synchronous mode.</p> <p>0: SSU mode</p>

- SS Mode Register (SSMR) Number of bits: 8 Address: H'FFFCC2

Bit	Bit Name	Set Value	R/W	Description
7	MLS	1	R/W	MSB First/LSB First Select Selects that the serial data is transmitted in MSB first or LSB first. 1: MSB first
6	CPOS	1	R/W	Clock Polarity Select Selects the SSCK clock polarity. 1: Low output in idle mode, and high output in active mode
5	CPHS	1	R/W	Clock Phase Select (Only for SSU Mode) Selects the SSCK clock phase. 1: Data is latched at the first edge.
2	CKS2	0	R/W	Transfer Clock Rate Select
1	CKS1	1	R/W	Select the transfer clock rate (prescaler division rate) when an internal clock is selected.
0	CKS0	1	R/W	011: $\phi/16$

- SS Control Register 2 (SSCR2) Number of bits: 8 Address: H'FFFCC5

Bit	Bit Name	Set Value	R/W	Description
7	SDOS	0	R/W	Serial Data Pin Open Drain Select Selects whether the serial data output pin is used as a CMOS or an NMOS open drain output. Pins to output serial data differ according to the register setting. 0: CMOS output
6	SSCKOS	0	R/W	SSCK Pin Open Drain Select Selects whether the SSCK pin is used as a CMOS or an NMOS open drain output. 0: CMOS output
5	SCSOS	0	R/W	SCS Pin Open Drain Select Selects whether the SCS pin is used as a CMOS or an NMOS open drain output. 0: CMOS output
4	TENDSTS	0	R/W	Selects the timing of setting the TEND bit (valid in SSU and master mode). 0: Sets the TEND bit when the last bit is being transmitted
3	SCSATS	0	R/W	Selects the assertion timing of the SCS pin (valid in SSU and master mode). 0: Min. values of t_{LEAD} and t_{LAG} are $1/2 \times t_{SUcyc}$
2	SSODTS	0	R/W	Selects the data output timing of the SSO pin (valid in SSU and master mode) 0: While BIDE = 0, MSS = 1, and TE = 1 or while BIDE = 1, TE = 1, and RE = 0, the SSO pin outputs data

(5) Flowchart

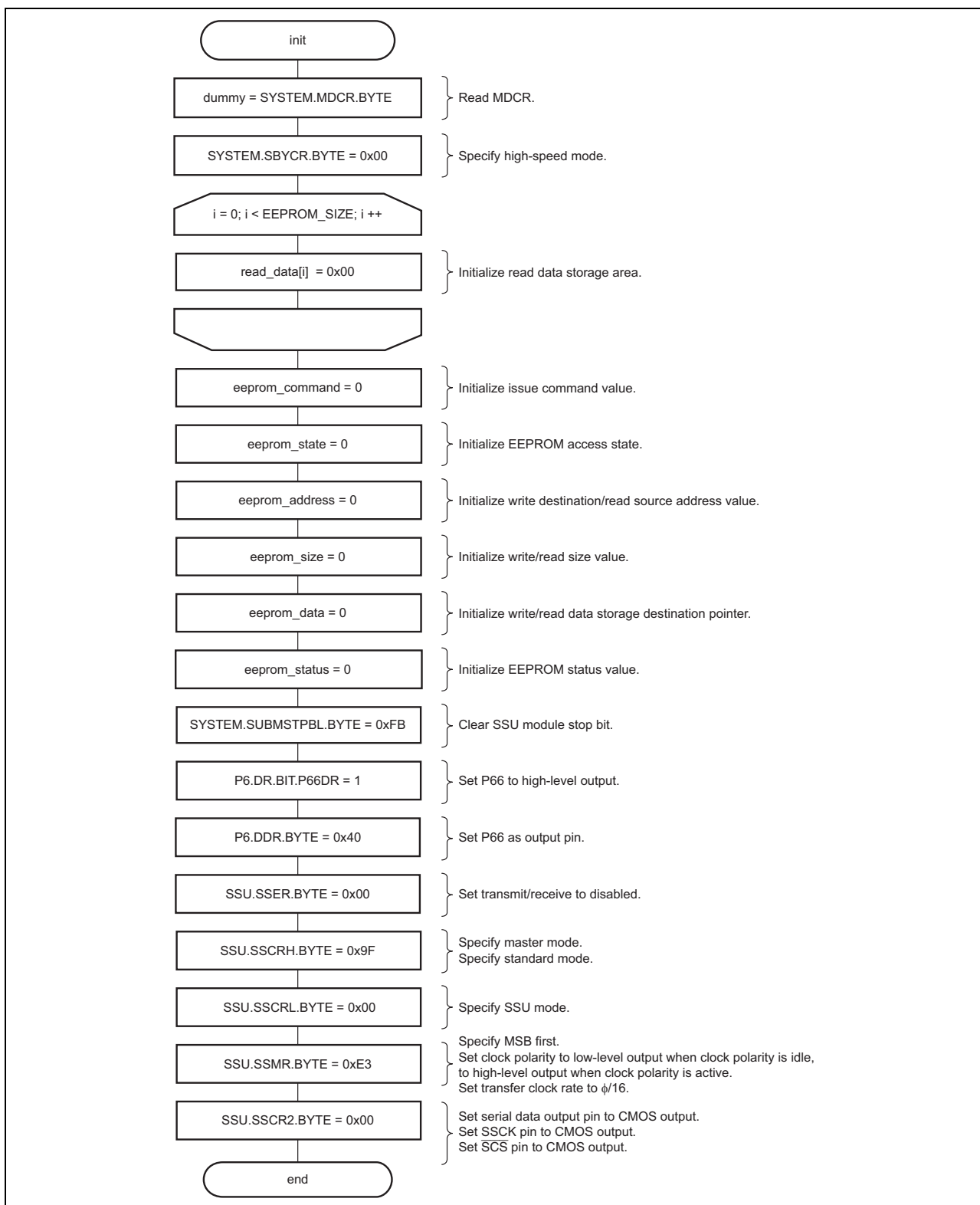


Figure 15 Initialization Flowchart (init)

5.5.4 eeprom_init Function

(1) Functional Overview

The eeprom_init function initializes the EEPROM status register.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

None

(5) Flowchart

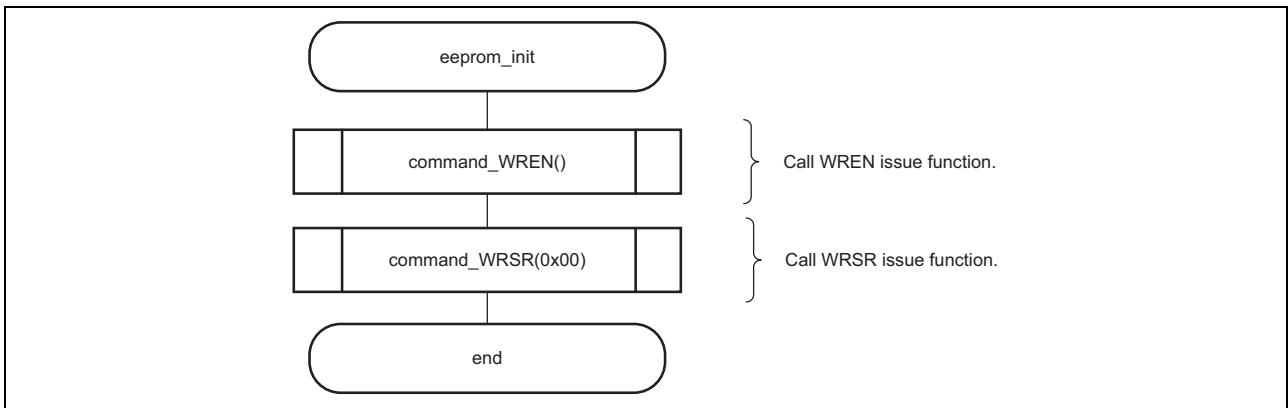


Figure 16 EEPROM Initialization Flowchart (eeprom_init)

5.5.5 eeprom_write Function

(1) Functional Overview

The eeprom_write function writes data to the EEPROM based on the values specified in the arguments.

(2) Arguments

Argument	Type	Argument Name	Setting	Description
1st argument	unsigned int	address	—	Specifies the write destination address.
2 nd argument	unsigned int	size	—	Specifies the write size.
3rd argument	unsigned char*	data	—	Specifies the write data storage destination pointer.

(3) Returned values

None

(4) Description of internal I/O registers used

None

(5) Flowchart

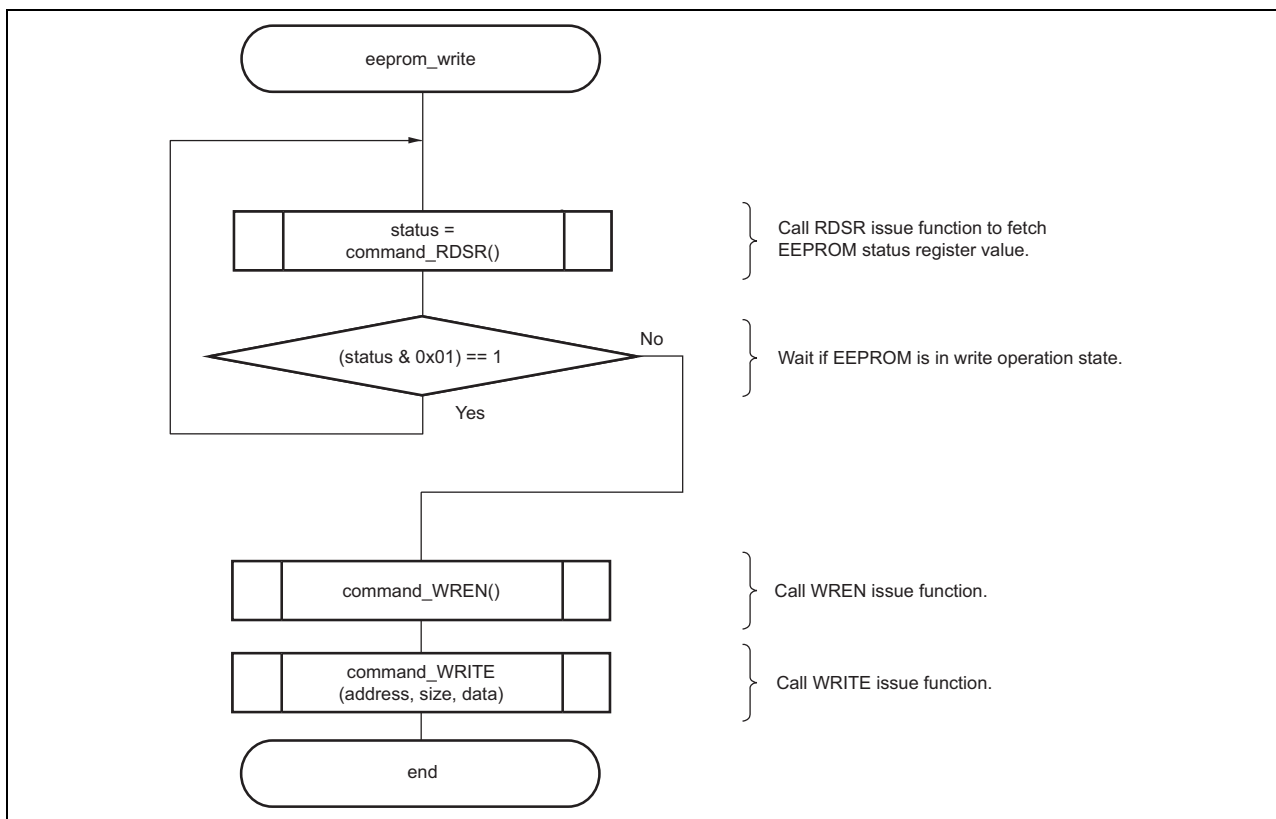


Figure 17 EEPROM Write Flowchart (eeprom_write)

5.5.6 eeprom_read Function

(1) Functional Overview

The eeprom_read function reads data from the EEPROM based on the values specified in the arguments.

(2) Arguments

Argument	Type	Argument Name	Setting	Description
1st argument	unsigned int	address	—	Specifies the read source address.
2nd argument	unsigned int	size	—	Specifies the read size.
3rd argument	unsigned char*	data	—	Specifies the read data storage destination pointer.

(3) Returned values

None

(4) Description of internal I/O registers used

None

(5) Flowchart

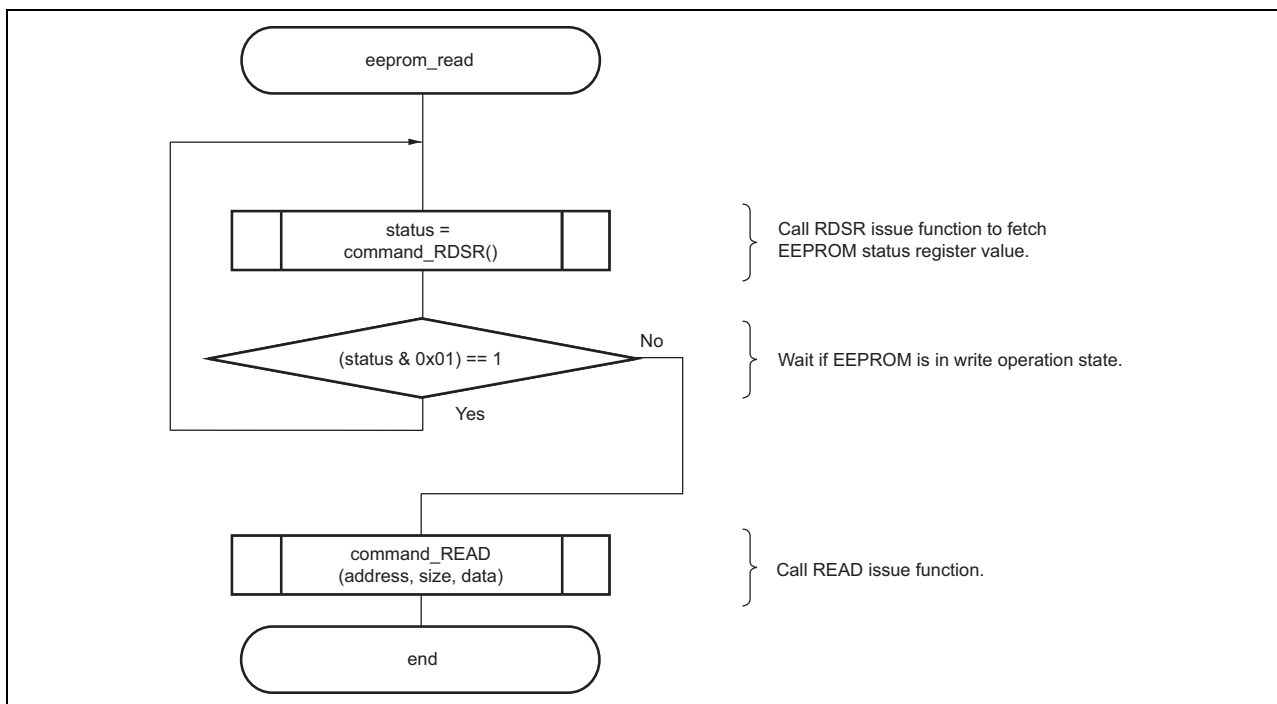


Figure 18 EEPROM Read Flowchart (eeprom_read)

5.5.7 command_WRSR Function

(1) Functional Overview

The command_WRSR function transmits the WRSR instruction code and EEPROM status register value to the EEPROM.

(2) Arguments

Argument	Type	Argument Name	Setting	Description
1st argument	unsigned int	address	—	Status value to be overwritten

(3) Returned values

None

(4) Description of internal I/O registers used

The internal I/O registers used by this function are shown below. Note that the setting values shown are those used in this application note and differ from the initial values.

- SS Control Register H (SSCRH) Number of bits: 8 Address: H'FFFCC0

Bit	Bit Name	Set Value	R/W	Description
1	CSS1	1	R/W	\overline{SCS} Pin Select
0	CSS0	1	R/W	Select that the \overline{SCS} pin functions as a port or \overline{SCS} input or output. However, when MSS = 0, the \overline{SCS} pin functions as an input pin regardless of the CSS1 and CSS0 settings. 11: Function as \overline{SCS} automatic output (outputs a high level before and after transfer and outputs a low level during transfer)

- SS Control Register L (SSCRL) Number of bits: 8 Address: H'FFFCC1

Bit	Bit Name	Set Value	R/W	Description
1	DATS1	0	R/W	Transmit/Receive Data Length Select Select serial data length.
0	DATS0	1	R/W	01: 16 bits

- SS Enable Register (SSER) Number of bits: 8 Address: H'FFFCC3

Bit	Bit Name	Set Value	R/W	Description
7	TE	1/0	R/W	Transmit Enable When this bit is set to 1, transmission is enabled.
6	RE	1/0	R/W	Receive Enable When this bit is set to 1, reception is enabled.
2	TIE	1/0	R/W	Transmit Interrupt Enable When this bit is set to 1, a TXI interrupt request is enabled.
1	RIE	1/0	R/W	Receive Interrupt Enable When this bit is set to 1, an RXI interrupt request and an OEI interrupt request are enabled.

(5) Flowchart

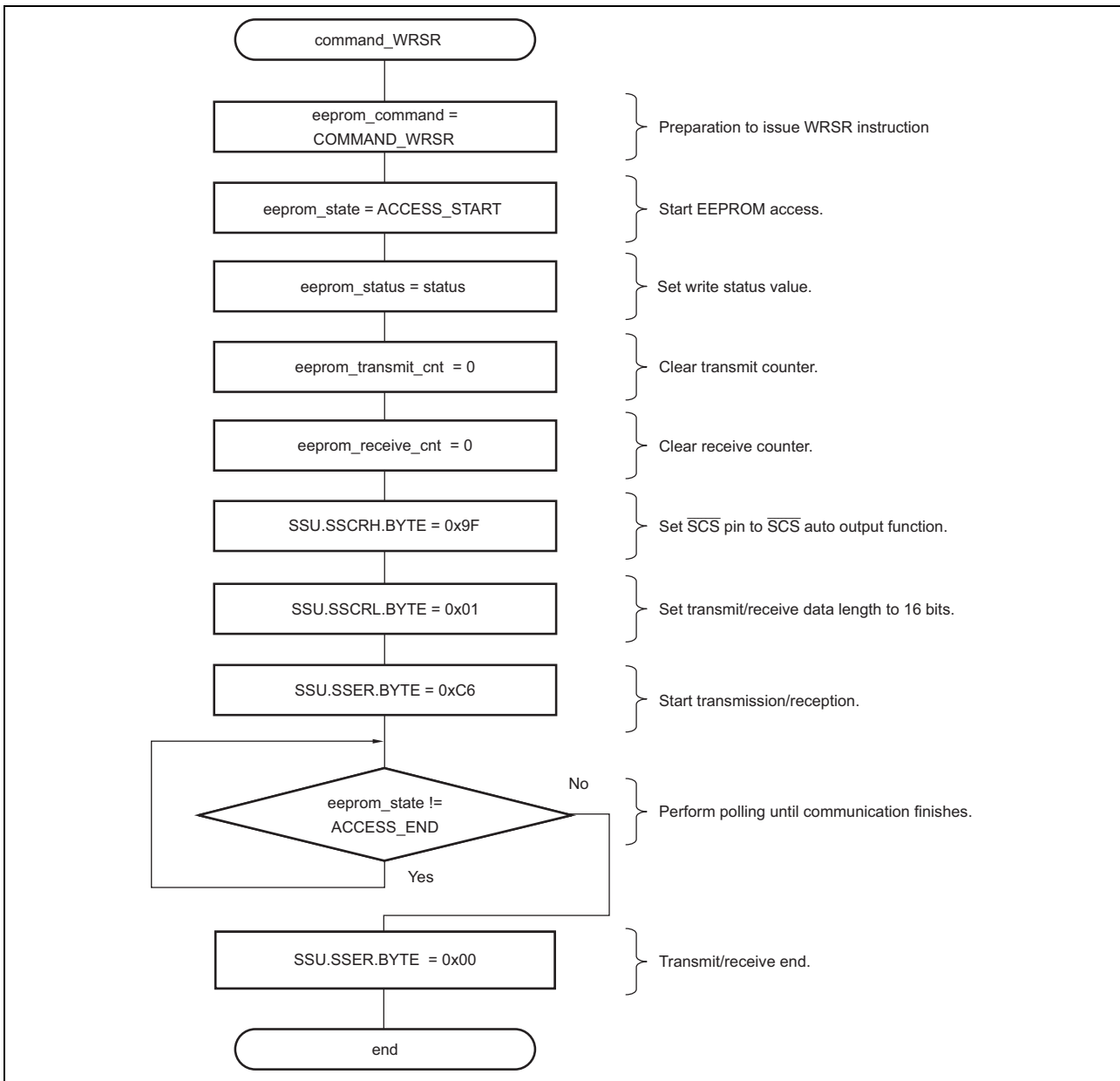


Figure 19 WRSR Issue Flowchart (command_WRSR)

5.5.8 command_RDSR Function

(1) Functional Overview

The command_RDSR function transmits the RDSR instruction code to the EEPROM. It also receives the EEPROM status register value from the EEPROM.

(2) Arguments

None

(3) Returned values

Type	Argument Name	Setting	Description
unsigned char	status	—	EEPROM status register data

(4) Description of internal I/O registers used

The internal I/O registers used by this function are shown below. Note that the setting values shown are those used in this application note and differ from the initial values.

- SS Control Register H (SSCRH) Number of bits: 8 Address: H'FFFCC0

Bit	Bit Name	Set Value	R/W	Description
1	CSS1	1	R/W	\overline{SCS} Pin Select
0	CSS0	1	R/W	Select that the \overline{SCS} pin functions as a port or \overline{SCS} input or output. However, when MSS = 0, the \overline{SCS} pin functions as an input pin regardless of the CSS1 and CSS0 settings. 11: Function as \overline{SCS} automatic output (outputs a high level before and after transfer and outputs a low level during transfer)

- SS Control Register L (SSCRL) Number of bits: 8 Address: H'FFFCC1

Bit	Bit Name	Set Value	R/W	Description
1	DATS1	0	R/W	Transmit/Receive Data Length Select
0	DATS0	1	R/W	Select serial data length. 01: 16 bits

- SS Enable Register (SSER) Number of bits: 8 Address: H'FFFCC3

Bit	Bit Name	Set Value	R/W	Description
7	TE	1/0	R/W	Transmit Enable When this bit is set to 1, transmission is enabled.
6	RE	1/0	R/W	Receive Enable When this bit is set to 1, reception is enabled.
2	TIE	1/0	R/W	Transmit Interrupt Enable When this bit is set to 1, a TXI interrupt request is enabled.
1	RIE	1/0	R/W	Receive Interrupt Enable When this bit is set to 1, an RXI interrupt request and an OEI interrupt request are enabled.

(5) Flowchart

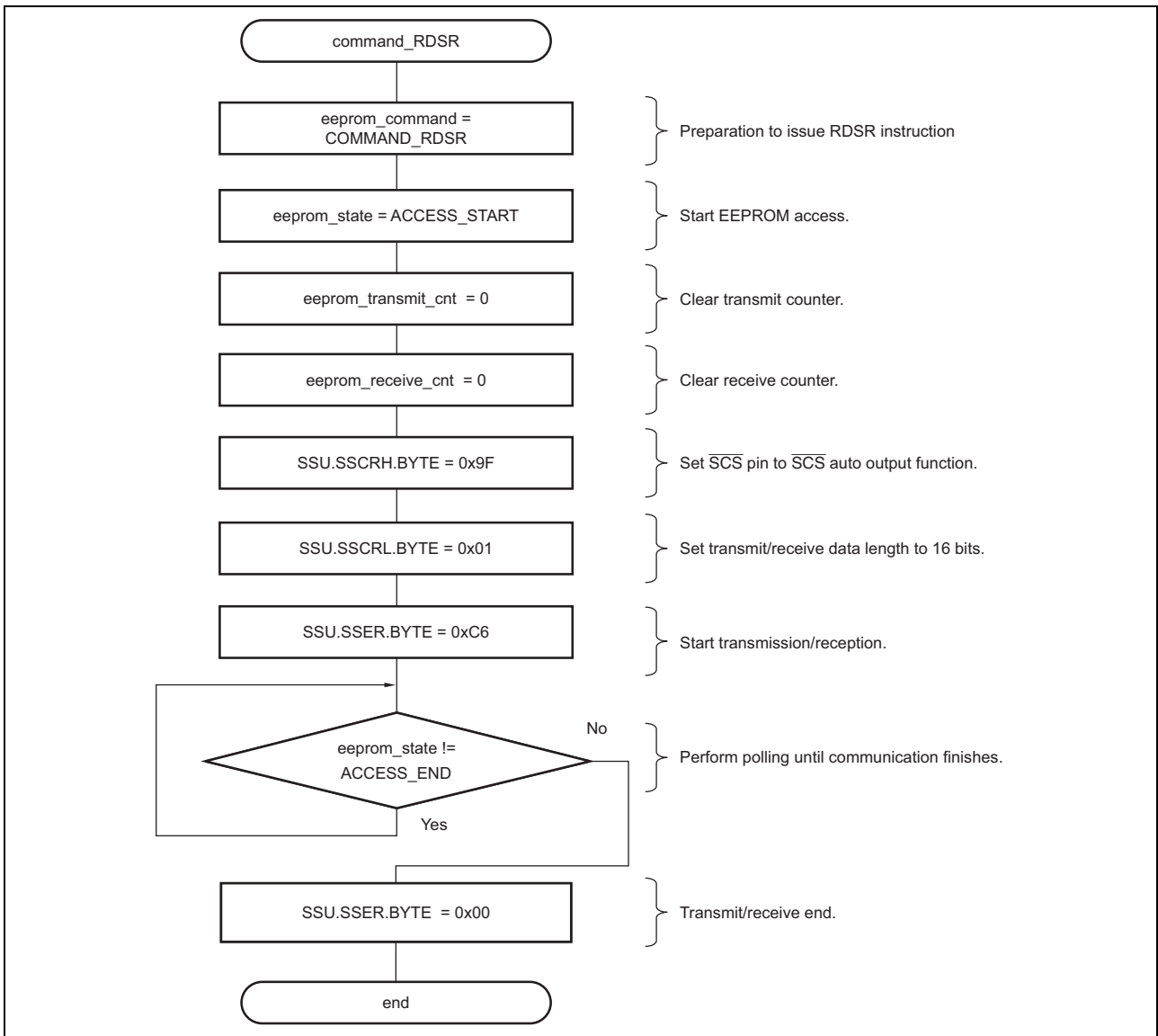


Figure 20 RDSR Issue Flowchart (command_RDSR)

5.5.9 command_WREN function

(1) Functional Overview

The command_WREN function transmits the WREN instruction code to the EEPROM.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

The internal I/O registers used by this function are shown below. Note that the setting values shown are those used in this application note and differ from the initial values.

- SS Control Register H (SSCRH) Number of bits: 8 Address: H'FFFCC0

Bit	Bit Name	Set Value	R/W	Description
1	CSS1	1	R/W	SCS Pin Select
0	CSS0	1	R/W	Select that the \overline{SCS} pin functions as a port or \overline{SCS} input or output. However, when MSS = 0, the \overline{SCS} pin functions as an input pin regardless of the CSS1 and CSS0 settings. 11: Function as \overline{SCS} automatic output (outputs a high level before and after transfer and outputs a low level during transfer)

- SS Control Register L (SSCRL) Number of bits: 8 Address: H'FFFCC1

Bit	Bit Name	Set Value	R/W	Description
1	DATS1	0	R/W	Transmit/Receive Data Length Select Select serial data length.
0	DATS0	0	R/W	00: 8 bits

- SS Enable Register (SSER) Number of bits: 8 Address: H'FFFCC3

Bit	Bit Name	Set Value	R/W	Description
7	TE	1/0	R/W	Transmit Enable When this bit is set to 1, transmission is enabled.
6	RE	1/0	R/W	Receive Enable When this bit is set to 1, reception is enabled.
2	TIE	1/0	R/W	Transmit Interrupt Enable When this bit is set to 1, a TXI interrupt request is enabled.
1	RIE	1/0	R/W	Receive Interrupt Enable When this bit is set to 1, an RXI interrupt request and an OEI interrupt request are enabled.

(5) Flowchart

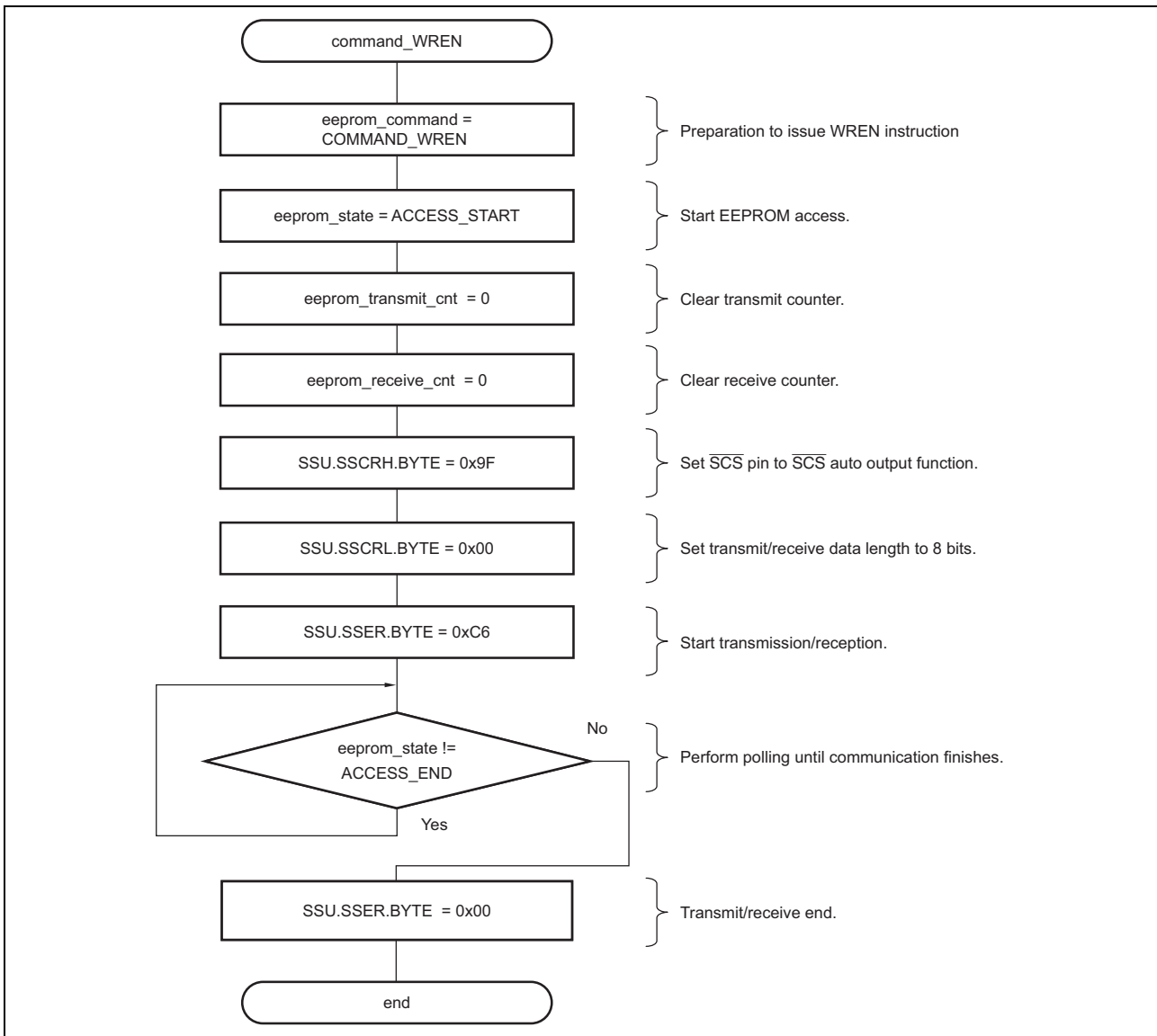


Figure 21 WREN Issue Flowchart (command_WREN)

5.5.10 command_WRITE Function

(1) Functional Overview

The command_WRITE function transmits the WRITE instruction code, address, and data to the EEPROM.

(2) Arguments

Argument	Type	Argument Name	Setting	Description
1st argument	unsigned int	address	—	Specifies the write destination address.
2nd argument	unsigned int	size	—	Specifies the write size.
3rd argument	unsigned char*	data	—	Specifies the write data storage destination pointer.

(3) Returned values

None

(4) Description of internal I/O registers used

The internal I/O registers used by this function are shown below. Note that the setting values shown are those used in this application note and differ from the initial values.

- SS Control Register H (SSCRH) Number of bits: 8 Address: H'FFFCC0

Bit	Bit Name	Set Value	R/W	Description
1	CSS1	0	R/W	SCS Pin Select
0	CSS0	0	R/W	Select that the \overline{SCS} pin functions as a port or \overline{SCS} input or output. However, when MSS = 0, the \overline{SCS} pin functions as an input pin regardless of the CSS1 and CSS0 settings. 00: I/O port

- SS Control Register L (SSCRL) Number of bits: 8 Address: H'FFFCC1

Bit	Bit Name	Set Value	R/W	Description
1	DATS1	0	R/W	Transmit/Receive Data Length Select Select serial data length.
0	DATS0	0	R/W	00: 8 bits

- Port 6 Data Register (P6DR) Number of bits: 8 Address: H'FFFBB

Bit	Bit Name	Set Value	R/W	Description
6	P6DR	1	R/W	This bit stores output data for a pin used as a general output port. When this register is read, the values for bits in P6DR corresponding to bits set to 1 in P6DDR are read, and for bits corresponding to bits cleared to 0 in P6DDR the pin states are read.

- SS Enable Register (SSER) Number of bits: 8 Address: H'FFFCC3

Bit	Bit Name	Set Value	R/W	Description
7	TE	1/0	R/W	Transmit Enable When this bit is set to 1, transmission is enabled.
6	RE	1/0	R/W	Receive Enable When this bit is set to 1, reception is enabled.
2	TIE	1/0	R/W	Transmit Interrupt Enable When this bit is set to 1, a TXI interrupt request is enabled.
1	RIE	1/0	R/W	Receive Interrupt Enable When this bit is set to 1, an RXI interrupt request and an OEI interrupt request are enabled.

(5) Flowchart

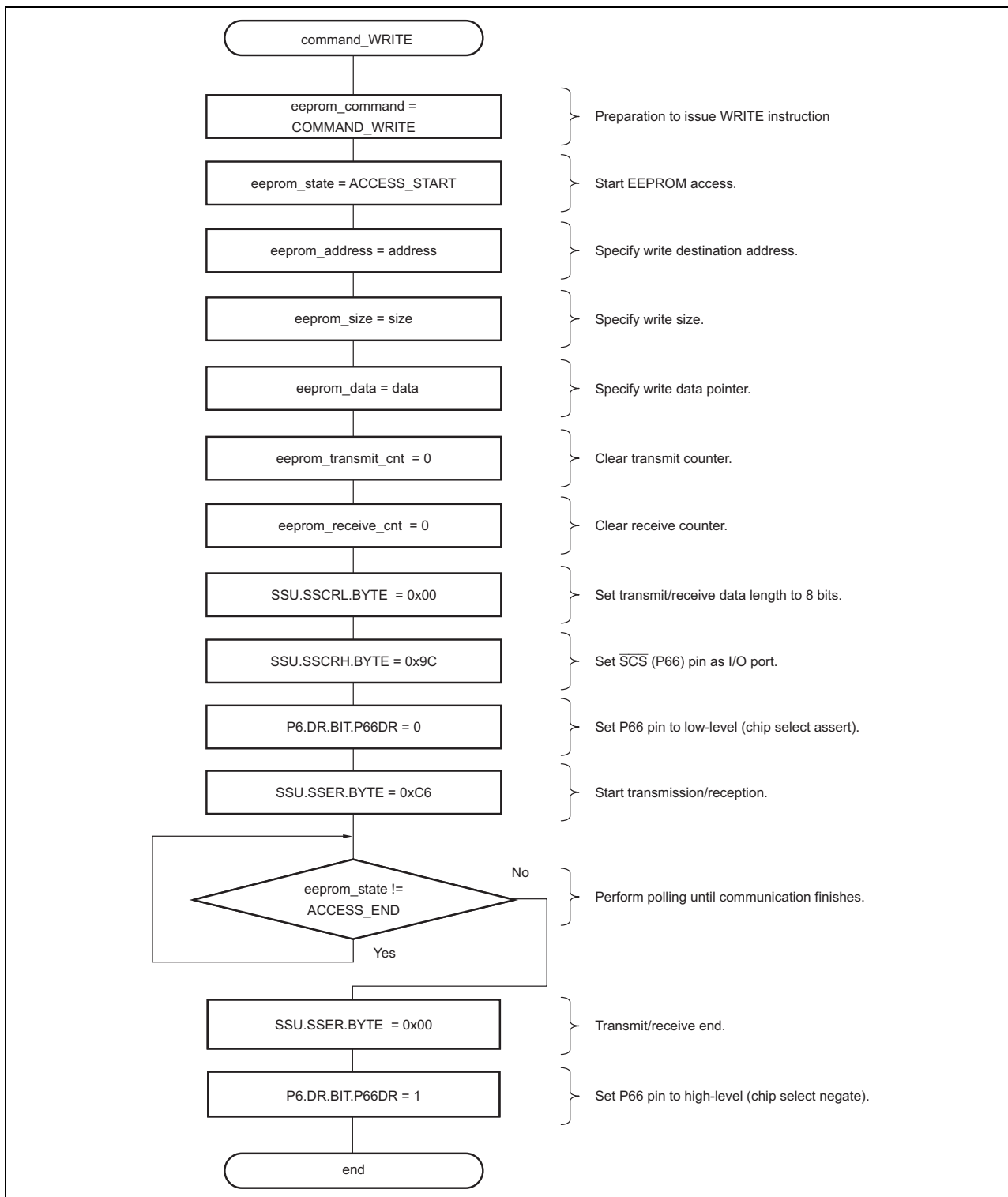


Figure 22 WRITE Issue Flowchart (command_WRITE)

5.5.11 command_READ Function

(1) Functional Overview

The command_READ function transmits the READ instruction code and address to the EEPROM. It also receives the data from the EEPROM.

(2) Arguments

Argument	Type	Argument Name	Setting	Description
1st argument	unsigned int	address	—	Specifies the read source address.
2nd argument	unsigned int	size	—	Specifies the read size.
3rd argument	unsigned char*	data	—	Specifies the read data storage destination pointer.

(3) Returned values

None

(4) Description of internal I/O registers used

The internal I/O registers used by this function are shown below. Note that the setting values shown are those used in this application note and differ from the initial values.

- SS Control Register H (SSCRH) Number of bits: 8 Address: H'FFFCC0

Bit	Bit Name	Set Value	R/W	Description
1	CSS1	0	R/W	\overline{SCS} Pin Select
0	CSS0	0	R/W	Select that the \overline{SCS} pin functions as a port or \overline{SCS} input or output. However, when MSS = 0, the \overline{SCS} pin functions as an input pin regardless of the CSS1 and CSS0 settings. 00: I/O port

- SS Control Register L (SSCRL) Number of bits: 8 Address: H'FFFCC1

Bit	Bit Name	Set Value	R/W	Description
1	DATS1	0	R/W	Transmit/Receive Data Length Select Select serial data length.
0	DATS0	0	R/W	00: 8 bits

- Port 6 Data Register (P6DR) Number of bits: 8 Address: H'FFFBB

Bit	Bit Name	Set Value	R/W	Description
6	P66DR	1	R/W	This bit stores output data for a pin used as a general output port. When this register is read, the values for bits in P6DR corresponding to bits set to 1 in P6DDR are read, and for bits corresponding to bits cleared to 0 in P6DDR the pin states are read.

- SS Enable Register (SSER) Number of bits: 8 Address: H'FFFCC3

Bit	Bit Name	Set Value	R/W	Description
7	TE	1/0	R/W	Transmit Enable When this bit is set to 1, transmission is enabled.
6	RE	1/0	R/W	Receive Enable When this bit is set to 1, reception is enabled.
2	TIE	1/0	R/W	Transmit Interrupt Enable When this bit is set to 1, a TXI interrupt request is enabled.
1	RIE	1/0	R/W	Receive Interrupt Enable When this bit is set to 1, an RXI interrupt request and an OEI interrupt request are enabled.

(5) Flowchart

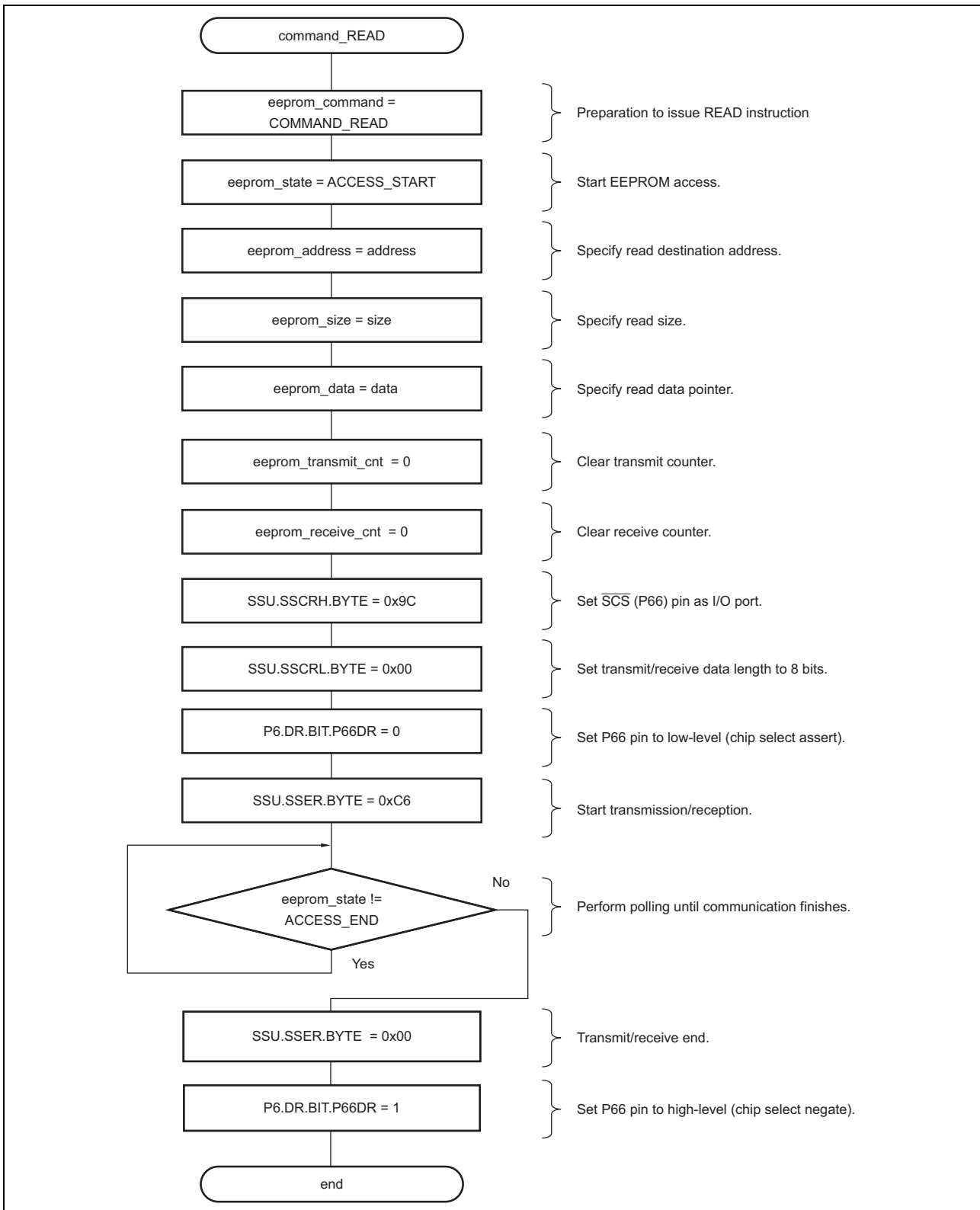


Figure 23 READ Issue Flowchart (command_READ)

5.5.12 INT_RXIS_SSU Function

(1) Functional Overview

The INT_RXIS_SSU function performs receive processing for the various instruction codes.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

The internal I/O registers used by this function are shown below. Note that the setting values shown are those used in this application note and differ from the initial values.

- SS Status Register (SSSR) Number of bits: 8 Address: H'FFFCC4

Bit	Bit Name	Set Value	R/W	Description
1	RDRF	0	R/W	<p>Receive Data Register Full</p> <p>Indicates whether or not SSRDR contains receive data.</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> • When receive data is transferred from SSTRSR to SSRDR after successful serial data reception <p>[Clearing conditions]</p> <ul style="list-style-type: none"> • When writing 0 after reading RDRF = 1 • When reading receive data from SSRDR

- SS Receive Data Registers 0 to 3 (SSRDR0 to SSRDR3) Number of bits: 8 Addresses: H'FFFCCA to H'FFFCCD
 Description: The SSRDR registers are 8-bit registers that store receive data. When 8-bit data length is selected by bits DATS1 and DATS0 in SSCRL, SSRDR0 is enabled. When 16-bit data length is selected, SSRDR0 and SSRDR1 are enabled. When 32-bit data length is selected, SSRDR0, SSRDR1, SSRDR2, and SSRDR3 are enabled.

Setting values: Status and read data

- SS Enable Register (SSER) Number of bits: 8 Addresses: H'FFFCC3

Bit	Bit Name	Set Value	R/W	Description
1	RIE	0	R/W	<p>Receive Interrupt Enable</p> <p>When this bit is set to 1, an RXI interrupt request and an OEI interrupt request are enabled.</p>

(5) Flowchart

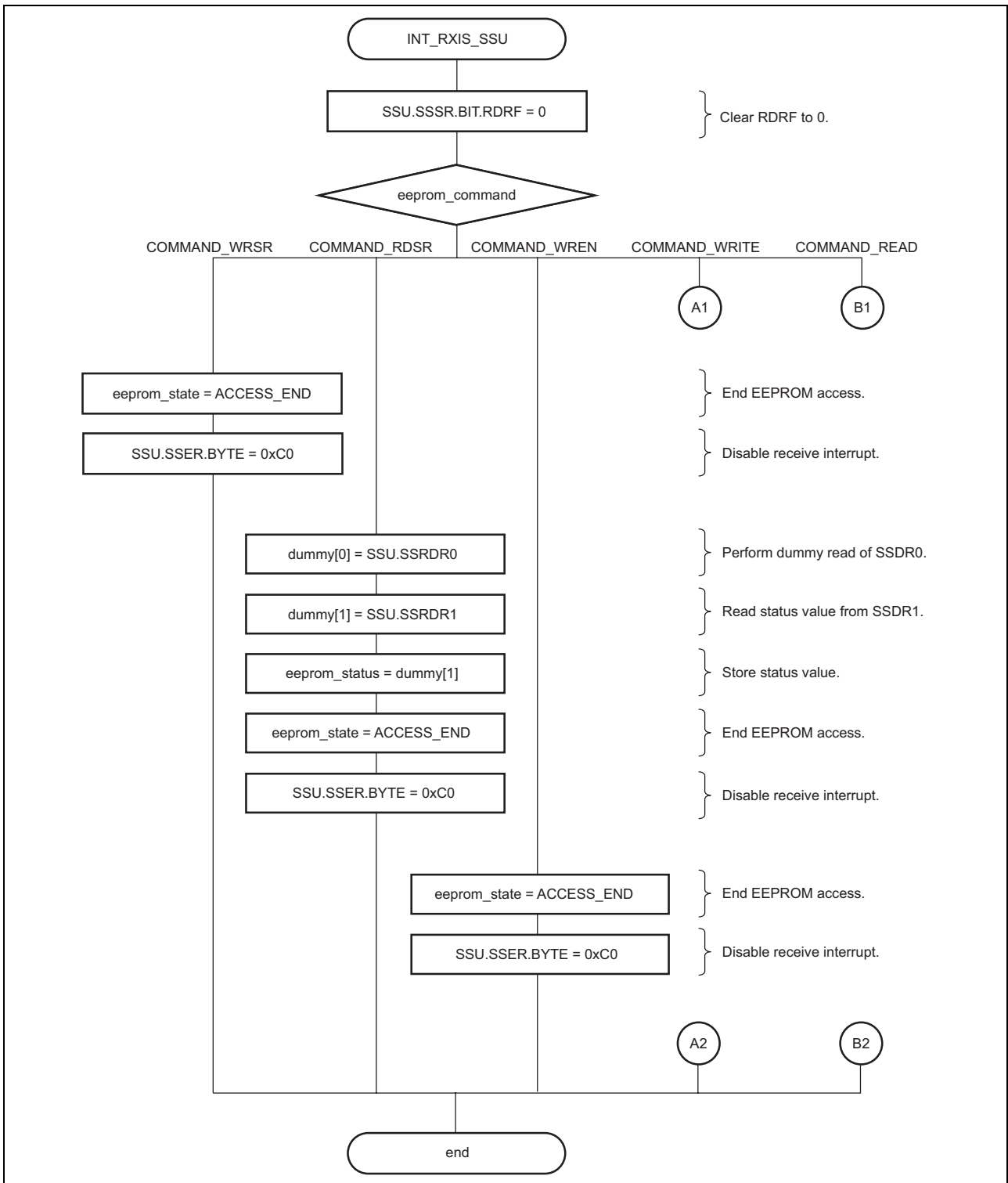


Figure 24 Receive Interrupt Flowchart 1. (INT_RXIS_SSU)

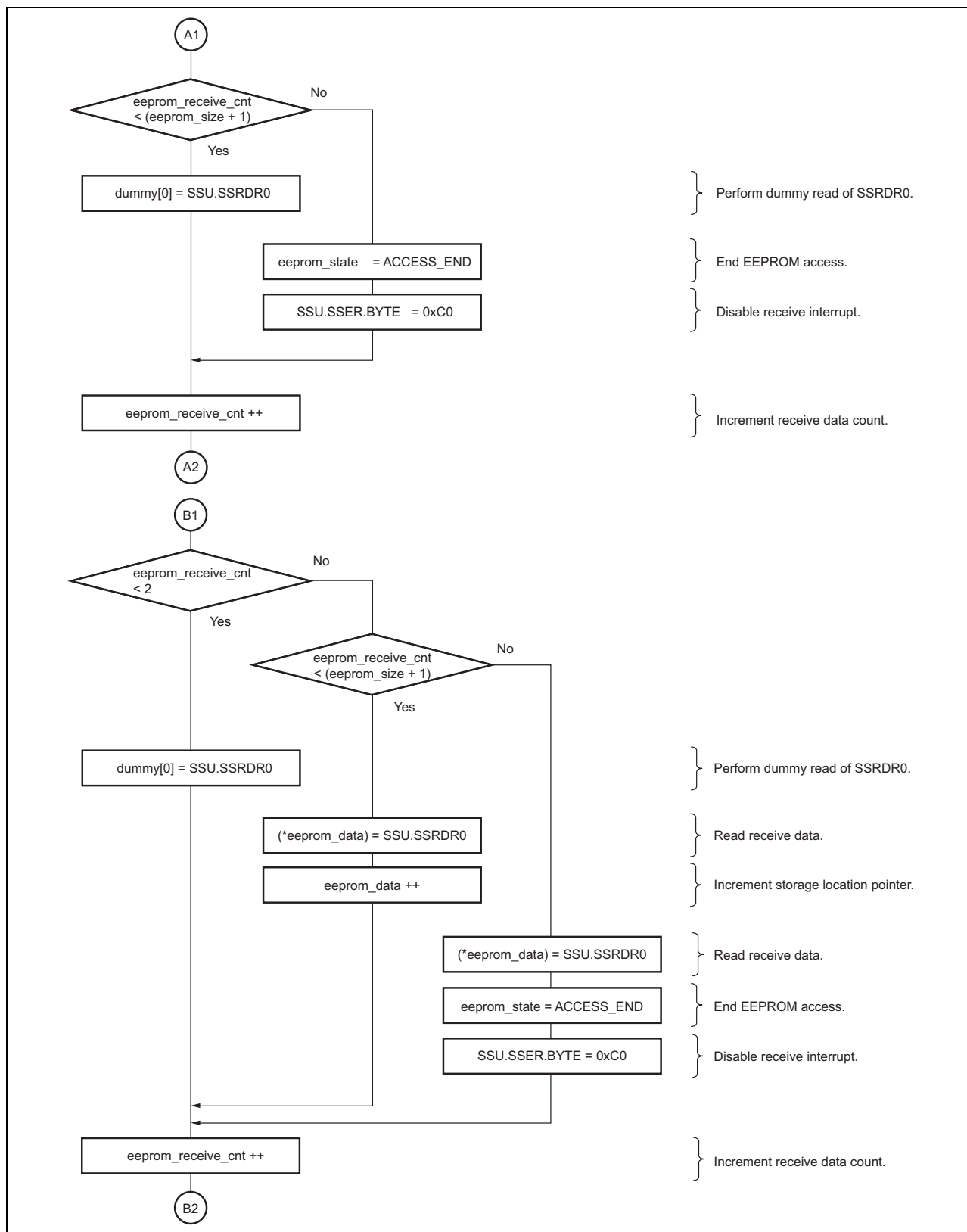


Figure 25 Receive Interrupt Flowchart 2. (INT_RXIS_SSU)

5.5.13 INT_TXIS_SSU Function

(1) Functional Overview

The INT_TXIS_SSU function performs transmit processing for the various instruction codes.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

The internal I/O registers used by this function are shown below. Note that the setting values shown are those used in this application note and differ from the initial values.

- SS Status Register (SSSR) Number of bits: 8 Address: H'FFFCC4

Bit	Bit Name	Set Value	R/W	Description
2	TDRE	0	R/W	Transmit Data Empty Indicates whether or not SSTDR contains transmit data. [Setting conditions] <ul style="list-style-type: none"> • When the TE bit in SSER is 0 • When data is transferred from SSTDR to SSTRSR and SSTDR is ready to be written to. [Clearing conditions] <ul style="list-style-type: none"> • When writing 0 after reading TDRE = 1 • When writing data to SSTDR with TE = 1

- SS Transmit Data Registers 0 to 3 (SSTDR0 to SSTDR3) Number of bits: 8 Addresses: H'FFFCC6 to H'FFFCC9
 Description: The SSTDR registers are 8-bit registers that store transmit data. When 8-bit data length is selected by bits DATS1 and DATS0 in SSCRL, SSTDR0 is enabled. When 16-bit data length is selected, SSTDR0 and SSTDR1 are enabled. When 32-bit data length is selected, SSTDR0, SSTDR1, SSTDR2, and SSTDR3 are enabled.

Setting values: Instruction code, address, status, and write data

- SS Enable Register (SSER) Number of bits: 8 Addresses: H'FFFCC3

Bit	Bit Name	Set Value	R/W	Description
2	TIE	1/0	R/W	Transmit Interrupt Enable When this bit is set to 1, a TXI interrupt request is enabled.

(5) Flowchart

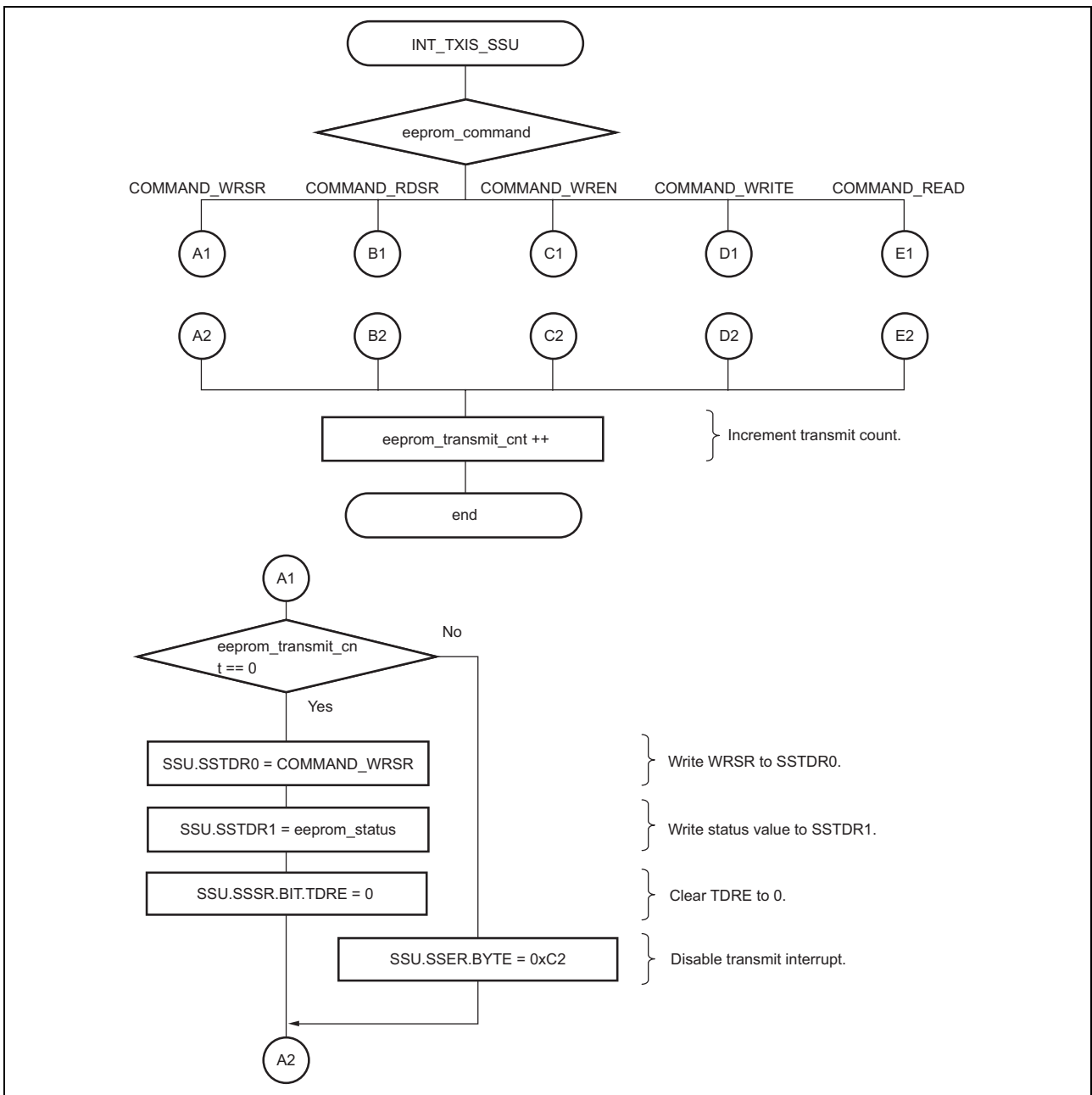


Figure 26 Transmit Interrupt Flowchart 1. (INT_TXIS_SSU)

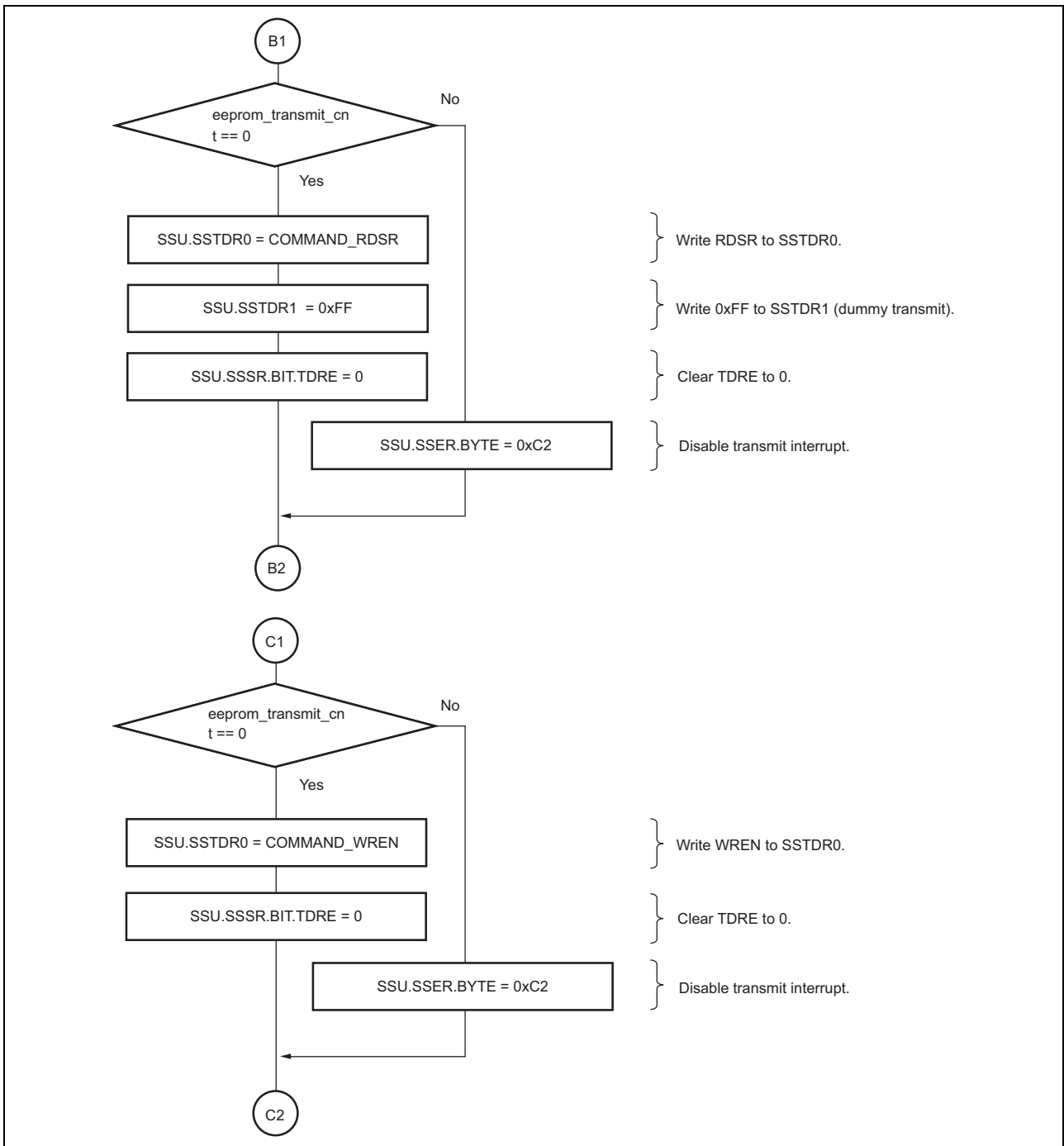


Figure 27 Transmit Interrupt Flowchart 2. (INT_TXIS_SSU)

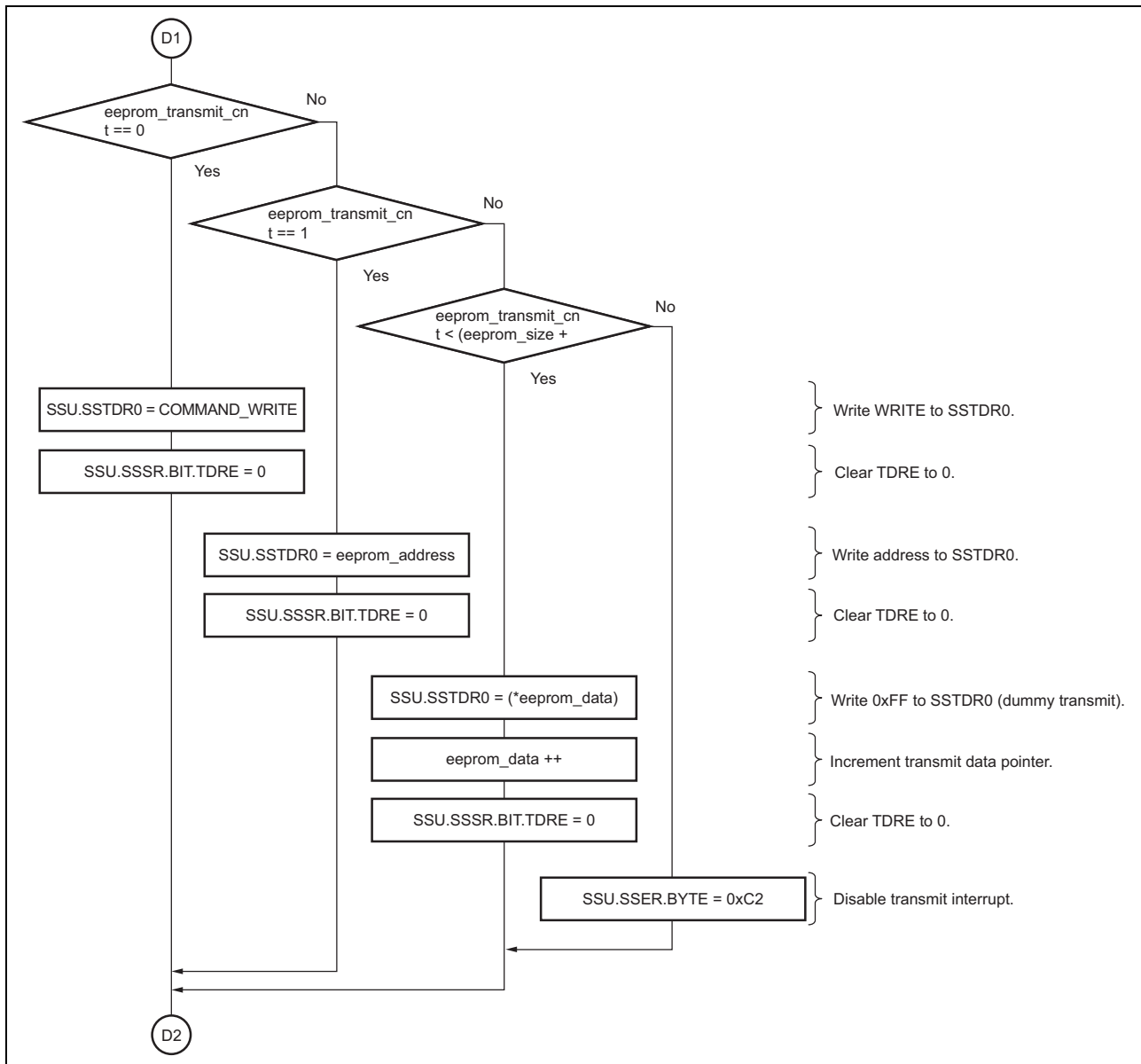


Figure 28 Transmit Interrupt Flowchart 3. (INT_TXIS_SSU)

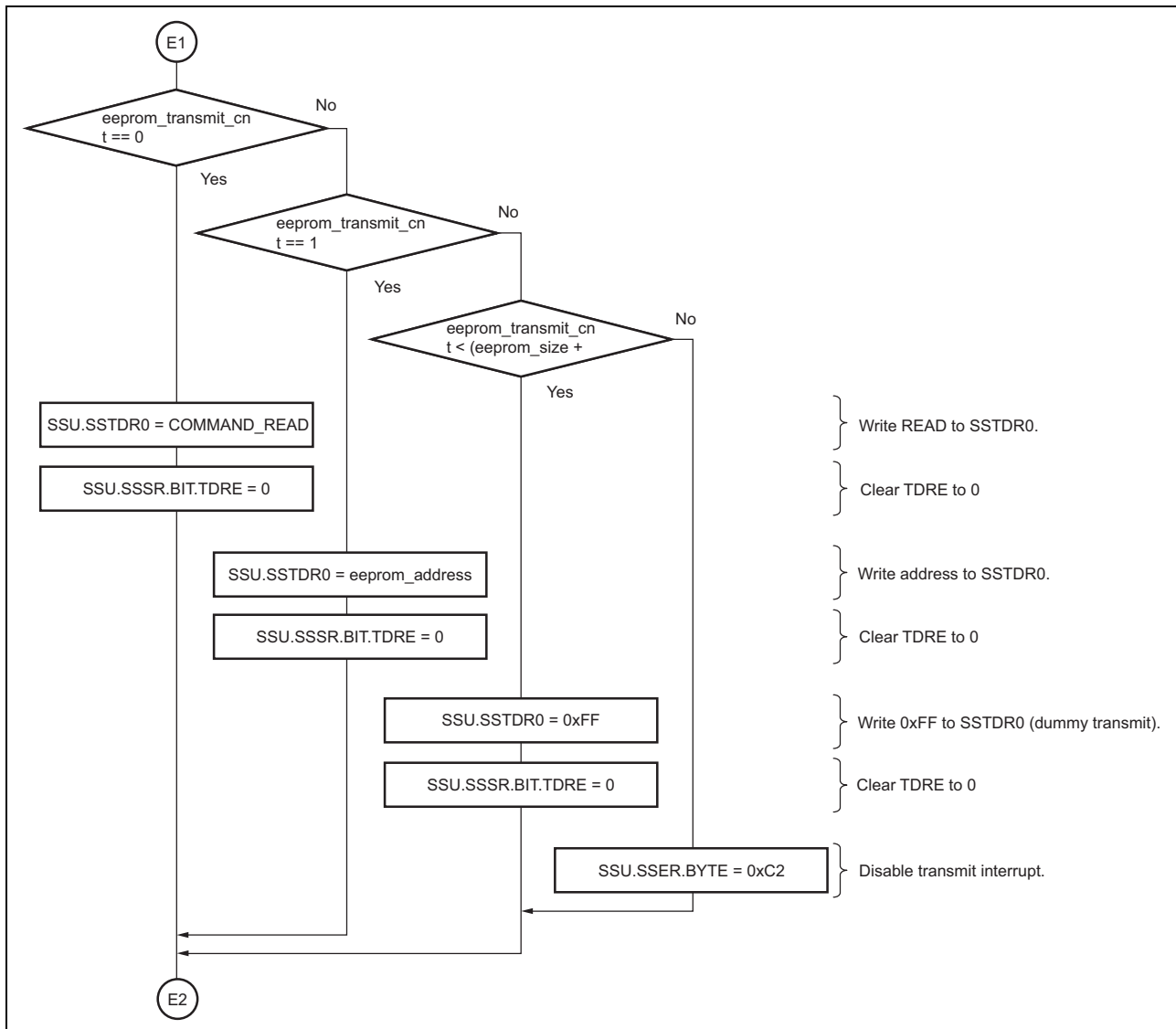


Figure 29 Transmit Interrupt Flowchart 4. (INT_TXIS_SSU)

6. Reference Documents

- Hardware Manual
H8S/2472, H8S/2463, H8S/2462 Group Hardware Manual
(The latest version can be downloaded from the Renesas Technology Web site.)
- Development Environment Manual
H8S/300, H8/300 Series C/C++ Compiler Package User's Manual
(The latest version can be downloaded from the Renesas Technology Web site.)
- Data Sheet
HN58X2502/HN58X2504I
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