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H8S/2200 Series

Bus Controller

Introduction

This application note provides subroutines that makes settings relating to bus controller modes, along with some examples of their usage.

Target Device

H8S/2215

Contents

1. Overview

This Application Note provides subroutines that are used to set the H8S/2215 bus controller modes, and shows usage samples.

2. Configuration

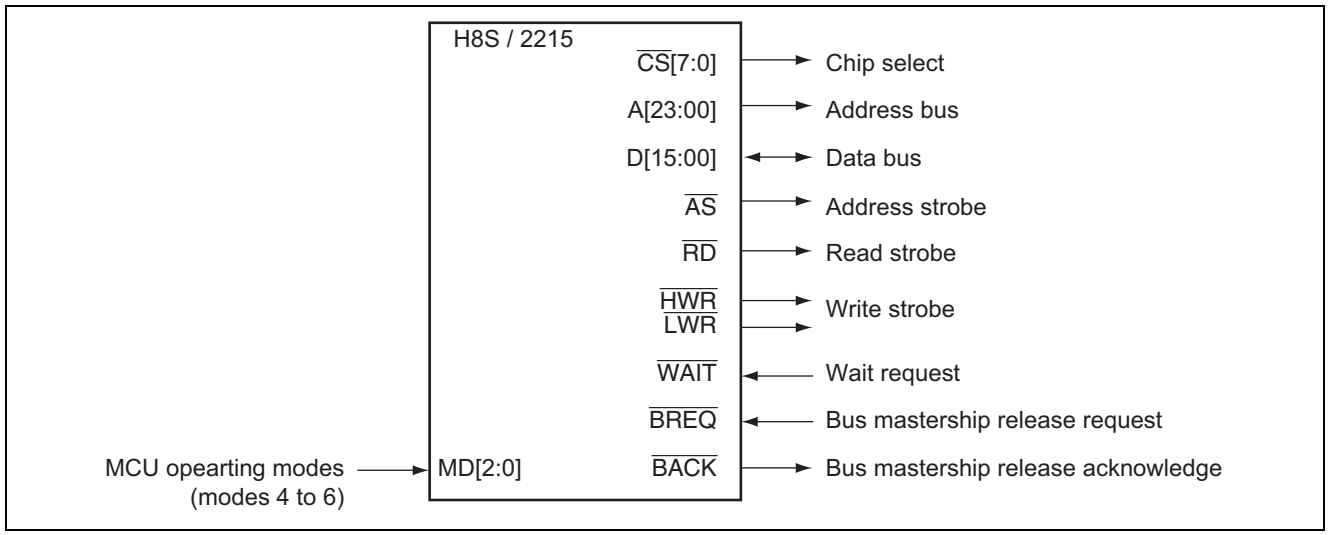


Figure 1 Bus Controller

Table 1 Pin Configuration

Signal Name	I/O	Description
$\overline{CS}$[7:0]	O	Chip select signal Indicates the selected area out of areas 0 to 7, each of which is a 2-Mbyte area making up a 16-Mbyte address space.
A[23:0]	O	Address bus
D[15:0]	I/O	Data bus
$\overline{AS}$	O	Address strobe signal Indicates that the address output on address bus is valid when this signal is low.
$\overline{RD}$	O	Read strobe signal Indicates that external address space is being read when this signal is low.
$\overline{HWR}$	O	Write strobe signal (D[15:08]) Indicates that external address space (D[15:08]) is being written to when this signal is low.
$\overline{LWR}$	O	Write strobe signal (D[07:00]) Indicates that external address space (D[07:00]) is being written to when this signal is low.
$\overline{WAIT}$	I	Wait request signal Wait state can be inserted by inputting a low-level signal to this pin.
$\overline{BREQ}$	I	Bus request signal Causes the microcomputer to release bus mastership (sets A[23:0], D[15:0], $\overline{CS}$[7:0], $\overline{AS}$, $\overline{RD}$, $\overline{HWR}$, and $\overline{LWR}$ to high impedance) by inputting a low-level signal to this pin.
$\overline{BACK}$	O	Bus request acknowledge signal Indicates the external bus released state while this signal is low.

3. Sample Programs

3.1 Functions

The sample programs provide subroutines for setting registers necessary for bus control processing.

1. Sets bus controller modes set for each area.
2. Specifies idle cycle insertion conditions.
3. Sets burst ROM mode for area 0.
4. Enables/disables external bus release.
5. Enables/disables wait input on $\overline{\text{WAIT}}$ pin.
6. Specifies address bus output enabled range.

3.2 Program Incorporation

1. Incorporate sample program 5-A: #define definitions.
2. Incorporate sample program 5-B: prototype declarations.
3. Sample program 5-C
   A. Add the process of enabling/disabling the bus controller to initial setting processing.
   B. Add bus controller-related common subroutines.

3.3 Modifications to Sample Programs

Without modifications to the sample program, the system may not run. Modifications must be made according to your program and system environment.

1. The sample programs can be used without further changes if you use the I/O register structure definition file, which is available free of charge from the following Renesas web site:
   http://www.renesas.com/eng/products/mpumcu/tool/crosstool/iodef/index.html
   When you create structure definitions by yourself, modify the I/O register structures used in the sample program as appropriate.
2. The chip select signal for the bus controller is set by the I/O port DDR register. The chip select signal is enabled when the corresponding DDR register is set to '1'. The initial settings should be modified according to your system. As for the locations of modifications, refer to program note in the sample program.

3.4 Using the Sample Programs

Subroutines for setting registers required for bus control processing provided in the sample programs are described below.

1. List of subroutines

Subroutine Name	Function
com_bus_are_control	Sets bus controller modes for each area
com_bus_idle_cycle_mode	Specifies idle cycle insertion conditions
com_bus_burst_rom_mode	Sets burst ROM mode for area 0
com_bus_release_control	Enables/disables external bus release
com_bus_hw_wait_control	Enables/disables wait input on WAIT pin
com_bus_address_control	Specifies address bus output enabled range

2. Sets bus controller modes for each area.

- Subroutine name: void com_bus_area_control (int area_no, int bus_width, int state_num, int wait_num)

Argument	Description
area_no	Specifies an area. BUS_AREA_0 to BUS_AREA_7 (0 to 7): Area 0 to 7
bus_width	Selects data bus width. BUS_16BIT (0): Data bus width: 16 bits BUS_8BIT (1): Data bus width: 8 bits
bus_state	Specifies the number of access states (the number of states for access to data bus). BUS_STATE_2 (0): Bus cycle: 2 states BUS_STATE_3 (1): Bus cycle: 3 states
wait_num	Specifies the number of wait states to be inserted in the program. This is only effective when bus cycle is 3 states. BUS_WAIT_0 (0): No program wait state is inserted BUS_WAIT_1 (1): 1 program wait state is inserted BUS_WAIT_2 (2): 2 program wait states are inserted BUS_WAIT_3 (3): 3 program wait states are inserted

Note: The initial value of the microcomputer prior to executing this subroutine differs depending on the H8 microcomputer's operating mode.

	Mode 4	Modes 5 to 7
Data bus width	16 bits (BUS_16BIT)	8 bits (BUS_8BIT)
Number of access states	3 states (BUS_STATE_3)	←
Number of wait states	3 states (BUS_WAIT_3)	←

3. Specifies idle cycle insertion conditions.

- Subroutine name: void com_bus_idle_cycle_mode (int idle_cycle_mode)

Argument	Setting
idle_cycle_mode	Specifies idle cycle insertion. BUS_IDLE_0 (0): No idle cycle is inserted BUS_IDLE_1 (1): An idle cycle is inserted when successive external read and write cycles are performed BUS_IDLE_2 (2): An idle cycle is inserted when successive external read cycles are performed in different areas BUS_IDLE_3 (3): An idle cycle is inserted when successive external read and write cycles are performed and when successive external read cycles are performed in different areas

Note: The initial value of the microcomputer prior to executing this subroutine is BUS_IDLE_3.

4. Sets burst ROM mode for area 0.

- Subroutine name: void com_bus_burst_rom_mode (int burst_rom_mode)

Argument	Description
ADC_NO_EXE (0)	Sets burst ROM mode. BUS_AREA0_BASIC (0): Area 0 is used through the basic bus interface (area 0 is not set to burst ROM mode). BUS_AREA0_BURST_1_4 (4): Area 0 is set to burst ROM mode. Burst cycle: 1 state, Burst access: max. 4 words BUS_AREA0_BURST_1_8 (5): Area 0 is set to burst ROM mode. Burst cycle: 1 state, Burst access: max. 8 words BUS_AREA0_BURST_2_4 (6): Area 0 is set to burst ROM mode. Burst cycle: 2 states, Burst access: max. 4 words BUS_AREA0_BURST_2_8 (7): Area 0 is set to burst ROM mode. Burst cycle: 2 states, Burst access: max. 8 words

Note: he initial value of the microcomputer prior to executing this subroutine is BUS_AREA0_BASIC.

5. Enables/disables wait input on WAIT pin.

- Subroutine name: void com_bus_hw_wait_control (int hw_wait_control)

Argument	Setting
hw_wait_control	Enables/disables wait input by WAIT pin. BUS_WAIT_DISABLE (0): Wait input by WAIT pin is disabled BUS_WAIT_ENABLE (1): Wait input by WAIT pin is enabled

Note: The initial value of the microcomputer prior to executing this subroutine is BUS_WAIT_DISABLE.

6. Enables/disables external bus release.

- Subroutine name: void com_bus_release_control (int bus_release_control)

Argument	Setting
bus_release_control	Enables/disables external bus release. BUS_RELEASE_DISABLE (0): External bus release is disabled BUS_RELEASE_ENABLE (1): External bus release is enabled

Note: The initial value of the microcomputer prior to executing this subroutine is BUS_RELEASE_DISABLE.

7. Specifies address bus output enabled range.

- Subroutine name: void com_bus_address_control (int address_control)

Argument	Setting
address_control	Specifies address bus output enabled range. BUS_A7_0_ENABLE (0): A7 to A0 output is enabled BUS_A8_0_ENABLE (1): A8 to A0 output is enabled BUS_A9_0_ENABLE (2): A9 to A0 output is enabled BUS_A10_0_ENABLE (3): A10 to A0 output is enabled BUS_A11_0_ENABLE (4): A11 to A0 output is enabled BUS_A12_0_ENABLE (5): A12 to A0 output is enabled BUS_A13_0_ENABLE (6): A13 to A0 output is enabled BUS_A14_0_ENABLE (7): A14 to A0 output is enabled BUS_A15_0_ENABLE (8): A15 to A0 output is enabled BUS_A16_0_ENABLE (9): A16 to A0 output is enabled BUS_A17_0_ENABLE (10): A17 to A0 output is enabled BUS_A18_0_ENABLE (11): A18 to A0 output is enabled BUS_A19_0_ENABLE (12): A19 to A0 output is enabled BUS_A20_0_ENABLE (13): A20 to A0 output is enabled BUS_A21_0_ENABLE (14): A21 to A0 output is enabled BUS_A22_0_ENABLE (15): A22 to A0 output is enabled BUS_A23_0_ENABLE (16): A23 to A0 output is enabled

Note: The initial value of the microcomputer prior to executing this subroutine is BUS_A20_0_ENABLE when the H8 microcomputer operating mode is 4 or 5; or BUS_A7_0_ENABLE when the H8 microcomputer operating mode is 6 or 7.

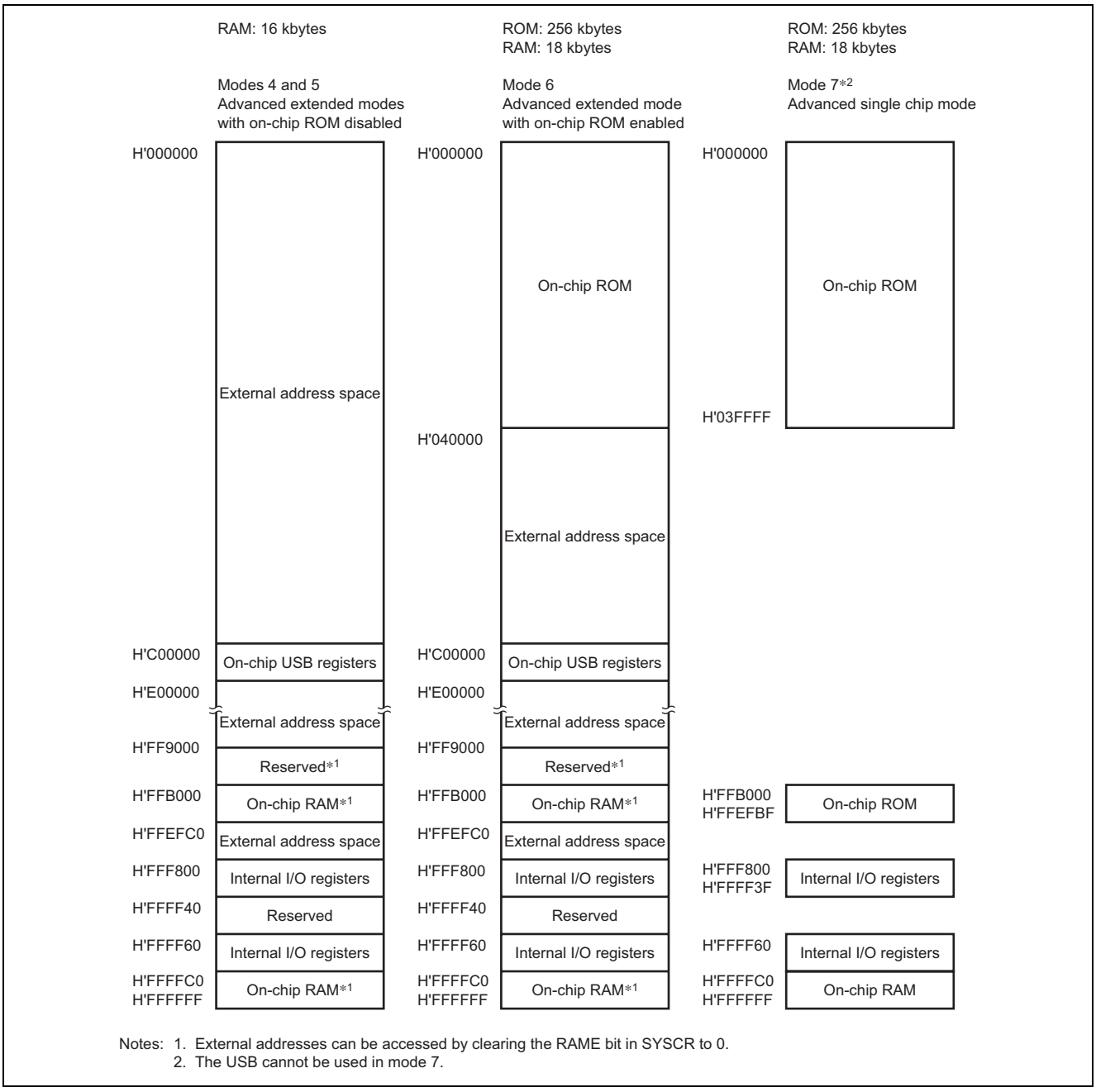
3.5 Description of Operation

3.5.1 CPU Operating Modes

The H8S/2215 can operate in four modes (modes 4 to 7) by setting the mode pins (MD2 to MD0) of the microcomputer. Of these, the bus controller settings are valid in modes 4 to 6. Table 2 shows specifications of each mode, and figure 2 shows the address map.

Table2 Specifications of CPU Operating Modes

	Mode 4 (Extended mode 1 with on-chip ROM disabled)	Mode 5 (Extended mode 2 with on-chip ROM disabled)	Mode 6 (Extended mode 1 with on-chip ROM enabled)	Mode 7 (single chip mode)
Address space	16 MB	←	←	←
On-chip ROM	Disabled	Disabled	Enabled	Enabled
External bus	Enabled	Enabled	Enabled	Disabled
Initial external bus width	16 bits	8 bits	8 bits	—
USB	Enabled (area 6)	←	←	Disabled



Notes: 1. External addresses can be accessed by clearing the RAME bit in SYSCR to 0.
2. The USB cannot be used in mode 7.

Figure 2 HD64F2215/HD64F2215U Address Map

3.5.2 Bus Area

The bus controller divides 16-Mbyte external address space into eight areas in 2-Mbyte units and provides bus control over the external address space for each area. The bus width, the number of access states, the number of program wait states, and enabling/disabling of the chip select (CS) signal can be specified for each area. Those except for enabling/disabling of the chip select (CS) signal can be set easily with the subroutines com_bus_area_control and com_bus_address_control provided in this Application Note.

1. Address Space of Each Area

Area	Address Space	Remarks
0	0x000000 to 0x1FFFFF	In mode 6, 0x000000 to 0x03FFFF is the area for On-chip ROM.
1	0x200000 to 0x3FFFFF	
2	0x400000 to 0x5FFFFF	
3	0x600000 to 0x7FFFFF	
4	0x800000 to 0x9FFFFF	
5	0xA00000 to 0xBFFFFF	
6	0xC00000 to 0xDFFFFF	On-chip USB registers
7	0xE00000 to 0xFFFFFF	0xFFB000 to 0xFFEFBF: On-chip RAM 0xFFF800 to 0xFFFF3F: Internal I/O registers 0xFFFF60 to 0xFFFFBF: Internal I/O registers 0xFFFFC0 to 0xFFEFFF: On-chip RAM

2. Bus Width
   A bus width of 8 or 16 bits can be selected depending on a device to be connected. When area 0 is set to burst ROM mode, the bus width is fixed to 16 bits. The bus width is set with the subroutine com_bus_area_control.

3. Number of Access States and Number of Program Wait States
   Two or three access states can be specified according to the operating speed of a device to be connected. When three access states are selected, the bus access period can be extended by specifying the number of program wait states. The number of access states and the number of program wait states are set with the subroutine com_bus_area_control.

Number of Access States	Number of Program Wait States	Bus Cycle
2	—	2
3	0	3
	1	4
	2	5
	3	6

4. Address Width
   The address width to be used can be specified. Address pins that are not used can function as the I/O ports. The address width is set with the subroutine com_bus_address_control.

5. Chip Select Signals

The chip select (CS) signal is enabled/disabled by setting the corresponding data direction (DDR) register for the I/O port. The CS signal is enabled by setting the corresponding DDR register to '1'. When the corresponding external address space is accessed with CS enabled, a low level CS signal is output during the bus cycle.

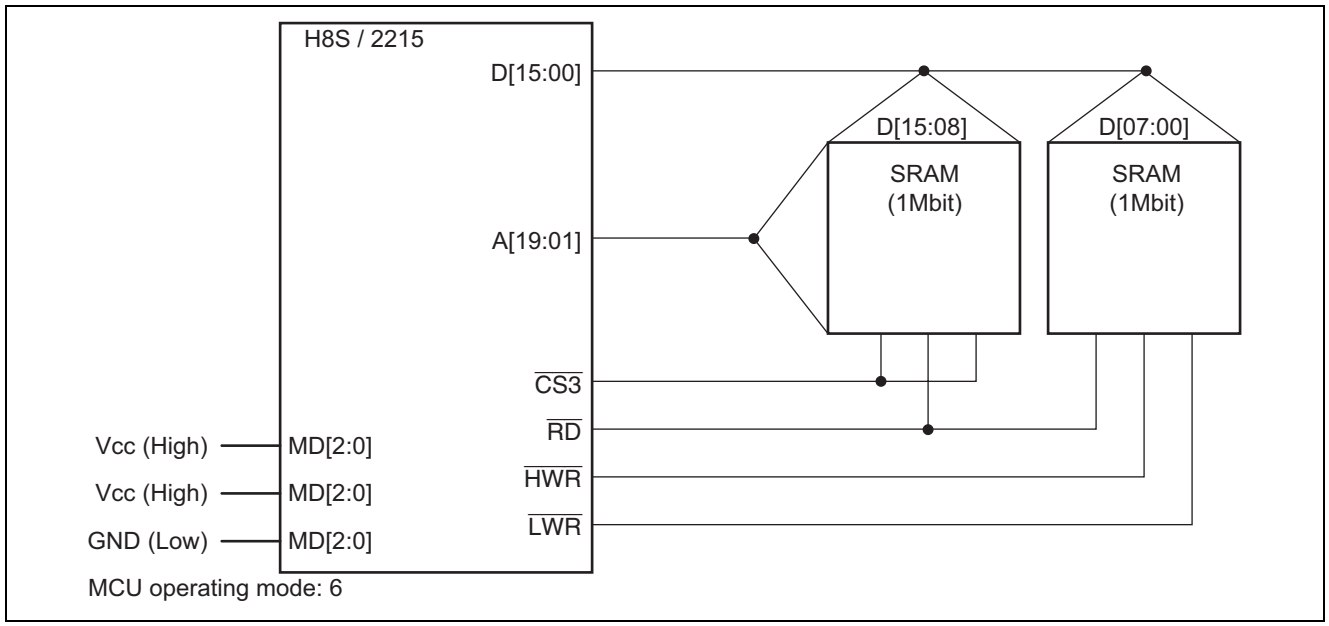
Being a write-only register, the DDR register cannot be read from and rewritten to after manipulating only the necessary bits. For this reason, this Application Note does not provide any subroutine for CS setting. The DDR resisters, including the bits not assigned a CS signal (PG0 and P74), should be set during the initial setting process of the microcomputer.

The DDR registers (PG0 and P74) that do not correspond to the CS signal should also be set in the initial setting process of the microcomputer.

I/O Port (Address)	Bit	Corresponding CS	Setting Value
PG (FE3F)	4	CS0	1: CS is enabled (output mode)
	3	CS1	0: CS is disabled (input mode)
	2	CS2	
	1	CS3	
	0	—	
P7 (FE36)	4	—	1: CS is enabled (output mode)
	3	CS7	0: CS is disabled (input mode)
	2	CS6	
	1	CS5	
	0	CS4	

6. Usage Examples

The following example shows the setting when two 128-kbit × 8-bit SRAMs are connected to area 3.



The followings should be set in the initial setting routine of the microcomputer.

— Chip select 3 (CS3) setting:
PG.DDR = 0x08;

— Bus controller mode setting for each area:
com_bus_area_control (BUS_AREA3, BUS_16BIT, BUS_STATE_3, BUS_WAIT_3)

Through the above settings, SRAM can be accessed in 2-byte units at addresses 0x600000 to 0x67FFFF.

3.5.3 Idle Cycle

An idle cycle can be inserted between bus cycles in the following two cases.

- When read accesses to different areas occur consecutively
- When a write cycle occurs immediately after a read cycle

By inserting an idle cycle it is possible to avoid data collisions between devices with different speeds that are connected to different areas. For details, see section 6.8, Idle Cycle, of the H8S/2215 Series Hardware Manual.

In the initial setting, the idle cycle insertion is enabled. Unless there is any specific strict performance request, the initial setting need not be changed.

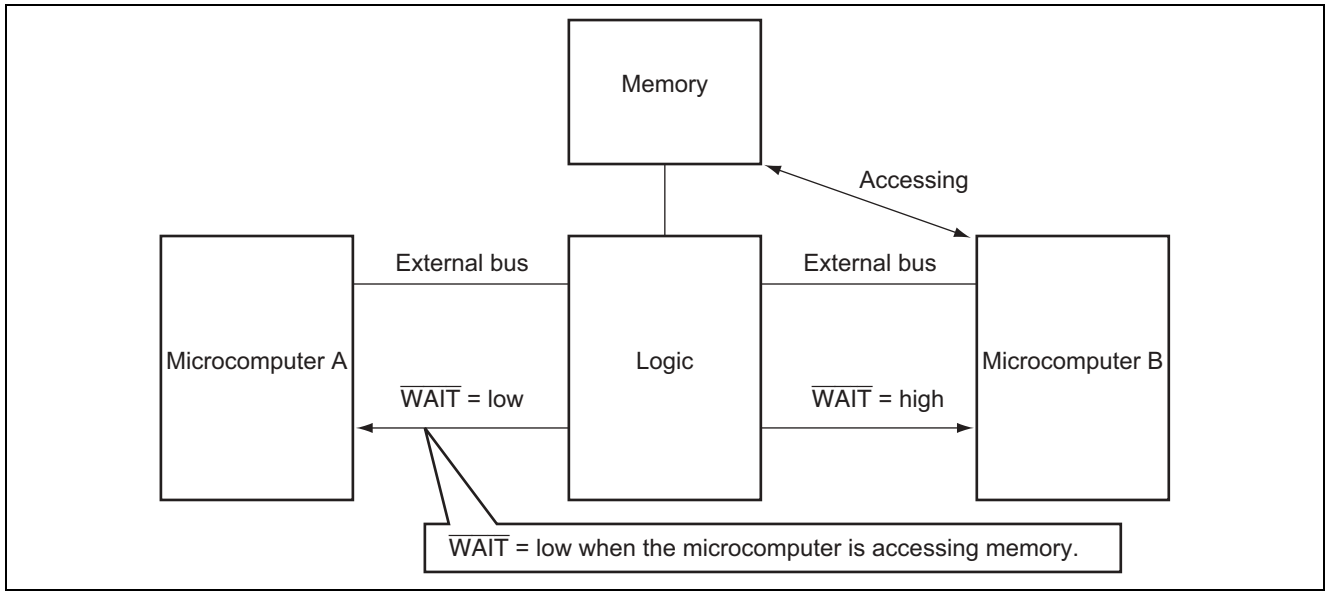
The idle cycle insertion can be easily set with the subroutine com_bus_ilde_cycle_mode provided in this Application Note.

3.5.4 Burst ROM Mode

ROM that supports burst mode (consecutive read) can be connected to the external address space of area 0. For details, see section 6.7, Burst ROM Interface, of the H8S/2215 Series Hardware Manual. The burst ROM mode can be easily set with the subroutine com_bus_burst_rom_mode provided in this Application Note.

3.5.5 $\overline{\text{WAIT}}$ Pin Function

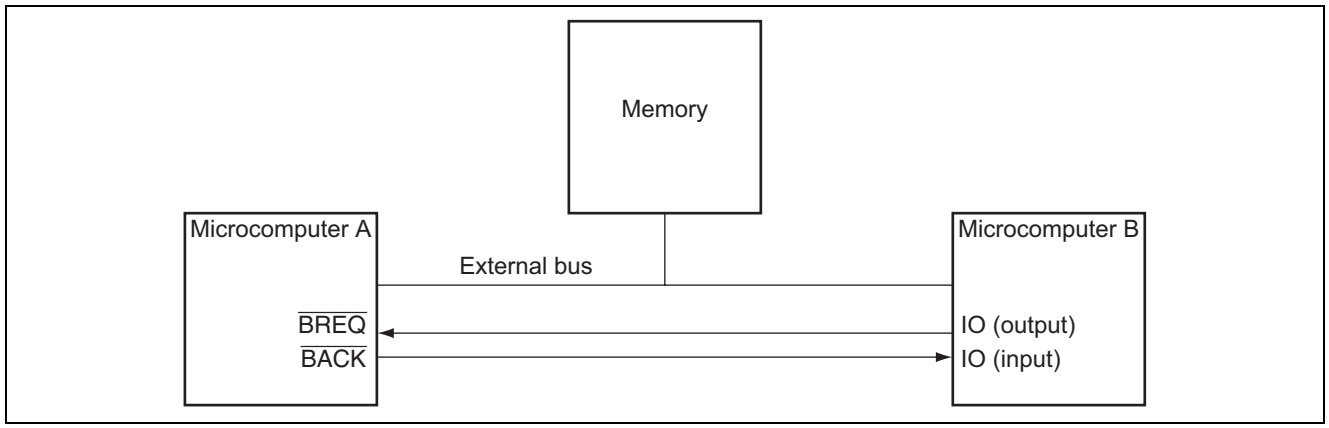
The bus cycle can be extended by inserting program wait states with the subroutine com_bus_area_control. When the bus cycle is not stable due to external factors, wait states must be controlled externally. For example, in the case of the shared memory with the following configuration, the microcomputer A must wait if the microcomputer B is accessing the memory. In such case, the microcomputer A is set to wait state by holding the WAIT pin at low level until the microcomputer B finishes its access. The WAIT pin can be easily enabled/disabled with the subroutine com_bus_hw_wait_control provided in this Application Note.

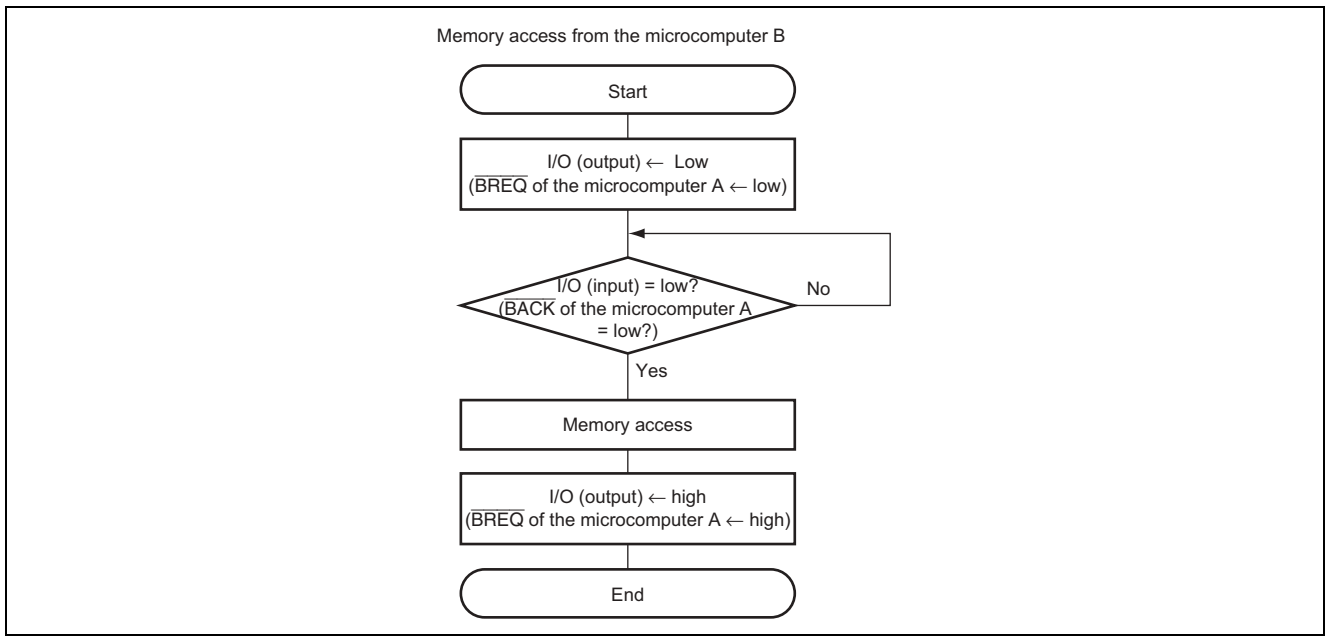


3.5.6 Bus Release Function

The bus can be released in response to a bus release request from the external device. When the $\overline{\text{BREQ}}$ pin is driven low, the $\overline{\text{BACK}}$ pin is driven low at the end of the bus cycle, and the address bus, the data bus, and the bus control signal are placed in the high-impedance state, establishing the external bus released state. In the external bus released state, external bus access by the microcomputer is suspended. When the $\overline{\text{BREQ}}$ pin is driven high, the $\overline{\text{BACK}}$ pin is driven high at the end of the bys cycle to cancel the external bus released state, and the suspended bus access is resumed.

With this function, simple memory sharing can be implemented. For example, in the case of the shared memory with the following configuration, the microcomputer A must wait if the microcomputer B is accessing the memory. In such case, the microcomputer B must drive the $\overline{\text{BREQ}}$ pin in the microcomputer A to be low and confirm that the $\overline{\text{BACK}}$ pin is driven low prior to memory access, and the microcomputer B then accesses memory, and drives the $\overline{\text{BREQ}}$ pin in the microcomputer A back to high after the access ends. This allows prevention of memory access conflicts between the microcomputers A and B. The $\overline{\text{BREQ}}$ and $\overline{\text{BACK}}$ pins can be easily enabled/disabled with the subroutine com_bus_release_control provided in this Application Note.





3.5.7 USB Area

The area 6 of the H8S/2215 is for the USB in operating modes 4 to 6. Therefore, the bus controller must be set as follows for area 6.

To use the USB, the following setting is necessary since the microcomputer is not set as follows after a reset.

Item	Setting	Setting
Bus width	8 bits	com_bus_area_control (BUS_AREA_0, BUS_8BIT, BUS_STATE_3, BUS_WAIT_0)
Number of access states	3 states	
Number of program wait states	0 state	

3.6 List of Registers Used

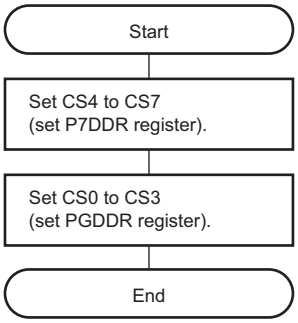
The internal registers of the H8 microcomputer used in the sample program are listed below. For detailed information, refer to the H8S/2215 Hardware Manual.

Name	Summary
Bus width control register (ABWCR)	Specifies bus width (8/16 bits) for areas 0 to 7
Access state control register (ASTCR)	Specifies the number of access states (2/3 states) for areas 0 to 7
Wait control register (WCRH, WCRL)	Selects the number of program wait states to be inserted
Bus control register H (BCRH)	Selects idle cycle insertion conditions Selects burst ROM mode for area 0
Bus control register L (BCRL)	Enables/disables external bus release Enables/disables wait input on the $\overline{\text{WAIT}}$ pin
Pin control register (PFCR)	Sets address bus output enabled range

3.7 Flowchart

Processing flow of the sample program is shown below.

Enabling/disabling of CS signal:
Should be performed in the initial setting routine of the microcomputer.
Only enable the CS signals to be used according to the system configuration.



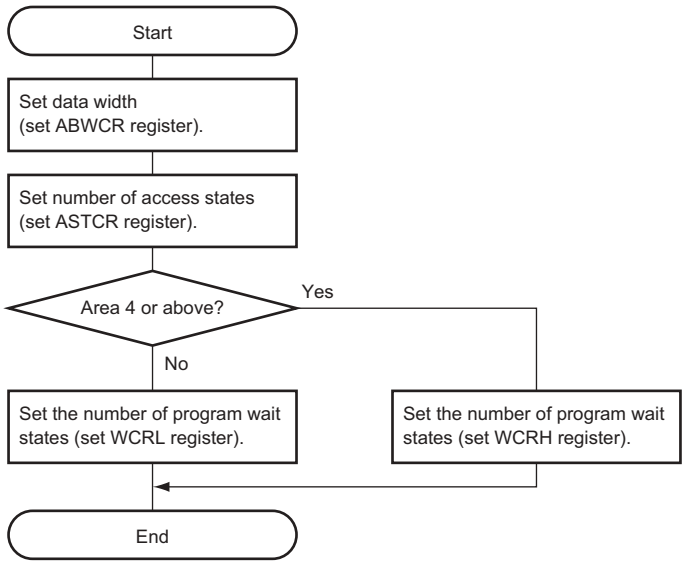
• P7DDR

Bit	Contents
7 to 5	Reserved
4	1: Output port 0: Input port
3	1: CS7 is enabled 0: Input port
2	1: CS6 is enabled 0: Input port
1	1: CS5 is enabled 0: Input port
0	1: CS4 is enabled 0: Input por

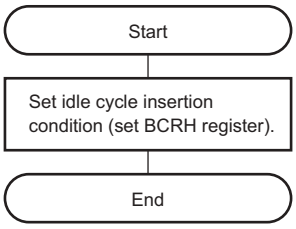
• PGDDR

Bit	Contents
7 to 5	Reserved
4	1: CS0 is enabled 0: Input port
3	1: CS1 is enabled 0: Input port
2	1: CS2 is enabled 0: Input port
1	1: CS3 is enabled 0: Input port
0	1: Output port 0: Input port

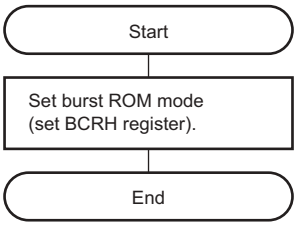
void com_bus_area_control
(int area_no, int bus_width, int state_num, int wait_num)
: Sets bus controller mode for each area.
area_no: Specifies an area
bus_width: Selects bus data width
state_num: Specifies the number of access states
wait_num: Specifies the number of wait states



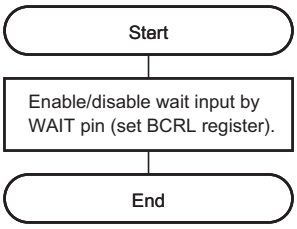
void com_bus_idle_cycle_mode (int idle_cycle_mode)
: Specifies idle cycle insertion conditions.
idle_cycle_mode: Specifies idle cycle insertion



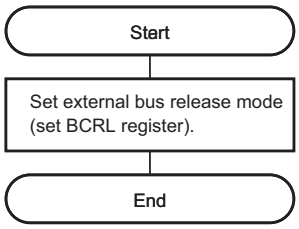
void com_bus_burst_rom_mode (int burst_rom_mode)
: Sets burst ROM mode for area 0.
burst_rom_mode: Sets burst ROM mode



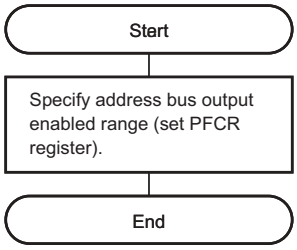
void com_bus_hw_wait_control (int hw_wait_control)
: Enables/disables wait input by WAIT pin.
hw_wait_control: Enables/disables wait input on WAIT pin



void com_bus_release_control (int bus_release_control)
: Sets external bus release mode.
bus_release_control: Sets external bus release mode



void com_bus_address_control (int address_control)
: Specifies address bus output enabled range.
address_control: Specifies address bus output enabled range



4. Reference Documents

- H8S/2215 Series Hardware Manual (published by Renesas Technology Corp.)

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.16, 2004	—	First edition issued

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