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April 1st, 2010
Renesas Electronics Corporation

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H8S Family

Using the HCAN (3): Extended Format, One Byte of Data

Introduction

The Controller Area Network (HCAN) module is used to control the Controller Area Network (CAN), which provides a means for real-time communications in automobiles and industrial equipment systems.

This application note presents an example of communications operation using the H8S/2636's on-chip HCAN module and is offered to users for reference in the software and hardware design processes.

Although the operation of the sample application and programs provided in this application note has been confirmed, please verify operation in your environment before actually using them.

Target Device

H8S/2636

Contents

1. Specifications

Between two H8S/2636 devices, one byte of data is transmitted and received in an extended format message.

(1) Specifications common to the transmitter and receiver

- Channel 0 (HCAN0) is used
- Baud rate: 250 Kbps (in 20-MHz operation)
- Message identifier consists of a standard identifier of H'555 and extended identifier of H'2AAAA.

(2) Specifications of the transmitter

- Uses mailbox 1
- Data length is one byte, and data for transmission is H'AA
- Polls the transmission-complete flag during transmission
- After confirming that the transmission-complete flag has been set, clears the flag as the final operation

(3) Specifications of the receiver

- Uses mailbox 0
- Sets the message identifier masks so that messages are only received if the identifier matches the mask setting
- Uses the bus-operation interrupt and reception interrupt
- By the reception interrupt routine, stores the received data to on-chip RAM and then puts the HCAN in sleep mode

2. Functional Descriptions of the Transmitter and Receiver

Table 1 lists the function assignment of the relevant pins and registers.

Table 1 Function Assignment for the HCAN Module

Pin Usage		Function
Pin	HTxD0	Used for message transmission by the HCAN module (pin 97)
	HRxD0	Used for message reception by the HCAN module (pin 98)

Relevant Registers		Function
Registers common to transmission and reception	MSTPCRC	Module stop control register C Takes HCAN0 out of the module stop mode.
	IRR	Interrupt register Indicates the states of individual interrupt sources.
	BCR	Bit configuration register Configures the baud-rate prescaler for CAN and sets up the bit-timing parameters.
	MBCR	Mailbox configuration register Configures mailboxes for transmission or reception.
	MCR	Master control register Controls the CAN interface.
	GSR	General status register Indicates the CAN bus states.
	MCx[n]	Message control registers (x = mailbox number)
	n = 1	Sets the data length for data frames and remote frames.
	n = 2 to 4	Reserved
	n = 5	Holds standard ID bits (STD_ID2 to STD_ID0), extended ID bits (EXD_ID17 and EXD_ID16), RTR (indicates data frame or remote frame), and IDE (indicates standard format or extended format).
	n = 6	Holds standard ID bits (STD_ID10 to STD_ID3)
	n = 7	Holds extended ID bits (EXD_ID7 to EXD_ID0)
	n = 8	Holds extended ID bits (EXD_ID15 to EXD_ID8)
	MDx[n]	Message data registers (x = mailbox number)
	n = 1 to 8	Hold CAN message data for transmission or received CAN message data.
Transmission-related registers	TXPR	Transmit wait register After a message for transmission has been stored in the mailbox, the corresponding bit in this register is set, indicating a transmission-wait state.
	TXACK	Transmit acknowledge register Each bit in this register indicates whether or not the message in the corresponding mailbox has been transmitted normally.
Reception-related registers	RXPR	Receive complete register Each bit in this register indicates that a message has been received normally in the corresponding mailbox.
	LAFMH, LAFML	Local acceptance filter mask H, L Identifier filter mask settings for the mailboxes configured for reception.

Relevant Registers		Function
Interrupt-related registers	MBIMR	Mailbox interrupt mask register Enables or disables interrupt requests for the individual mailboxes.
	IMR	Interrupt mask register Enables or disables interrupt requests by the IRR interrupt flag.
	IPRM	Interrupt priority register Sets the priority level for HCAN interrupts.
	SYSCR	System control register Sets the interrupt control mode.

3. Flowchart for the Transmitter

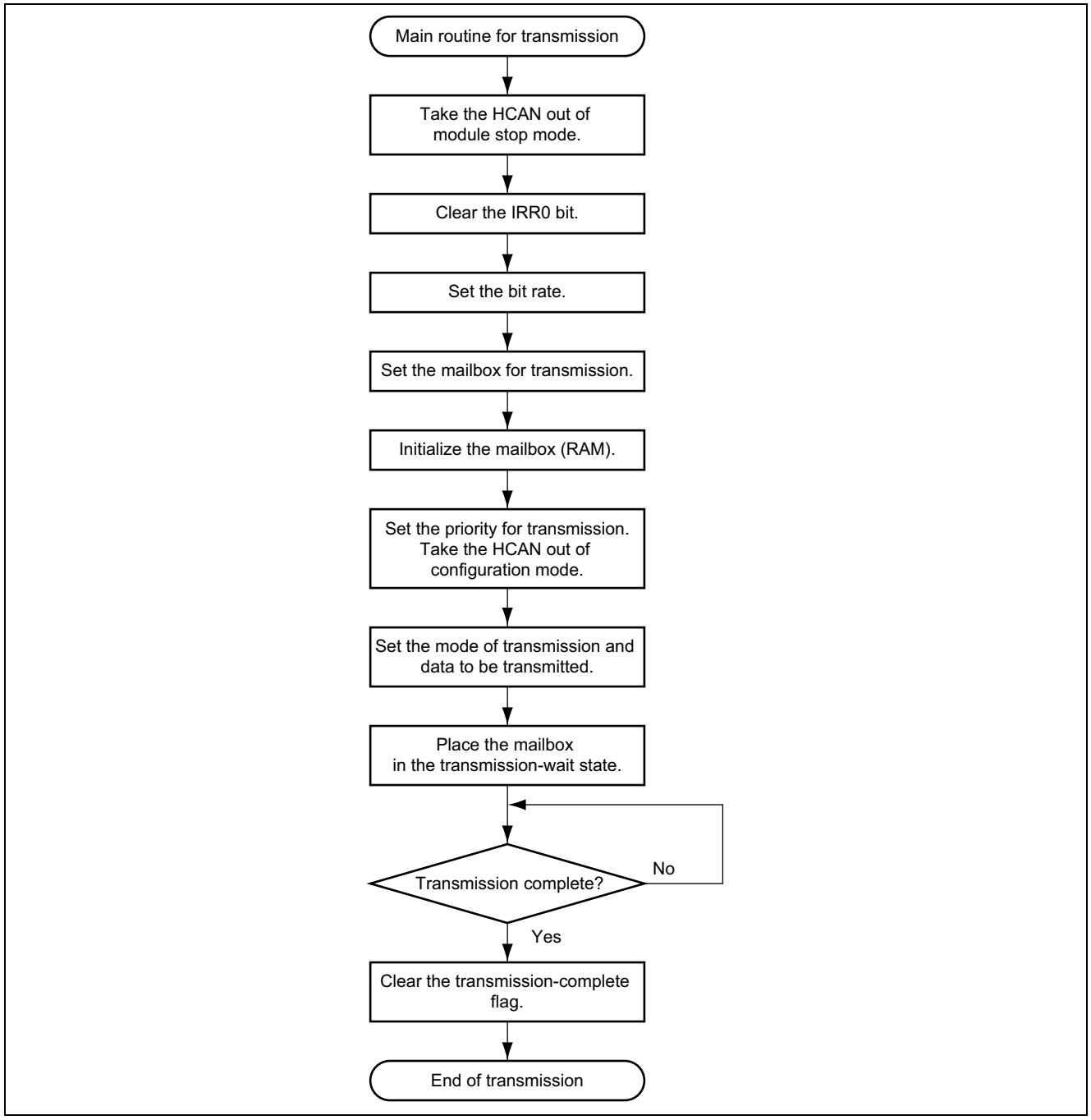

Figure 1 Flowchart for the Transmitter

4. Description of Software (Transmitter)

4.1 Module

Table 2 Description of Module

Module	Label	Function
Main Routine	t_main	Initialize the HCAN and makes settings for transmission.

4.2 Registers

Table 3 Description of Registers*

Register	Function	Setting	Used in
MSTP.CRC.BYTE	Takes HCAN0 out of module stop mode.	H'F7	Main routine
HCAN0.IRR.WORD	The reset interrupt flag in this register is cleared. (Clearing condition: writing a 1 to the bit)	H'0100	
HCAN0.BCR.WORD	Sets the bit rate to 250 Kbps when ϕ = 20 MHz	H'0334	
HCAN0.MBCR.WORD	Sets mailbox 1 for transmission.	H'FDFF	
HCAN0.MCR.BYTE	Selects transmission in mailbox-number order and takes the HCAN module out of configuration mode.	H'04	
HCAN0.GSR.BYTE	Checked to confirm that HCAN0 is out of configuration mode.	—	
HCAN0.MC[1][4]	For mailbox 1, sets the frame type to data frame and the frame format to extended format. Also holds the message identifier bits STD_ID2 to STD_ID0 (for standard ID = H'555) and EXD_ID17 and EXD_ID16 (for extended ID = H'2AAAA).	H'AA	
HCAN0.MC[1][5]	Holds the message identifier bits, STD_ID10 to STD_ID3 (for standard ID = H'555).	H'AA	
HCAN0.MC[1][6]	Holds the message identifier bits, EXD_ID7 to STD_ID0 (for extended ID = H'2AAAA).	H'AA	
HCAN0.MC[1][7]	Holds the message identifier bits, EXD_ID15 to STD_ID8 (for extended ID = H'2AAAA).	H'AA	
HCAN0.MC[1][0]	Sets the data length for transmission from mailbox 1 to one byte.	H'01	
HCAN0.MD[1][0]	Holds the data for transmission from mailbox 1.	H'AA	
HCAN0.TXPR.WORD	Places mailbox 1 in the transmission-wait state.	H'0200	
HCAN0.TXACK.WORD	Checked to see if the transmission-complete flag for mailbox 1 is set; when set, the flag is cleared. (Clearing condition: writing a 1 to the bit)	H'0200	

Note: * The register names shown above are defined in a header file which is available for downloading from the following web page.
http://download.renesas.com/eng/mpumcu/sample_codes/h8sx_h8s_h8_family/io_register/index.html

5. Program Listing (Transmission)

```
/*****************************************************************************************/
/*  HCAN Transmission Program (No.3)                                                     */
/*****************************************************************************************/
#include <stdio.h>                          /* Header file for library functions         */
#include <machine.h>                        /* Header file for library functions         */
#include "2636S.h"                          /* Header file of peripheral register definitions  */

void t_main(void){
    unsigned char i,j;
/* Initialization  */
    MSTP.CRC.BYTE = 0xF7;                   /* Cancel module stop mode of HCAN           */
    HCAN0.IRR.WORD = 0x0100;                /* Initialize reset flag for HCAN module     */
    HCAN0.BCR.WORD = 0x0334;                /* Bit rate: 250 kbps                        */
    HCAN0.MBCR.WORD = 0xFDFF;               /* Set mailbox 1 for transmission            */
    for(i=0; i<=15; i++){                   /* Initialize mailboxes (RAM)                */
        for(j=0; j<=7; j++){
            HCAN0.MC[i][j] = 0x00;
        }
    }
    for(i=0; i<=15; i++){                   /* Initialize mailboxes (RAM)                */
        for(j=0; j<=7; j++){
            HCAN0.MD[i][j] = 0x00;
        }
    }
    HCAN0.MCR.BYTE = 0x04;                  /* Transmission in mailbox No. order;        */
                                            /*                             cancel config. mode */
    while(HCAN0.GSR.BYTE & 0x08);           /* Configuration mode cancellation check     */

/* Transmit data setting */
    HCAN0.MC[1][4] = 0xAA;                  /* Extended format, data frame, and          */
                                            /*                               identifier setting */
    HCAN0.MC[1][5] = 0xAA;                  /* Identifier setting                        */
    HCAN0.MC[1][6] = 0xAA;                  /* Identifier setting                        */
    HCAN0.MC[1][7] = 0xAA;                  /* Identifier setting                        */
    HCAN0.MC[1][0] = 0x01;                  /* Data length: 1 byte                       */
    HCAN0.MD[1][0] = 0xAA;                  /* Message data: 10101010                    */
/* Message transmission */
    HCAN0.TXPR.WORD = 0x0200;               /* Place mailbox 1 in a transmission wait state  */
    while((HCAN0.TXACK.WORD & 0x0200) != 0x0200);
/* Transmission-complete flag clearing */
    HCAN0.TXACK.WORD &= 0x0200;             /* Clear transmission-complete flag          */
    while(1);
}
```

6. Flowchart for the Receiver

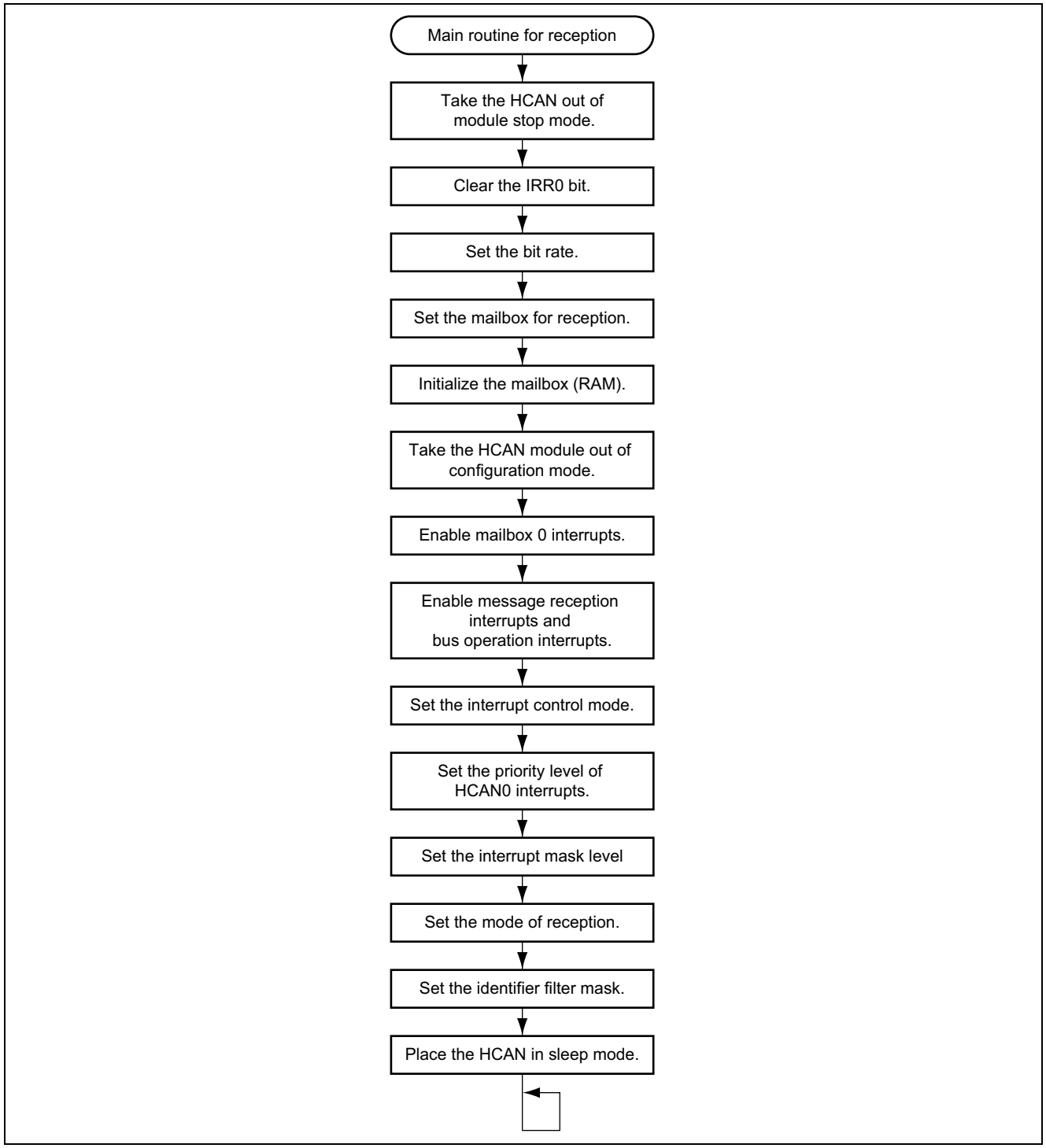

Figure 2 Flowchart for the Receiver

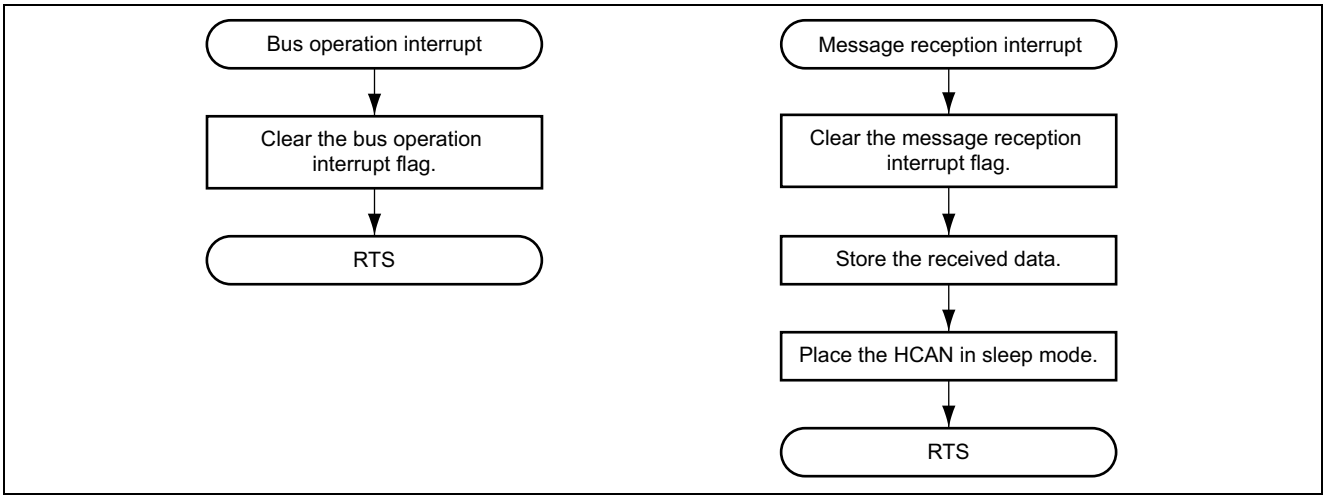

Figure 3 Flowchart of Interrupt Routines for the Receiver

7. Description of Software (Receiver)

7.1 Modules

Table 4 Description of Modules

Module	Label	Function
Main Routine	r_main	Initializes the HCAN and makes settings for reception.
Bus operation interrupt routine	OVR0_IRR12	Clears the bus operation interrupt flag.
Message reception interrupt routine	RM0	Clears the reception flag, stores the received data, and then places the HCAN in sleep mode.

7.2 Registers

Table 5 Description of Registers*

Register	Function	Setting	Used in
MAIL_BOX0	Storage for the received data (Address: H'FFE000)	—	Main routine
MSTP.CRC.BYTE	Takes HCAN0 out of module stop mode.	H'F7	
HCAN0.IRR.WORD	The reset interrupt flag in this register is cleared. (Clearing condition: writing a 1 to the bit)	H'0100	
HCAN0.BCR.WORD	Sets the bit rate to 250 Kbps when ϕ = 20 MHz	H'0334	
HCAN0.MBCR.WORD	Sets mailbox 0 for reception.	H'0100	
HCAN0.MCR.BYTE	Takes HCAN0 out of configuration mode and places it in sleep mode.	H'FE and H'A0	
HCAN0.GSR.BYTE	Checked to confirm that HCAN0 is out of configuration mode.	—	
HCAN0.MBIMR.WORD	Enables interrupt requests of mailbox 0.	H'FEFF	
HCAN0.IMR.WORD	Enables message reception and bus operation interrupts.	H'FCEF	
SYSCR.BYTE	Sets the interrupt control mode.	H'20	
INTC.IPRM.BYTE	Sets the priority level of HCAN interrupts.	H'07	

Register	Function	Setting	Used in
HCAN0.MC[0][4]	For mailbox 0, sets the frame type to data frame and the frame format to extended format. Also holds the message identifier bits STD_ID2 to STD_ID0 (for standard ID = H'555) and EXD_ID17 and EXD_ID16 (for extended ID = H'2AAAA).	H'AA	Main routine
HCAN0.MC[0][5]	Holds the message identifier bits, STD_ID10 to STD_ID3 (for standard ID = H'555).	H'AA	
HCAN0.MC[0][6]	Holds the message identifier bits, EXD_ID7 to STD_ID0 (for extended ID = H'2AAAA).	H'AA	
HCAN0.MC[0][7]	Holds the message identifier bits, EXD_ID15 to STD_ID8 (for extended ID = H'2AAAA).	H'AA	
HCAN0.LAFMH.WORD	Mailbox 0 receives data if all identifier bits match.	H'0000	
HCAN0.LAFML.WORD	Mailbox 0 receives data if all identifier bits match.	H'0000	
HCAN0.IRR.WORD	The bus-operation interrupt flag in this register is cleared.	H'0010	Reception interrupt routine
HCAN0.RXPR.WORD	The reception-complete flag for mailbox 0 in this register is cleared. (Clearing condition: writing a 1 to the bit)	H'FFFF	
HCAN_IMR	Enables message reception interrupts.	H'FFFD	
HCAN_MBIMR0	Enables mailbox 0 interrupt requests.	H'FFFE	

Note: * The register names shown above are defined in a header file which is available for downloading from the following web page.
http://download.renesas.com/eng/mpumcu/sample_codes/h8sx_h8s_h8_family/io_register/index.html

8. Program Listing (Reception)

```
/*****************************************************************************************/
/*  HCAN Reception Program (No.3)                                                        */
/*****************************************************************************************/
#include <stdio.h>                          /* Header file for library functions         */
#include <machine.h>                        /* Header file for library functions         */
#include "2636S.h"                          /* Header file of peripheral register definitions  */

/*****************************************************************************************/
/*  Definitions of Constants                                                             */
/*****************************************************************************************/
#define MAIL_BOX0 (*(unsigned char  *)0xFFE000)
                                            /* Received data storage for mailbox 0       */

void r_main(void){
    unsigned char i,j;
/* Initialization */
    MSTP.CRC.BYTE = 0xF7;                   /* Cancel module stop mode of HCAN           */
    HCAN0.IRR.WORD = 0x0100;                /* Initialize reset flag for HCAN module     */
    HCAN0.BCR.WORD = 0x0334;                /* Bit rate: 250 kbps                        */
    HCAN0.MBCR.WORD = 0x0100;               /* Set mailbox 0 for reception               */
    for(i=0; i<=15; i++){                   /* Initialize mailboxes (RAM)                */
        for(j=0; j<=7; j++){
            HCAN0.MC[i][j] = 0x00;
        }
    }
    for(i=0; i<=15; i++){                   /* Initialize mailboxes (RAM)                */
        for(j=0; j<=7; j++){
            HCAN0.MD[i][j] = 0x00;
        }
    }
    HCAN0.MCR.BYTE &= 0xFE;                 /* Cancel configuration mode                 */
    while(HCAN0.GSR.BYTE & 0x08);           /* Configuration mode cancellation check     */
/* Interrupt settings */
    HCAN0.MBIMR.WORD = 0xFEFF;              /* Enable mailbox 0 interrupt requests       */
    HCAN0.IMR.WORD = 0xFCEF;                /* Enable message reception and              */
                                            /*                        bus operation interrupts */
    SYSCR.BYTE |= 0x20;                     /* Set interrupt control mode 2              */
    INTC.IPRM.BYTE = 0x07;                  /* Set the priority level of HCAN0 interrupts to 7 */
    set_imask_exr(0);                       /* Set interrupt request mask level          */
/* Reception data settings */
    HCAN0.MC[0][4] = 0xAA;                  /* Extended format, data frame, and          */
                                            /*                              identifier setting */
    HCAN0.MC[0][5] = 0xAA;                  /* Identifier setting                        */
    HCAN0.MC[0][6] = 0xAA;                  /* Identifier setting                        */
    HCAN0.MC[0][7] = 0xAA;                  /* Identifier setting                        */
    HCAN0.LAFMH.WORD = 0x0000;              /* Mailbox 0 receives data                   */
                                            /*                     if all identifier bits match */
    HCAN0.LAFML.WORD = 0x0000;              /* Mailbox 0 receives data                   */
                                            /*                     if all identifier bits match */
```

```
/* HCAN sleep mode settings */
    HCAN0.MCR.BYTE |= 0xA0;                 /* Put HCAN in sleep mode;                          */
                                            /*      enable recovery by bus-operation interrupt */
    while(1);
}
/*****************************************************************************************/
/*  Bus-Operation Interrupt Routine                                                      */
/*****************************************************************************************/
#pragma interrupt(OVR0_IRR12)
void OVR0_IRR12(void){
    HCAN0.IRR.WORD &= 0x0010;               /* Clear IRR12 (bus-operation interrupt flag)      */
}
/*****************************************************************************************/
/*  Message Reception Interrupt Routine                                                  */
/*****************************************************************************************/
#pragma interrupt(RM0)
void RM0(void){
    HCAN0.RXPR.WORD &= 0xFFFF;              /* Clear IRR1(reception message interrupt flag)    */
    MAIL_BOX0 = HCAN0.MD[0][0];             /* Store received data                             */
/* HCAN sleep mode setting */
    HCAN0.MCR.BYTE |= 0x20;                 /* Put HCAN in sleep mode                          */
}
```

9. Waveforms during Operation (Transmission and Reception)

Figure 4 shows the waveforms seen during the execution of this application.

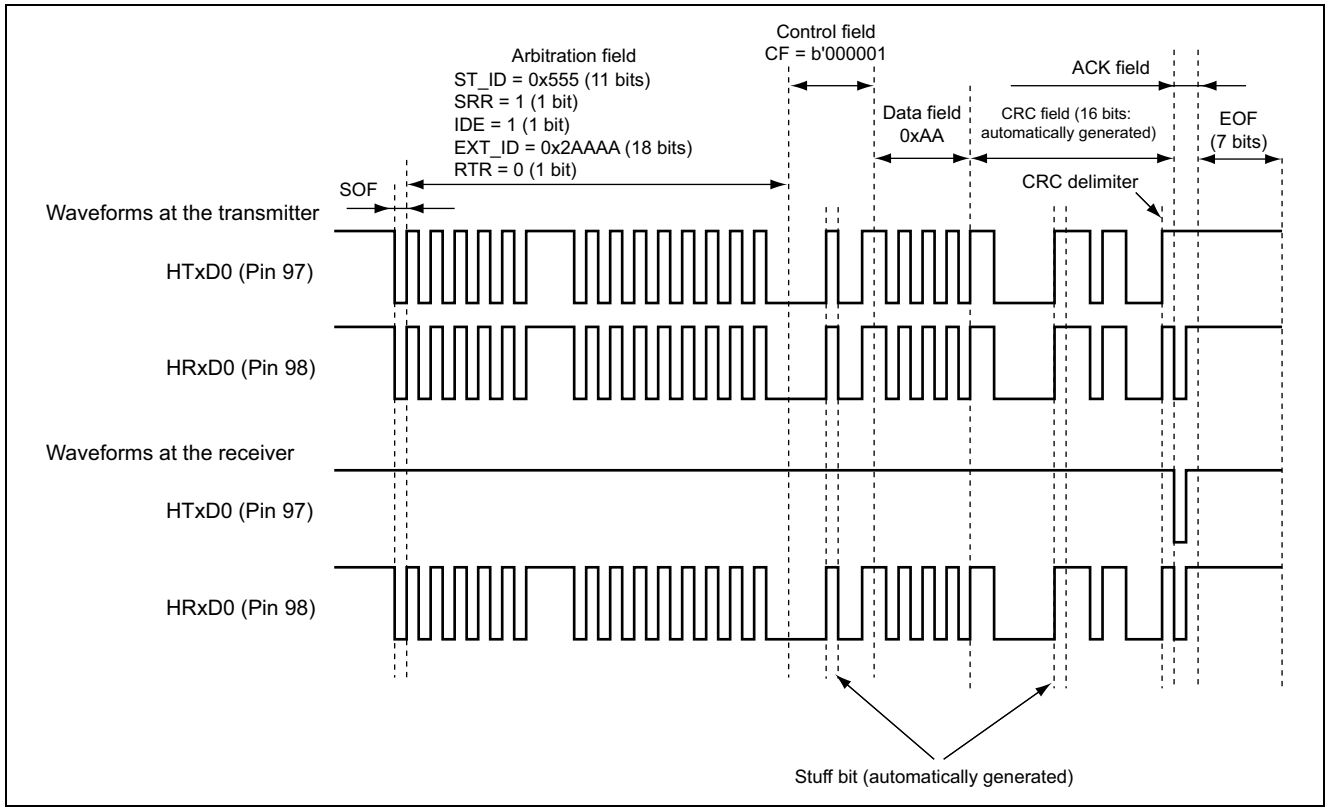

Figure 4 Waveforms during Operation

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Jul.22.05	—	First edition issued

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