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# H8S Family

## Using the HCAN (2): Standard Format, 8 Bytes of Data, DTC in Use

### Introduction

The Controller Area Network (HCAN) module is used to control the Controller Area Network (CAN), which provides a means for real-time communications in automobiles and industrial equipment systems.

This application note presents an example of communications operation using the H8S/2636's on-chip HCAN module and is offered to users for reference in the software and hardware design processes.

Although the operation of the sample application and programs provided in this application note has been confirmed, please verify operation in your environment before actually using them.

### Target Device

H8S/2636

### Contents

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3. Flowchart for the Transmitter ..... 5
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9. Waveforms during Operation (Transmission and Reception) ..... 14

# 1. Specifications

Between two H8S/2636 devices, eight bytes of data are transmitted and received in a standard format message. The data transfer controller (DTC) is used to store the received data.

**(1) Specifications common to the transmitter and receiver**

- Channel 0 (HCAN0) is used
- Baud rate: 250 Kbps (in 20-MHz operation)
- Message identifier: H'555

**(2) Specifications of the transmitter**

- Uses mailbox 1
- Data length is eight bytes, and data for transmission are H'55, H'66, H'77, H'88, H'99, H'AA, H'BB and H'FF
- Polls the transmission-complete flag during transmission
- After confirming that the transmission-complete flag has been set, clears the flag as the final operation

**(3) Specifications of the receiver:**

- Uses mailbox 0
- Sets the message identifier mask so that messages are only received if the identifier matches the mask setting
- Uses the receive message interrupt (IRRI)
  (a) The DTC is activated on a receive message interrupt and stores the received data in on-chip RAM.
  (b) The DTC is used in block-transfer mode, and transfers one block consisting of eight bytes.
  (c) After the DTC transfer has ended, the receive message interrupt routine clears the reception-complete flag and disables the receive message interrupt, after which the operation is over.

## 2. Functional Descriptions of the Transmitter and Receiver

Tables 1 and 2 list the function assignments of the relevant pins and registers.

**Table 1 Function Assignment for the HCAN Module**

| Pin Usage | | Function |
|---|---|---|
| Pin | HTxD0 | Used for message transmission by the HCAN module (pin 97) |
| | HRxD0 | Used for message reception by the HCAN module (pin 98) |

| Relevant Registers | | Function |
|---|---|---|
| Registers common to transmission and reception | MSTPCRC | Module stop control register C<br>Takes HCAN0 out of the module stop mode. |
| | IRR | Interrupt register<br>Indicates the states of individual interrupt sources. |
| | BCR | Bit configuration register<br>Configures the baud-rate prescaler for CAN and sets up the bit-timing parameters. |
| | MBCR | Mailbox configuration register<br>Configures mailboxes for transmission or reception. |
| | MCR | Master control register<br>Controls the CAN interface. |
| | GSR | General status register<br>Indicates the CAN bus states. |
| | MCx[n] | Message control registers (x = mailbox number) |
| | n = 1 | Sets the data length for data frames and remote frames. |
| | n = 2 to 4 | Reserved |
| | n = 5 | Holds standard ID bits (STD_ID2 to STD_ID0), extended ID bits (EXD_ID17 and EXD_ID16), RTR (indicates data frame or remote frame), and IDE (indicates standard format or extended format). |
| | n = 6 | Holds standard ID bits (STD_ID10 to STD_ID3) |
| | n = 7 | Holds extended ID bits (EXD_ID7 to EXD_ID0) |
| | n = 8 | Holds extended ID bits (EXD_ID15 to EXD_ID8) |
| | MDx[n] | Message data registers (x = mailbox number) |
| | n = 1 to 8 | Hold CAN message data for transmission or received CAN message data. |
| Transmission-related registers | TXPR | Transmit wait register<br>After a message for transmission has been stored in the mailbox, the corresponding bit in this register is set, indicating a transmission-wait state. |
| | TXACK | Transmit acknowledge register<br>Each bit in this register indicates whether or not the message in the corresponding mailbox has been transmitted normally. |
| Reception-related registers | RXPR | Receive complete register<br>Each bit in this register indicates that a message has been received normally in the corresponding mailbox. |
| | LAFMH, LAFML | Local acceptance filter mask H, L<br>Identifier filter mask settings for the mailboxes configured for reception. |

| Relevant Registers | | Function |
|---|---|---|
| Interrupt-related registers | MBIMR | Mailbox interrupt mask register<br>Enables or disables interrupt requests for the individual mailboxes. |
| | IMR | Interrupt mask register<br>Enables or disables interrupt requests by the IRR interrupt flag. |
| | IPRM | Interrupt priority register<br>Sets the priority level for HCAN interrupts. |
| | SYSCR | System control register<br>Sets the interrupt control mode. |

**Table 2 Function Assignment for the DTC**

| DTC-Related Registers | Function |
|---|---|
| MSTPCRA | Module stop control register A<br>Takes the DTC out of module stop mode. |
| MRA, MRB | DTC mode register A, B<br>Control the operating mode of the DTC. |
| SAR | DTC source address register<br>Specifies the address of the source data area for DTC transfer. |
| DAR | DTC destination address register<br>Specifies the address of the destination data area for DTC transfer. |
| CRA | DTC transfer count register A<br>Specifies the number of data transfers by the DTC. |
| CRB | DTC transfer count register B<br>In block transfer mode, specifies the block length. |
| DTCERA to DTCERG | DTC enable register<br>Selects the interrupt source that activates the DTC. |
| DTVECR | DTC vector register<br>Enables or disables activation of the DTC by software and sets the vector number for the software activation interrupt. |

## 3. Flowchart for the Transmitter

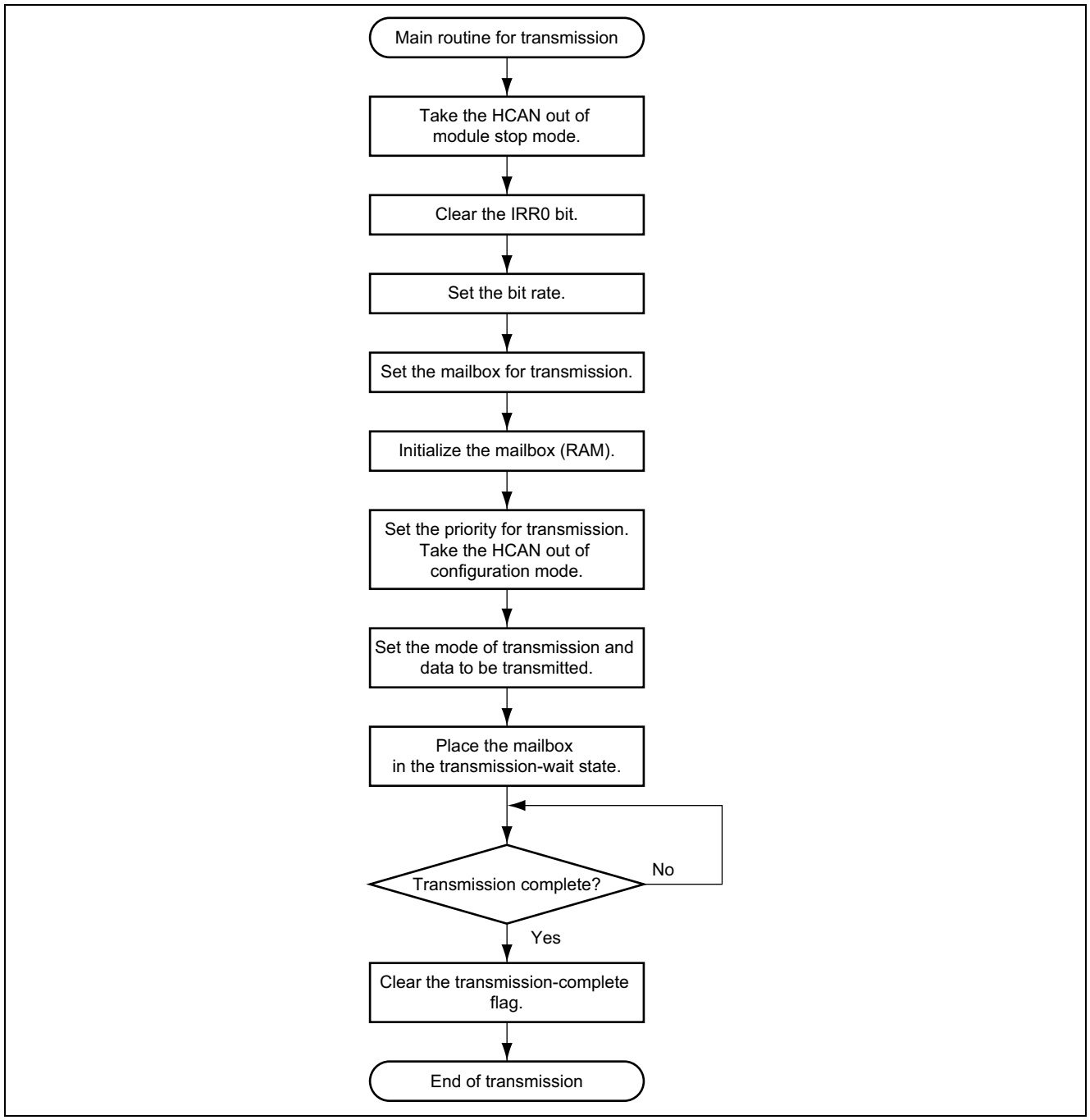


**Figure 1 Flowchart for the Transmitter**

# 4. Description of Software (Transmitter)

## 4.1 Module

**Table 3 Description of Module**

| Module | Label | Function |
|---|---|---|
| Main Routine | t_main | Initialize the HCAN and makes settings for transmission. |

## 4.2 Registers

**Table 4 Description of Registers ***

| Register | Function | Setting | Used in |
|---|---|---|---|
| MSTP.CRC.BYTE | Takes HCAN0 out of module stop mode. | H'F7 | Main routine |
| HCAN0.IRR.WORD | The reset interrupt flag in this register is cleared.<br>(Clearing condition: writing a 1 to the bit) | H'0100 | |
| HCAN0.BCR.WORD | Sets the bit rate to 250 Kbps when $\phi$ = 20 MHz | H'0334 | |
| HCAN0.MBCR.WORD | Sets mailbox 1 for transmission. | H'FDFF | |
| HCAN0.MCR.BYTE | Selects transmission in mailbox-number order and takes the HCAN module out of configuration mode. | H'04 | |
| HCAN0.GSR.BYTE | Checked to confirm that HCAN0 is out of configuration mode. | — | |
| HCAN0.MC[1][4] | For mailbox 1, sets the frame type to data frame and the frame format to standard format.<br>Also holds the message identifier bits, STD_ID2 to STD_ID0 (for message ID = H'555). | H'A0 | |
| HCAN0.MC[1][5] | Holds the message identifier bits, STD_ID10 to STD_ID3 (for message ID = H'555). | H'AA | |
| HCAN0.MC[1][0] | Sets the data length for transmission from mailbox 1 to eight bytes. | H'08 | |
| HCAN0.MD[1][0] | Holds the 1st byte for transmission from mailbox 1. | H'55 | |
| HCAN0.MD[1][1] | Holds the 2nd byte for transmission from mailbox 1. | H'66 | |
| HCAN0.MD[1][2] | Holds the 3rd byte for transmission from mailbox 1. | H'77 | |
| HCAN0.MD[1][3] | Holds the 4th byte for transmission from mailbox 1. | H'88 | |
| HCAN0.MD[1][4] | Holds the 5th byte for transmission from mailbox 1. | H'99 | |
| HCAN0.MD[1][5] | Holds the 6th byte for transmission from mailbox 1. | H'AA | |
| HCAN0.MD[1][6] | Holds the 7th byte for transmission from mailbox 1. | H'BB | |
| HCAN0.MD[1][7] | Holds the 8th byte for transmission from mailbox 1. | H'FF | |
| HCAN0.TXPR.WORD | Places mailbox 1 in the transmission-wait state. | H'0200 | |
| HCAN0.TXACK.WORD | Checked to see if the transmission-complete flag for mailbox 1 is set; when set, the flag is cleared.<br>(Clearing condition: writing a 1 to the bit) | H'0200 | |

Note: * The register names shown above are defined in a header file which is available for downloading from the following web page.
http://download.renesas.com/eng/mpumcu/sample_codes/h8sx_h8s_h8_family/io_register/index.html

## 5. Program Listing (Transmission)

```
/*****************************************************************************************/
/*  HCAN Transmission Program (No.2)                                                     */
/*****************************************************************************************/
#include <stdio.h>                          /* Header file for library functions         */
#include <machine.h>                        /* Header file for library functions         */
#include "2636S.h"                          /* Header file of peripheral register definitions  */

void t_main(void){
    unsigned char i,j;
/* Initialization */
    MSTP.CRC.BYTE = 0xF7;                   /* Cancel module stop mode of HCAN           */
    HCAN0.IRR.WORD = 0x0100;                /* Initialize reset flag for HCAN module     */
    HCAN0.BCR.WORD = 0x0334;                /* Bit rate: 250 kbps                        */
    HCAN0.MBCR.WORD = 0xFDFF;               /* Set mailbox 1 for transmission            */
    for(i=0; i<=15; i++){                   /* Initialize mailboxes (RAM)                */
        for(j=0; j<=7; j++){
            HCAN0.MC[i][j] = 0x00;
        }
    }
    for(i=0; i<=15; i++){                   /* Initialize mailboxes (RAM)                */
        for(j=0; j<=7; j++){
            HCAN0.MD[i][j] = 0x00;
        }
    }
    HCAN0.MCR.BYTE = 0x04;                  /* Transmission in mailbox No. order;        */
                                            /*                             cancel config. mode */
    while(HCAN0.GSR.BYTE & 0x08);           /* Configuration mode cancellation check     */

/* Transmit data setting */
    HCAN0.MC[1][4] = 0xA0;                  /* Standard format, data frame, and          */
                                            /*                              identifier setting */
    HCAN0.MC[1][5] = 0xAA;                  /* Identifier setting                        */
    HCAN0.MC[1][0] = 0x08;                  /* Data length: 8 bytes                      */
    HCAN0.MD[1][0] = 0x55;                  /* Message data: 01010101                    */
    HCAN0.MD[1][1] = 0x66;                  /* Message data: 01100110                    */
    HCAN0.MD[1][2] = 0x77;                  /* Message data: 01110111                    */
    HCAN0.MD[1][3] = 0x88;                  /* Message data: 10001000                    */
    HCAN0.MD[1][4] = 0x99;                  /* Message data: 10011001                    */
    HCAN0.MD[1][5] = 0xAA;                  /* Message data: 10101010                    */
    HCAN0.MD[1][6] = 0xBB;                  /* Message data: 10111011                    */
    HCAN0.MD[1][7] = 0xFF;                  /* Message data: 11111111                    */
/* Message transmission */
    HCAN0.TXPR.WORD = 0x0200;               /* Place mailbox 1 in a transmission wait state  */
    while((HCAN0.TXACK.WORD & 0x0200) != 0x0200);
/* Transmission-complete flag clearing */
    HCAN0.TXACK.WORD &= 0x0200;             /* Clear transmission-complete flag          */
    while(1);
}
```

## 6. Flowchart for the Receiver

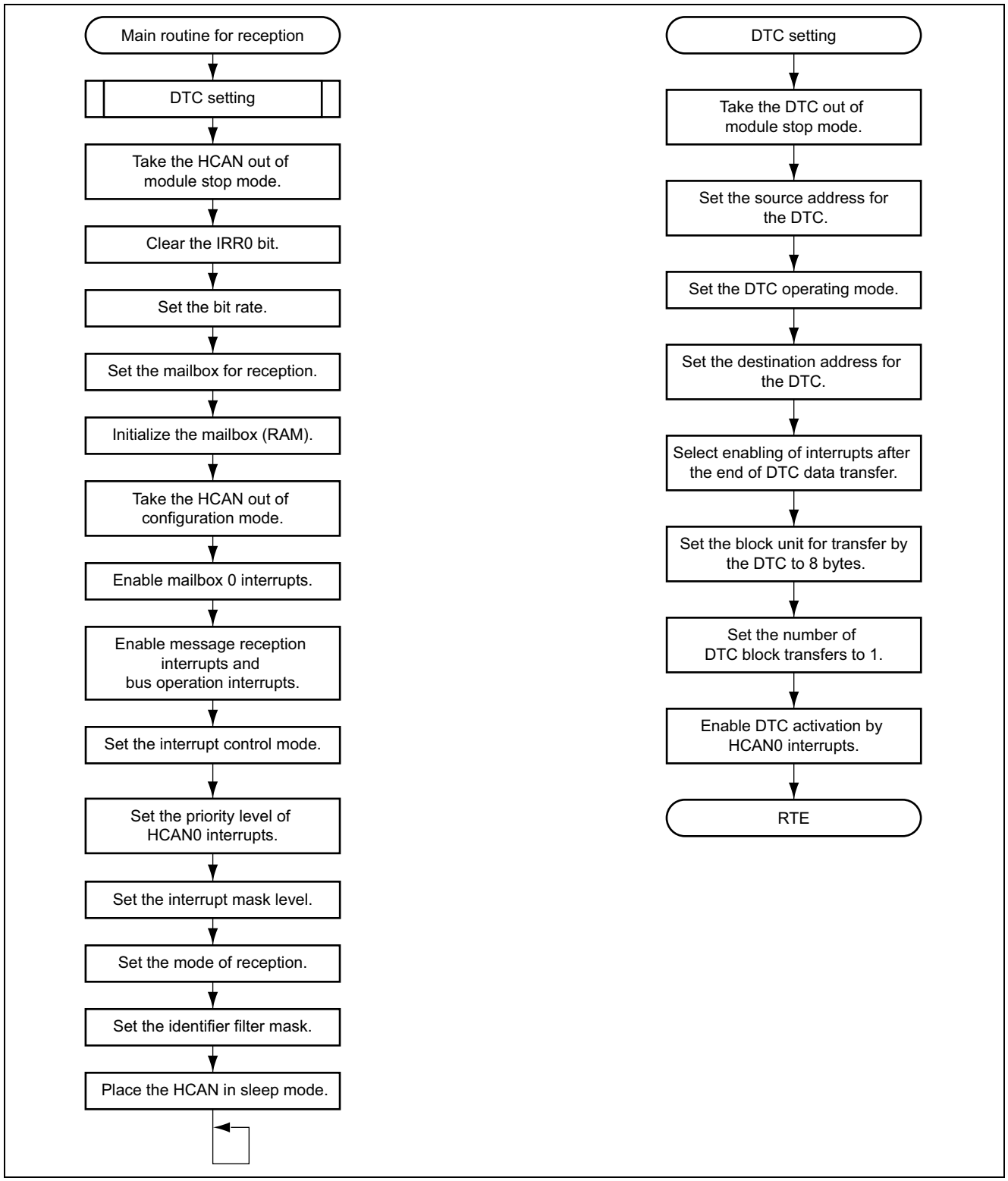


**Figure 2 Flowchart for the Receiver**

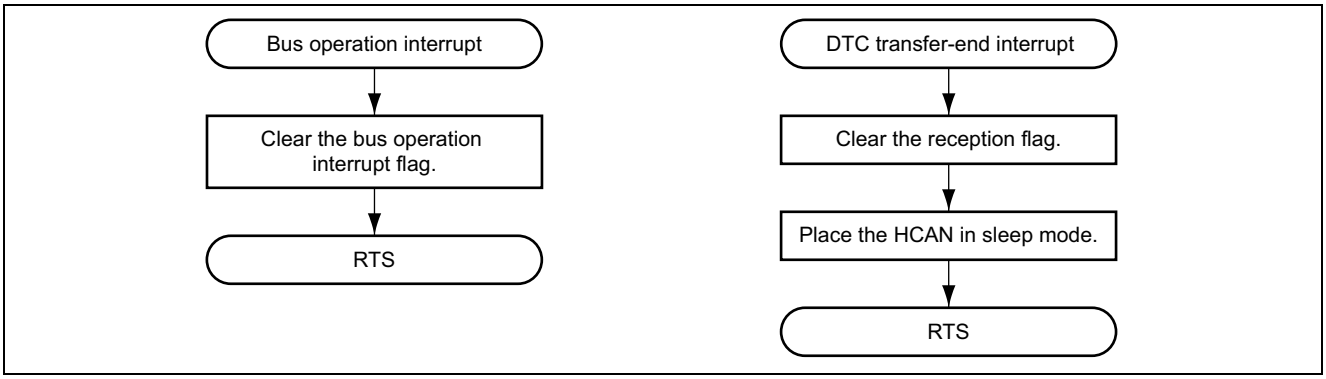


**Figure 3 Flowchart of Interrupt Routines for the Receiver**

# 7. Description of Software (Receiver)

## 7.1 Modules

**Table 5 Description of Modules**

| Module | Label | Function |
|---|---|---|
| Main Routine | r_main | Initializes the HCAN and makes settings for reception. |
| Bus operation interrupt routine | OVR0_IRR12 | Clears the bus operation interrupt flag. |
| DTC transfer-end interrupt routine | DTCend_RM0 | Clears the reception flag and places the HCAN in sleep mode. |

## 7.2 Registers

**Table 6 Description of Registers***

| Register | Function | Setting | Used in |
|---|---|---|---|
| MAILBOX.MDATA[1][8] | Storage for the received data<br>Address range: H'FFE000 to H'FFE007 | — | Main routine |
| MSTP.CRA.BYTE | Takes the DTC out of module stop mode. | H'3F | |
| DTC_SAR | Sets the first address of the message data area for mailbox 0 as the source address for transfer. | H'FFF8B0 | |
| DTC_MRA | Sets the incrementation of both DTC_SAR and DTC_DAR after each transfer, and selects block transfer mode and byte-sized transfer. | H'AA | |
| DTC_DAR | Sets the first address of the received-data storage area as the destination address for transfer. | H'FFE000 | |
| DTC_MRB | Enables interrupts to the CPU after the end of DTC transfer. | H'40 | |
| DTC_CRA | Sets the size of a block (8 bytes). | H'0808 | |
| DTC_CRB | Sets the number of block transfers (one). | H'0001 | |
| DTC.DTCEG.BYTE | Selects the DTC activation source (RM0). | H'04 | |
| MSTP.CRC.BYTE | Takes HCAN0 out of module stop mode. | H'F7 | |
| HCAN0.IRR.WORD | The reset interrupt flag in this register is cleared.<br>(Clearing condition: writing a 1 to the bit) | H'0100 | |
| HCAN0.BCR.WORD | Sets the bit rate to 250 Kbps when $\phi$ = 20 MHz | H'0334 | |
| HCAN0.MBCR.WORD | Sets mailbox 0 for reception. | H'0100 | |
| HCAN0.MCR.BYTE | Takes HCAN0 out of configuration mode and places it in sleep mode. | H'FE and H'A0 | |
| HCAN0.GSR.BYTE | Checked to confirm that HCAN0 is out of configuration mode. | — | |
| HCAN0.MBIMR.WORD | Enables interrupt requests of mailbox 0. | H'FEFF | |
| HCAN0.IMR.WORD | Enables message reception and bus operation interrupts. | H'FCEF | |

| Register | Function | Setting | Used in |
|---|---|---|---|
| SYSCR.BYTE | Sets the interrupt control mode. | H'20 | Main routine |
| INTC.IPRM.BYTE | Sets the priority level of HCAN interrupts. | H'07 | |
| HCAN0.MC[0][4] | For mailbox 0, sets the frame type to data frame and the frame format to standard format.<br>Also holds the message identifier bits, STD_ID2 to STD_ID0 (for message ID = H'555). | H'A0 | |
| HCAN0.MC[0][5] | Holds the message identifier bits, STD_ID10 to STD_ID3 (for message ID = H'555). | H'AA | |
| HCAN0.LAFMH.WORD | Provides the filter mask setting. | H'0000 | |
| HCAN0.IRR.WORD | The bus-operation interrupt flag in this register is cleared. | H'0010 | Reception interrupt routine |
| HCAN0.RXPR.WORD | The reception-complete flag for mailbox 0 in this register is cleared.<br>(Clearing condition: writing a 1 to the bit) | H'FFFF | |

Note: * The register names shown above are defined in a header file which is available for downloading from the following web page.
http://download.renesas.com/eng/mpumcu/sample_codes/h8sx_h8s_h8_family/io_register/index.html

## 8. Program Listing (Reception)

```
/*****************************************************************************************/
/*  HCAN Reception Program (No.2)                                                        */
/*****************************************************************************************/
#include <stdio.h>                          /* Header file for library functions         */
#include <machine.h>                        /* Header file for library functions         */
#include "2636S.h"                          /* Header file of peripheral register definitions  */
/*****************************************************************************************/
/*  Definitions of Constants                                                             */
/*****************************************************************************************/
volatile struct MB{                         /* struct MAILBOX0-15                        */
    unsigned char MDATA[1][8];              /* Storage of received data                  */
};
#define MAILBOX    (*(volatile struct MB *)0xFFE000)
                                            /* First address of received data storage    */
#define DTC_SAR    (*(volatile unsigned long  *)0xFFEBC0) /* DTC register info setting  */
#define DTC_MRA    (*(volatile unsigned char  *)0xFFEBC0) /* DTC register info setting  */
#define DTC_DAR    (*(volatile unsigned long  *)0xFFEBC4) /* DTC register info setting  */
#define DTC_MRB    (*(volatile unsigned char  *)0xFFEBC4) /* DTC register info setting  */
#define DTC_CRA    (*(volatile unsigned short *)0xFFEBC8) /* DTC register info setting  */
#define DTC_CRB    (*(volatile unsigned short *)0xFFEBCA) /* DTC register info setting  */

void r_main(void){
    unsigned char i,j;
/* DTC initialization */
    MSTP.CRA.BYTE = 0x3F;                   /* Cancel module stop mode of DTC            */
    DTC_SAR = (long)(&HCAN0.MD[0][0]);      /* Set transfer source address               */
    DTC_MRA = 0xA8;                         /* SAR and DAR incremented after transfer;   */
                                            /*                          set block transfer mode */
    DTC_DAR = (long)(&MAILBOX.MDATA[0][0]); /* Set transfer destination address (on-chip RAM)  */
    DTC_MRB = 0x40;                         /* Enable interrupt to the CPU after end of  */
                                            /*                                    DTC transfer */
    DTC_CRA = 0x0808;                       /* Block transfer size: 8 bytes              */
    DTC_CRB = 0x0001;                       /* Number of block transfers: 1              */
    DTC.DTCEG.BYTE |= 0x04;                 /* Enable activation of DTC by               */
                                            /*                            HCAN0 interrupt (RM0) */
/* HCAN initialization */
    MSTP.CRC.BYTE = 0xF7;                   /* Cancel module stop mode of HCAN           */
    HCAN0.IRR.WORD = 0x0100;                /* Initialize reset flag for HCAN module     */
    HCAN0.BCR.WORD = 0x0334;                /* Bit rate: 250 kbps                        */
    HCAN0.MBCR.WORD = 0x0100;               /* Set mailbox 0 for reception               */
    for(i=0; i<=15; i++){                   /* Initialize mailboxes (RAM)                */
        for(j=0; j<=7; j++){
            HCAN0.MC[i][j] = 0x00;
        }
    }
    for(i=0; i<=15; i++){                   /* Initialize mailboxes (RAM)                */
        for(j=0; j<=7; j++){
            HCAN0.MD[i][j] = 0x00;
        }
    }
    HCAN0.MCR.BYTE &= 0xFE;                 /* Cancel configuration mode                 */
    while(HCAN0.GSR.BYTE & 0x08);           /* Configuration mode cancellation check     */
```

```
/* Interrupt settings */
    HCAN0.MBIMR.WORD = 0xFEFF;              /* Enable mailbox 0 interrupt requests             */
    HCAN0.IMR.WORD = 0xFCEF;                /* Enable message reception and                    */
                                            /*                          bus operation interrupts */
    SYSCR.BYTE |= 0x20;                     /* Set interrupt control mode 2                    */
    INTC.IPRM.BYTE = 0x07;                  /* Set the priority level of HCAN0 interrupts to 7 */
    set_imask_exr(0);                       /* Set interrupt request mask level                */
/* Reception data settings */
    HCAN0.MC[0][4] = 0xA0;                  /* Standard format, data frame,                    */
                                            /*                            and identifier setting */
    HCAN0.MC[0][5] = 0xAA;                  /* Identifier setting                              */
    HCAN0.LAFMH.WORD = 0x0000;              /* Mailbox 0 receives data if identifier bits match*/
/* HCAN sleep mode setting */
    HCAN0.MCR.BYTE |= 0xA0;                 /* Put HCAN in sleep mode;                         */
                                            /*      enable recovery by bus operation interrupt */
    while(1);
}
/*****************************************************************************************************/
/*  Bus-Operation Interrupt Routine                                                                  */
/*****************************************************************************************************/
#pragma interrupt(OVR0_IRR12)
void OVR0_IRR12(void){
    HCAN0.IRR.WORD &= 0x0010;               /* Clear IRR12 (bus-operation interrupt flag)      */
}
/*****************************************************************************************************/
/*  DTC Transfer-End Interrupt Routine                                                               */
/*****************************************************************************************************/
#pragma interrupt(DTCend_RM0)
void DTCend_RM0(void){
    HCAN0.RXPR.WORD &= 0xFFFF;              /* Clear IRR1 (reception message interrupt flag)   */
/* HCAN sleep mode setting */
    HCAN0.MCR.BYTE |= 0x20;                 /* Put HCAN in sleep mode                          */
}
```

## 9. Waveforms during Operation (Transmission and Reception)

Figure 4 shows the waveforms seen during the execution of this application.

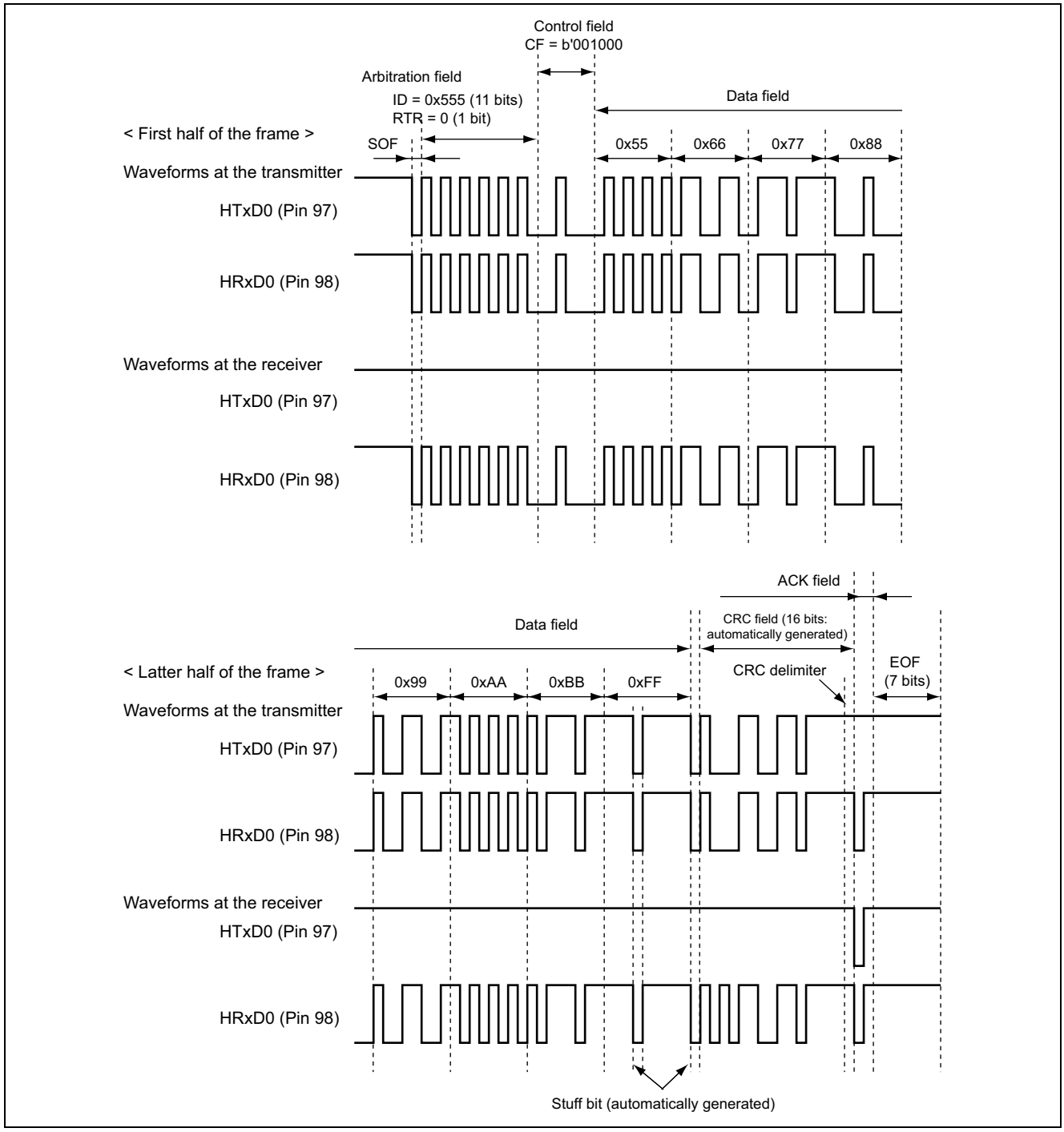


**Figure 4 Waveforms during Operation**

## Revision Record

| | | Description | |
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## Keep safety first in your circuit designs!

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   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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