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Renesas Electronics Corporation

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H8S Family

Using the 8-Bit PWM Function

Introduction

This application note presents an example usage of the 8-bit PWM function of the H8S/2100 Series to implement a D/A converter.

Target Device

H8S/2114

H8S/2111B

H8S/2140B

H8S/2141B

H8S/2160B

H8S/2161B

H8S/2145B

H8S/2189

H8S/2168

H8S/2148

H8S/2138

H8S/2128

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1. Specifications

- The 8-bit PWM module outputs a PWM signal from the PWi (i = 8 to 15) pin. By passing this PWM output signal through a low-pass filter (RC network) as shown in figure 1, an analog output (D/A-converted signal) is produced. In this sample task, we use the output on the PW8 pin.
- In 10-MHz operation, the internal clock frequency is selectable from among ϕ , $\phi/2$, $\phi/4$, $\phi/8$, and $\phi/16$. In this sample task, $\phi/16$ is selected. For specific values, please see table 1.
- In this sample task, we measure the analog outputs corresponding to duty cycles in the range from 0/16 to 15/16. The relationship between duty cycle and analog voltage is given in table 2.

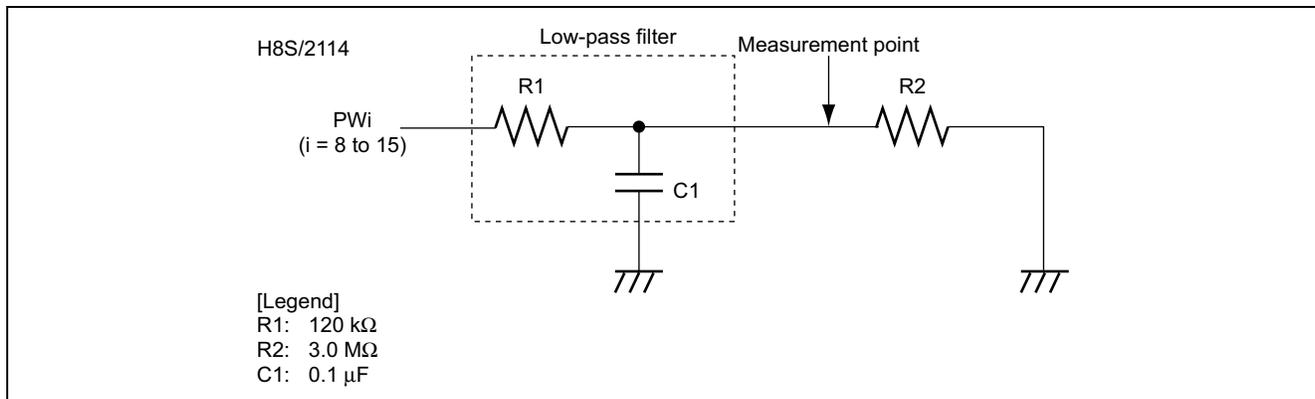


Figure 1 Example Circuit for Use as a D/A Converter

Table 1 Resolution, PWM Conversion Period, and Carrier Frequency when $\phi = 10$ MHz

Internal Clock	Resolution	PWM Conversion Period	Carrier Frequency
ϕ	100 ns	25.6 μs	625 kHz
$\phi/2$	200 ns	51.2 μs	312.5 kHz
$\phi/4$	400 ns	102.4 μs	156.3 kHz
$\phi/8$	800 ns	204.8 μs	78.1 kHz
$\phi/16$	1600 ns	409.6 μs	39.1 kHz

Table 2 Relationship between Duty Cycle and Analog Output

No.	Duty Cycle	PWDR Setting	Analog Output [V]		
			Theoretical Value* ¹	(1)* ²	(2)* ²
1	0/16 (no additional pulse)	H'00	0.00	0.01	0.01
2	1/16 (no additional pulse)	H'10	0.21	0.20	0.23
3	2/16 (no additional pulse)	H'20	0.41	0.38	0.42
4	3/16 (no additional pulse)	H'30	0.62	0.57	0.63
5	4/16 (no additional pulse)	H'40	0.83	0.78	0.82
6	5/16 (no additional pulse)	H'50	1.03	0.96	1.04
7	6/16 (no additional pulse)	H'60	1.24	1.17	1.23
8	7/16 (no additional pulse)	H'70	1.44	1.35	1.45
9	8/16 (no additional pulse)	H'80	1.65	1.54	1.63
10	9/16 (no additional pulse)	H'90	1.86	1.73	1.84
11	10/16 (no additional pulse)	H'A0	2.06	1.95	2.04
12	11/16 (no additional pulse)	H'B0	2.27	2.12	2.24
13	12/16 (no additional pulse)	H'C0	2.48	2.32	2.45
14	13/16 (no additional pulse)	H'D0	2.68	2.53	2.67
15	14/16 (no additional pulse)	H'E0	2.89	2.73	2.85
16	15/16 (no additional pulse)	H'F0	3.09	2.93	3.06
17	15/16 (additional pulse: 15/16)* ³	H'FF	—	3.10	3.24
18	PWM output fixed at high level (100% duty cycle)	—	3.30	3.10	3.24

Notes 1. The theoretical values of the analog output are calculated from the following formula:

$$\text{Analog output (theoretical value)} = V_{cc} \times \text{duty cycle, where } V_{cc} = 3.3 \text{ V}$$

2. Values of R1, R2, and C1 in figure 1:

(1) R1 = 120 kΩ, R2 = 3.0 MΩ, C1 = 0.1 μF

(2) R1 = 120 kΩ, R2 = no resistor connected (open), C1 = 0.1 μF

The R2 value in the figure is chosen on the assumption that the input impedance of an actually connected device is 3 MΩ.

The values shown here are reference values that suited our environment. Before actually using the circuit, evaluate the values on your system.

3. By superposing an additional pulse, the analog voltage can be set in finer steps. When the PWM function is used, the configuration of a 15/16 duty cycle with a 15/16 additional pulse leads to the maximum analog output that can be obtained through PWDR setting.

2. Conditions for Application

Table 3 Conditions for Application

Item	Description
Operating frequency	System clock (ϕ): 10 MHz
Operating mode	Mode 6 (MD2 = 1, MD1 = 1, MD0 = 0) Mode 2 (MD2 = 0, MD1 = 1, MD0 = 0)
Development tool	HEW: version 4.00.00.027
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler: version 6.0.3.0 (from Renesas Technology Corp.)
Compiler options	-cpu = 2000A:24, -code = asmcode, -optimize = 1

3. Functional Description

This sample task applies the 8-bit PWM function to output pulses with a controlled duty cycle (0/16 to 15/16) from a PWM output pin. Figure 2 is a block diagram of the 8-bit PWM module, and is followed by a description of the module.

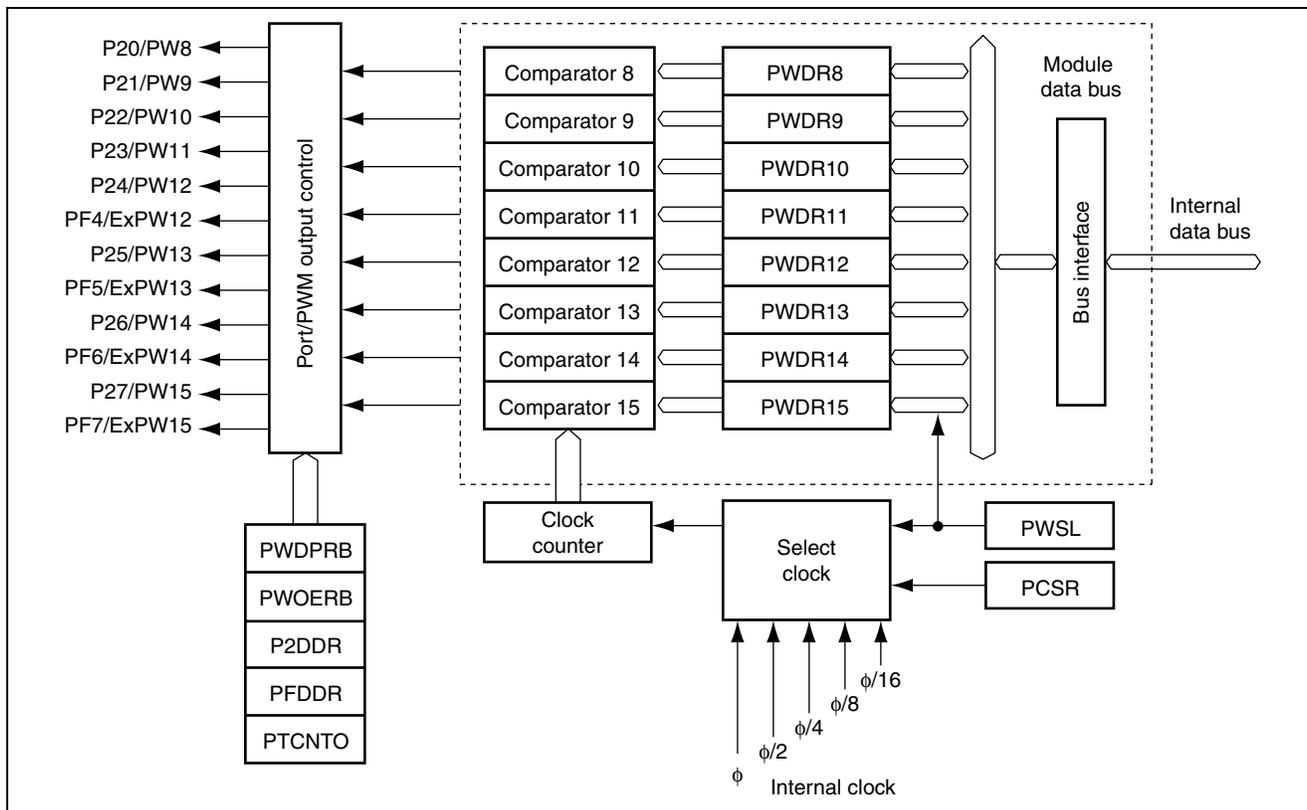


Figure 2 Block Diagram of 8-bit PWM Module

- The 8-bit PWM module can operate with a maximum carrier frequency of 625 kHz ($f = 10 \text{ MHz}$) through pulse division.
- Duty cycles ranging 0 to 100% can be set with 1/256 resolution (100% duty cycle is realizable as a port output).
- The input clock for the PWM timer is selectable from among ϕ , $\phi/2$, $\phi/4$, $\phi/8$, and $\phi/16$. The system clock (ϕ) is the reference clock used to drive the CPU and peripheral functions. The resolution, conversion period, and carrier frequency for PWM are calculated from the selected internal clock frequency by using the following formulae.

Resolution (minimum pulse width) = $1/\text{Internal clock frequency}$

PWM conversion period = resolution \times 256

Carrier frequency = $16/\text{PWM conversion period}$

- PWM data registers 15 to 8 (PWDR15 to PWDR8) are 8-bit readable/writable registers that set the duty cycles of the basic pulses for output and the number of additional pulses to be superposed on them. The higher-order four bits set the duty cycle of the basic pulse in the range from 1/16 to 1/15 with 1/16 resolution. The lower-order four bits set the number of additional pulses to be superposed within the conversion period, which consists of 16 basic pulses. Consequently, the setting range of PWDR is from 0/256 to 255/256. To produce a PWM output corresponding to 256/256 (100% duty cycle), use the port output function.
- PWM data polarity register (PWDPRB) is an 8-bit readable/writable register that controls the polarity (direct or inverted output) of the PWM output.
- PWM output enable register B (PWOERB) is an 8-bit readable/writable register that selects between PWM output and port output. To set up a pin for output, also set the corresponding bit in the port data direction register to specify the pin as an output pin.
- Port 2 data direction register (P2DDR) is an 8-bit write-only register. Each bit in this register sets the signal direction (input/output) for the corresponding pin of port 2. The port 2 pins are shared with the PW8 to PW15 pins. The bits corresponding to the pins to be used for PWM output should be set to configure them as output pins.
- Port 2 data register (P2DR) is an 8-bit readable/writable register. It is used to produce a PWM output fixed at a high level (when OS = 0) or low level (when OS = 1).

Note: The register descriptions above apply to the H8S/2114 group. When using a device from another group of the H8S/2100 series, consult the corresponding datasheet.

4. Description of Operation

This section explains the operation of this sample task. Figure 3 illustrates the D/A converter operation using the 8-bit PWM function. The pulses output from the PW_i (i = 8 to 15) pin are smoothed by the RC network (low-pass filter) to produce an analog output (D/A-converted output). For reference, figure 4 shows an example of a D/A-converted waveform generated by using the 8-bit PWM function.

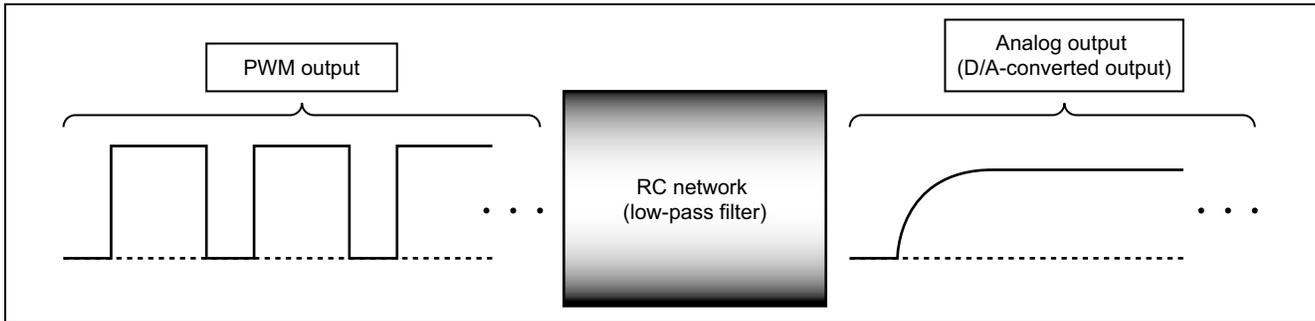


Figure 3 Operation of a D/A Converter Driven by the 8-bit PWM Function

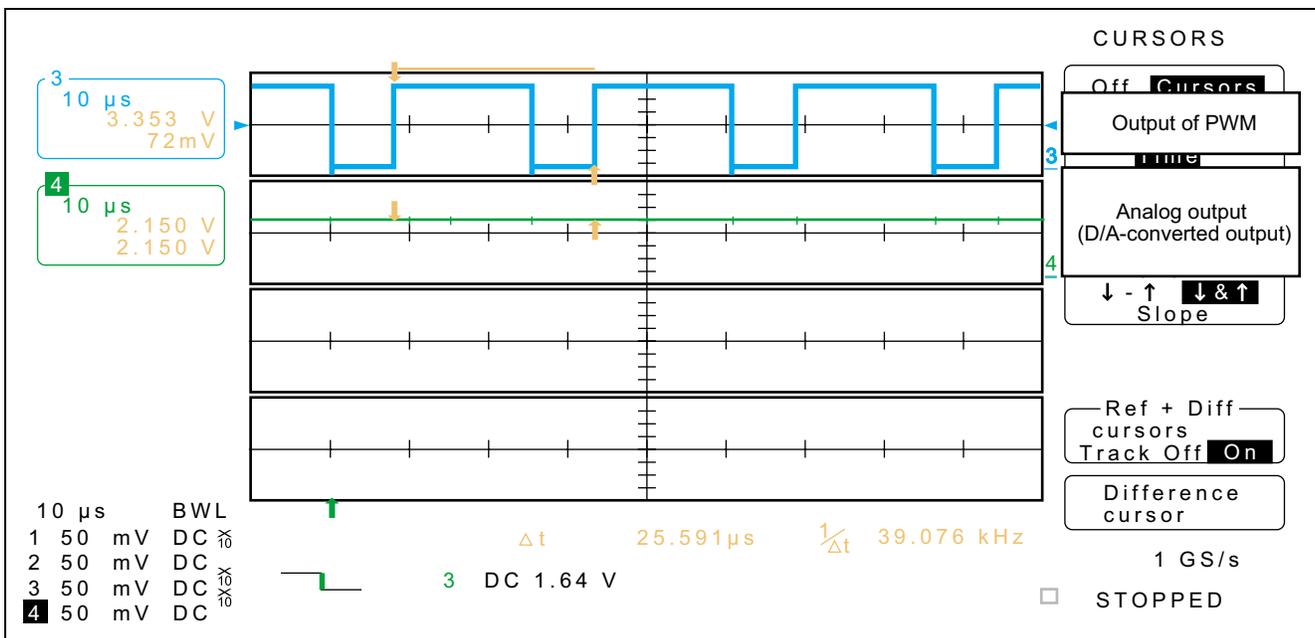


Figure 4 D/A-Converted Waveform Generated by Using the 8-bit PWM Function (for Reference)

5. Description of Software

5.1 Module

Table 4 describes the single module of this sample task.

Table 4 Description of Module

Module	Label	Function
Main Routine	main	Implements 8-bit PWM output on the PW8 pin

5.2 Arguments

No argument is used in this sample task.

5.3 Internal Registers

Table 5 describes the internal registers used in this sample task.

Table 5 Description of Internal Registers

Register	Function	Address	Setting
PWSL	PWCKE PWM Register Select (PWM clock enable) Selects the internal clock for input to TCNT of the 8-bit PWM module. See table 6 for details. 0: Clock input is disabled. 1: Clock selected by the PWCKS bit and PCSR register is input.	H'FFFD6 Bit 7	1
	PWCKS PWM Register Select (PWM clock select) Selects the internal clock for input to TCNT of the 8-bit PWM module. See table 6 for details. 0: System clock (ϕ) 1: Clock selected by PCSR	H'FFFD6 Bit 6	1
RS3	PWM Register Select (Register select)	H'FFFD6	1
RS2	These bits select a PWM data register. In this sample task,	Bits 3 to 0	0
RS1	PWDR8 is selected.		0
RS0	0xxx: No effect on operation 1000: PWDR8 is selected. 1001: PWDR9 is selected. 1010: PWDR10 is selected. 1011: PWDR11 is selected. 1100: PWDR12 is selected. 1101: PWDR13 is selected. 1110: PWDR14 is selected. 1111: PWDR15 is selected.		0

Register	Function	Address	Setting								
PCSR	PWCKB	Peripheral Clock Select Register (PWM clock select B, A)	H'FFFF82 1								
	PWCKA	These bits select the internal clock for input to TCNT of the 8-bit PWM module. See table 6 for details. In this sample task, $\phi/16$ is selected. 00: $\phi/2$ is selected. 01: $\phi/4$ is selected. 10: $\phi/8$ is selected. 11: $\phi/16$ is selected.	Bits 2, 1 1								
PWDR8	PWM Data Register 8 Sets the duty cycle of the basic pulse to be output and the number of additional pulses to be superposed. <ul style="list-style-type: none"> Higher-order 4 bits Duty cycle of the basic pulse (Setting range is from 0/16 to 15/16 with 1/16 resolution) Lower-order 4 bits Number of additional pulses (Setting range is from 0 to 15 pulses) 	H'FFFFD7	H'80								
PWDRB	OS8 PWM Data Polarity Register B (Output select 8) Selects the output phase of the PWM. The OS8 bit corresponds to the PWM8 output. 0: Direct PWM output (Value of PWDR sets the high-level width of the output) 1: Inverted PWM output (Value of PWDR sets the low-level width of the output)	H'FFFFD4 Bit 0	0								
PWOERB	OE8 PWM Output Enable Register B (Output enable 8) With the P20DDR bit in P2DDR, specifies the P20/PW8 pin function. The OE8 bit corresponds to the PWM8 output.	H'FFFFD2 Bit 0	1								
<table border="1"> <thead> <tr> <th>[P20DDR, OE8]</th> <th>Pin function</th> </tr> </thead> <tbody> <tr> <td>0x:</td> <td>Port input</td> </tr> <tr> <td>10:</td> <td>Port output or 256/256 PWM output</td> </tr> <tr> <td>11:</td> <td>PWM output (0/256 to 255/256)</td> </tr> </tbody> </table>				[P20DDR, OE8]	Pin function	0x:	Port input	10:	Port output or 256/256 PWM output	11:	PWM output (0/256 to 255/256)
[P20DDR, OE8]	Pin function										
0x:	Port input										
10:	Port output or 256/256 PWM output										
11:	PWM output (0/256 to 255/256)										
P2DDR	Port 2 Data Direction Register Here, sets the PW8 pin as an output pin.	H'FFFFAD Bit 0	1								
MSTPCRH	MSTP11 Module Stop Control Register H (MSTP11) Here, used to take the 8-bit PWM timer (PWMX) out of the module stop mode. 0: Module stop mode is cancelled. 1: Module stop mode is set.	H'FFFF86 Bit 3	0								

Table 6 Internal Clock Selection

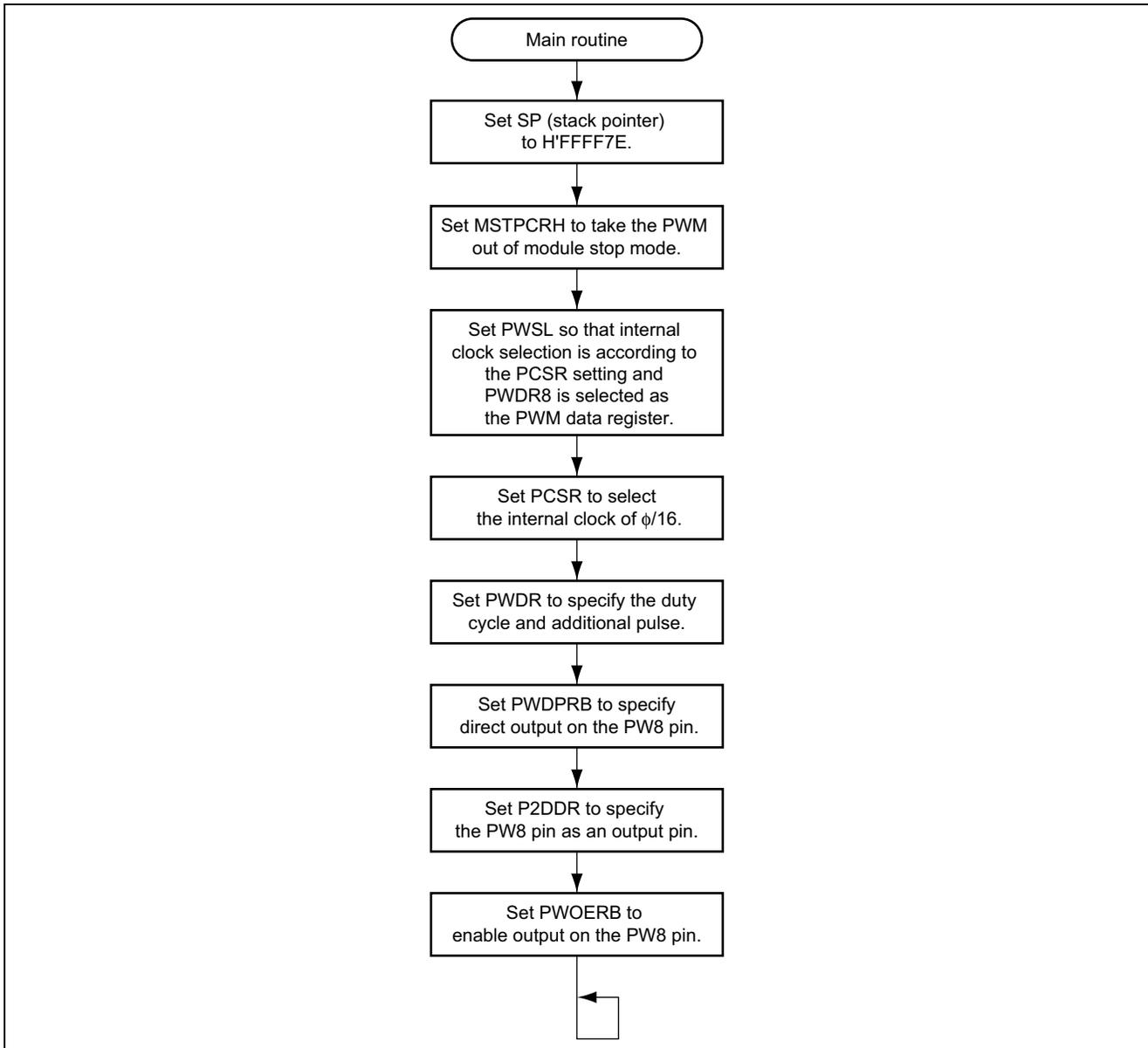
PWCKE	PWSL		PCSR		Description
	PWCKS	PWCKB	PWCKA		
0	—	—	—		Clock input is disabled (initial value)
1	0	—	—		ϕ (system clock) is selected
			0		$\phi/2$ is selected
	1	0	1		$\phi/4$ is selected
			0		$\phi/8$ is selected
		1		$\phi/16$ is selected	

5.4 RAM Usage

RAM is not used in this sample task.

6. Flowchart

6.1 Main routine



7. Program Listing

```

/*****
/*
/* This program is 8bit PWM output program for H8S/2114 evaluation.
/*
/*
/* File name : pwm8.c
/*
/* Frequency : 10MHz
/*
/* CPU TYPE : H8S/2114
/*
*****/

/*****
/* Include
*****/

#include <stdio.h> /* Input/Output library file
#include <machine.h> /* Built-in function file
#include "2114.h" /* H8S/2114 I/O register definition file

/*****
/* Prototype
*****/

void main(void); /* Main routine

/*****
/* RAM allocation
*****/

/*****
/* main : Main routine
*****/

void main(void)

#pragma section

#pragma asm

    mov.l    #H'FFFF7E,sp ; Initialize stack pointer

#pragma endasm

```

```

{

/* Module stop mode reset */

    MSTPCR.BYTE.H = 0x37;                                /* Reset PWM module stop mode          */

/* PWM internal clock & PWM data register set*/

    PWM.PWSL.BYTE = 0xE8;                                /* Set PWM data register                */
//      b7 b6 b5 b4 b3 b2 b1 b0                          //
//      x  x  x  x-----0xxx : Operation not affected    //
//      1000 : Select PWDR8 (This is set)                  //
//      1001 : Select PWDR9                                //
//      1010 : Select PWDR10                               //
//      1011 : Select PWDR11                               //
//      1100 : Select PWDR12                               //
//      1101 : Select PWDR13                               //
//      1110 : Select PWDR14                               //
//      1111 : Select PWDR15                               //

    PWM.PCSR.BYTE = 0x06;                                /* PCSR set                             */
//      b7 b6 b5 b4 b3 b2 b1 b0                          //
//      x  x-----00 : Select phi/2                      //
//      01 : Select phi/4                                  //
//      10 : Select phi/8                                  //
//      11 : Select phi/16 (This is set)                  //

    PWM.PWDR = 0x80;                                    /* Duty cycle & Add pulse setting      */

    PWM.PWDPRB.BIT.OS8 = 0;                             /* PW8 output : direct output          */

/* PWM output port set */

    P2.DDR = 0xFF;                                       /* Set PW8-15 output                    */

    PWM.PWOERB.BIT.OE8 = 1;                             /* Enable PW8(P20) output              */

    while(1);                                           /* Loop                                  */

}

```

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Jul.22.05	—	First edition issued

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