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Renesas Electronics Corporation

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H8S Family

Simultaneous Startup of DTC, DMAC, and CPU

Introduction

Starts up DTC, DMAC, and CPU each time a compare match occurs. DTC transfers data from the ROM to the I/O port and outputs pulses. The DMAC transfers data stored in RAM1 to RAM2. The CPU monitors the state of the port and stops DTC and DMAC when the port output goes high.

Target Device

H8S/2339

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1. Specifications

1. As shown in figure 1, this sample task starts up DTC, DMAC, and CPU each time a timer compare match occurs. DTC transfers data to I/O Port from the data table (ROM) to output the pulses. The DMAC transfers 512-byte data stored in RAM1 to RAM2. The CPU monitors the state of the port. When the port goes high, the CPU stops DTC and DMAC transfer. An interrupt to the CPU continues to be enabled.
2. Data to be transferred by the DMAC is stored in addresses H'FF8C00 to H'FF8DFF.
3. The H8S/2339 runs at 19.6608-MHz internal operating frequency.

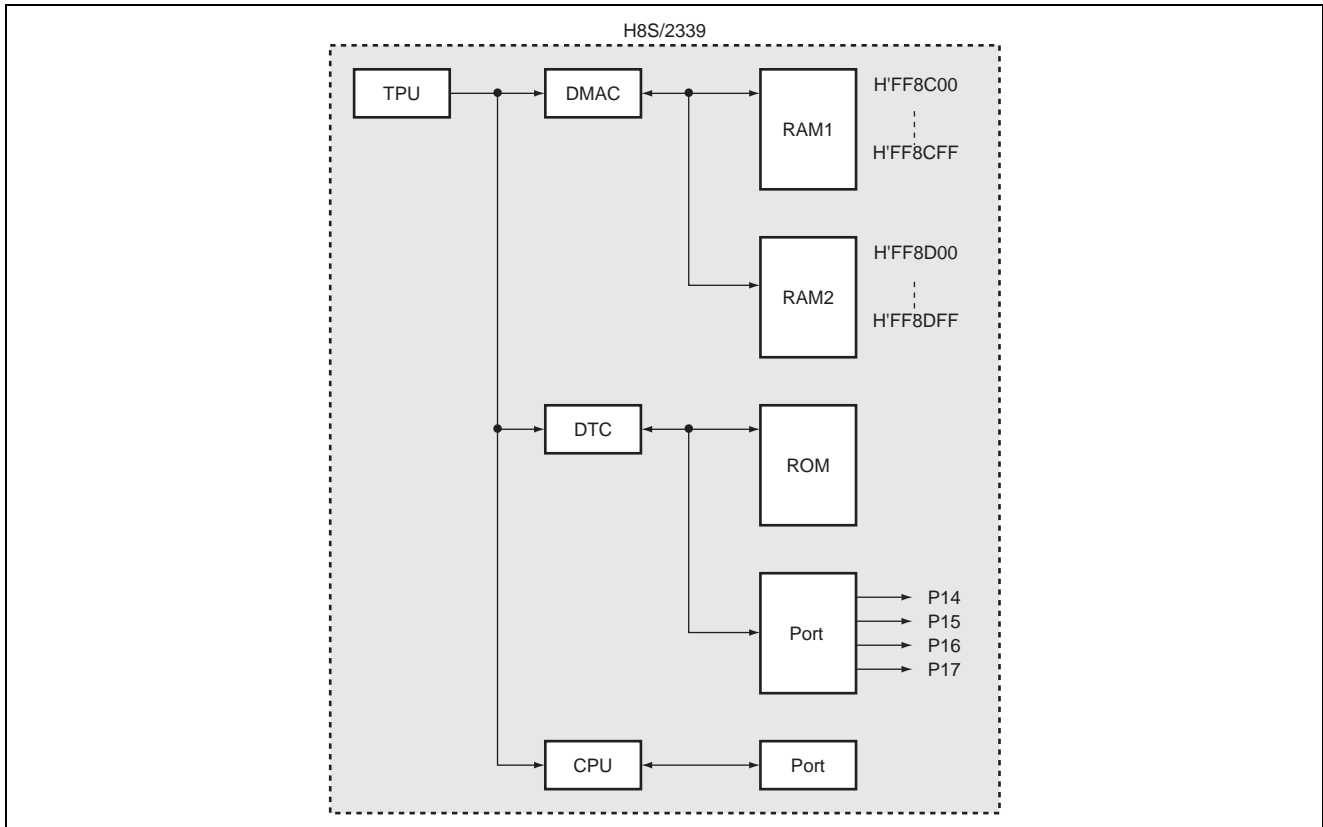


Figure 1 Block Diagram of Simultaneous Startup of DTC, DMAC, and CPU

2. Description of Functions

1. This sample task starts up the DMAC, DTC, and CPU each time a TPU compare match occurs.

A. The block diagram of H8S/2339 internal functions that this sample task uses is shown in figure 2.

This sample task uses the following functions to start up DTC, DMAC, and CPU simultaneously to transfer data and monitor the port.

[TPU]

Generates a compare match to generate a transfer request to DTC and DMAC and a CPU interrupt request.

[DMAC]

Starts up by a TPU compare match to transfer 256-byte data to RAM2 from RAM1.

[DTC], [PORT]

Start up by a TPU compare match to transfer 4-byte data to I/O port from the data table.

[CPU]

Executes interrupt processing by a TPU compare match. During interrupt processing, monitors the port state and controls DMAC and DTC transfer.

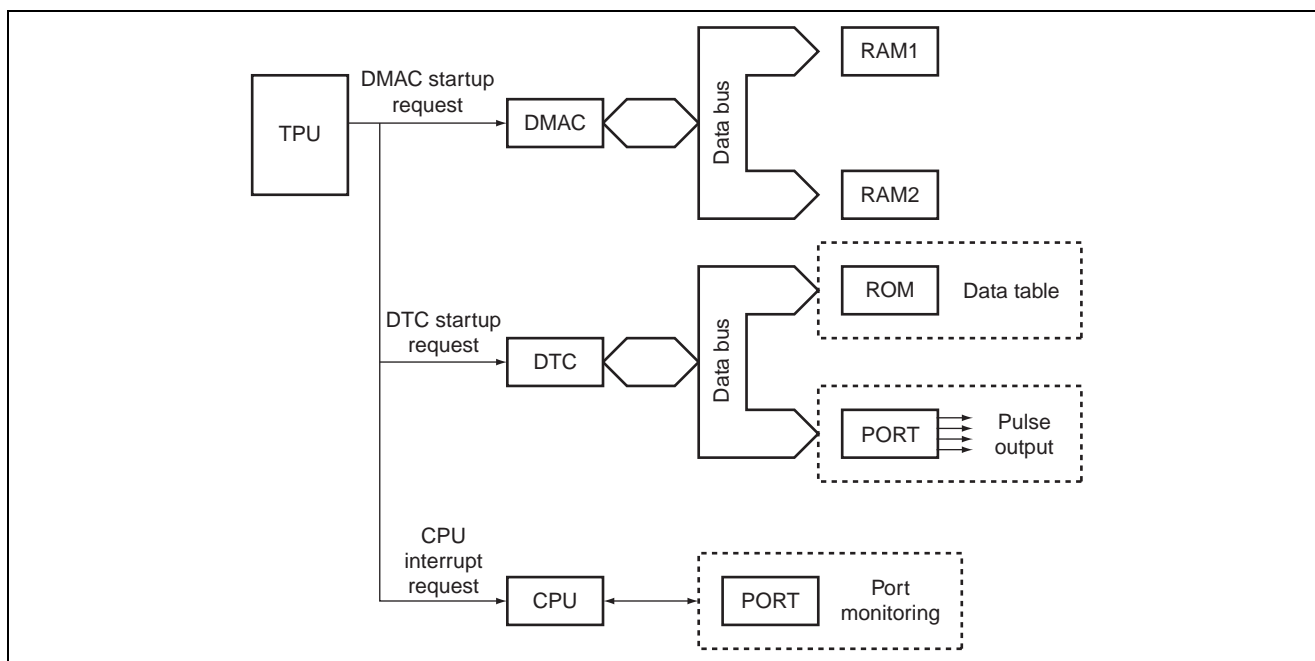


Figure 2 Block Diagram of Simultaneous Startup of DTC, DMAC, and CPU

3. Principles of Operation

The principles of operations used are shown in figure 3. This sample task performs hardware and software processing at the timing shown in figure 3 to request simultaneous startup of DTC, DMAC, and CPU interrupt.

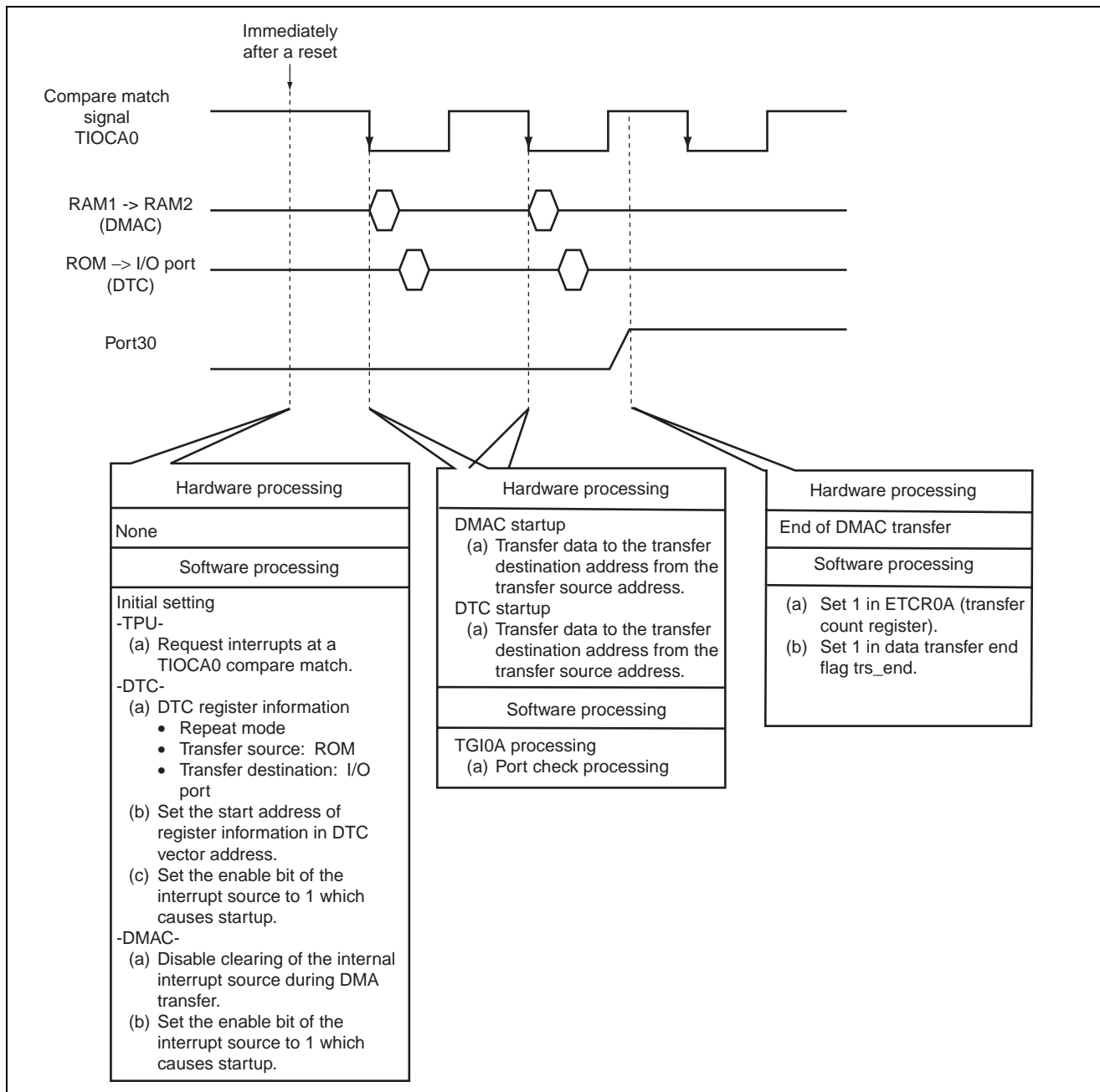


Figure 3 Principles of Operations Used of Simultaneous Startup of DTC, DMAC, and CPU

4. Description of Software

1. Description of Modules

Module Name	Label Name	Function
Main routine	simbsrnm	Performs initial setting of the TPU, DTC, DMAC, I/O port and interrupt processing.
Port check	portchk	Checks the port and performs transfer disable processing.
Data transfer end	trsend	Sets the data transfer end flag.

2. Description of Arguments

Elements	Function	Data Length	Used in	I/O
status	Indicates the state of port 30. 0: Transfer enabled 1: Data transfer disabled	unsigned char	Port check	Output
trs_end	Flag indicating the end of 256-byte transfer 0: Transfer enabled 1: Data transfer disabled	unsigned char	Data transfer end	Output

3. Description of Internal Registers Used

Implemented Function	Register Name	Function
DMAC	DMABCR	Sets the DMAC0A as follows: <ul style="list-style-type: none"> • Full-address mode as the transfer mode • Disabling clear of the internal interrupt source during DMA transfer • Enabling data transfer and a transfer end interrupt
	DMACR0A	Sets the DMAC0A as follows: <ul style="list-style-type: none"> • Byte size as the data size • MAR increment • Block transfer mode for data transfer, and block area is set on the destination side • Setting the startup source to TPU0A
	MAR0A	Sets the start address (trs) of RAM1.
	MAR0B	Sets the start address (rev) of RAM2.
	ETCR0A, OB	Sets the transfer count.
	TPU	TCR0
TIOR0		Enables compare match output.
TIER0		Enables a compare match interrupt.
TSR0		Sets the TGRA capture interrupt request flag.
TGR0A		Set the compare-match counter value in TGR0A.
TSTR		Startup the TPU0 counter.
DTC		DT CER
MSTPCR		Controls module stop mode of DTC, TPU and DMAC.

4. RAM Usage

Table below describes RAM usage in this sample task.

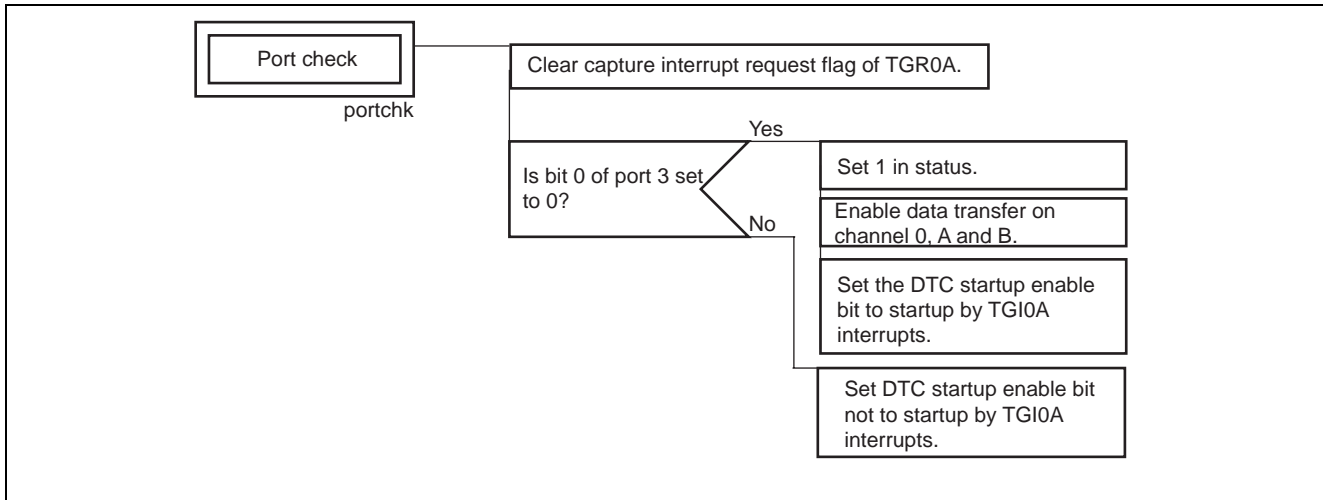
Elements	Function	Data Length	Used in
MAR0	Sets the DTC0 in the repeat mode.	unsigned char	Main routine
MRB0	Enables an interrupt to the CPU.	unsigned char	
SAR0	Sets the transfer source address (PATTBL1).	unsigned long	
DAR0	Sets the transfer destination address (P07 to P04).	unsigned long	
CRA0	Sets the transfer count.	unsigned short	
trs	Stores transmit data.	256 bytes	
rev	Stores received data.	256 bytes	
PATTBL1	Stores pulse output data.	4 bytes	

5. PAD

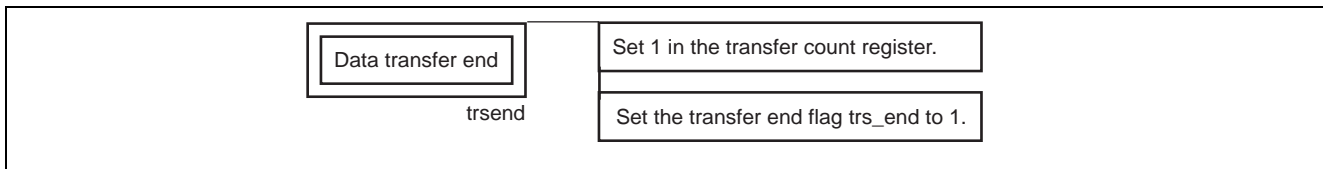
1. Main Routine

<div style="border: 1px solid black; padding: 2px; display: inline-block;">Simultaneous startup</div> simbsrmm	Initialize status flag and trs_end flag.
	Cancel the TPU, DMA, and DTC module stop mode.
	Set port 2 to output.
	Using "next data enable L register", set pulse pins PO7 to PO0 to output.
	Initialize "output data register".
	Set PPG pulse output groups 3 to 0 to operate at TPU0 compare-match.
	Set PPG output mode register so that PPG pulse output groups 3 to 0 outputs are not inverted.
	Set DMAC to full address mode and to disable clearing of internal interrupt sources
	Set the transfer source address (MAR0A) to RAM1 start address.
	Set the transfer destination address (MAR0B) to RAM2 start address.
	Set the number of transfer to 256 times.
	Set transfer in block transfer mode, the block area on the transfer destination side, byte size, and to increment MARA after data transfer.
	After data transfer, increment MARB, and startup following interrupt by TPU0 compare match.
	Set the DTME bit to enable data transfer of channel 0.
	Set the DTE bit of DMAC to enable data transfer of channel 0.
	Set the DTIEA bit to enable transfer end interrupts on channel 0.
	Set the DTIEB bit to enable transfer-suspend interrupts on channel 0.
	Set the start address of the transfer source PATTBL1 in SAR0.
	Set the start address of the transfer destination PPG.NDRL1 in DAR0.
	Increment SAR after transfer, DAR is fixed, and transfer in repeat mode on the transfer source side.
	After DTC data transfer is completed, enable interrupts to the CPU.
	Set the number of data transfers by the DTC to 04.
	Set the DTC startup enable bit to startup by the TG10A interrupt.
	Output 1 by compare match of the output compare register.
	Set the count value to be used for compare matching in TGRA.
	Clear TCNT by TGRA compare match.
	Enable TGIA interrupts.
	Clear the I flag and enable interrupts.
	Enable TPU0 count operation.
	while (1)

2. Port Check



3. Data Transfer End



6. Link Address Specifications

Section Name	Address
dDtc_vect_TGI0A	H'00000400
PResetPRG, PIntPRG, P, C, C\$DSEC, C\$BSEC, D	H'00000800
B, R	H'00FFDC00
S	H'00FFF9F0

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Feb.17.05	—	First edition issued

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