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April 1st, 2010
Renesas Electronics Corporation

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H8S Family

DTMF Signal Output (DTMF Generation Circuit)

Introduction

The internal DTMF generation circuit is used to output the DTMF signals. A 4 x 4 keypad is externally connected.

Target Device

H8S/2268

Contents

1. Specifications

(1) The DTMF generation circuit is used to output DTMF signals.
(2) A 4 × 4 keypad is connected to the H8S/2268 and DTMF signals corresponding to the depressed keys are output.
(3) The DTMF signals are output from the TONED pin.
(4) The configuration for this sample task is shown in figure 1.

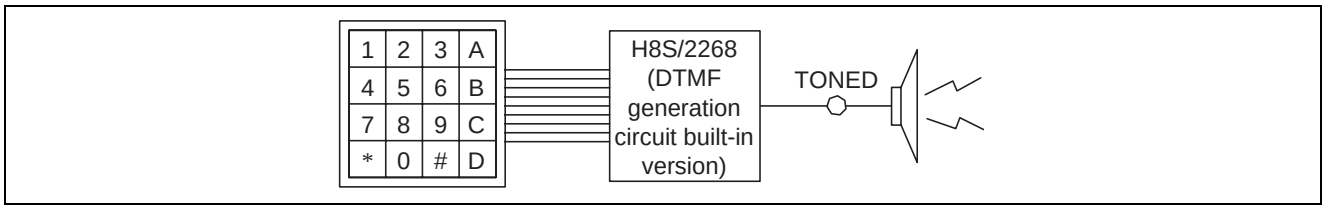


Figure 1 Configuration for Sample Task

2. Functions Used

(1) Block Diagram of Functions Used
A block diagram of functions used for this sample task is shown in figure 2.

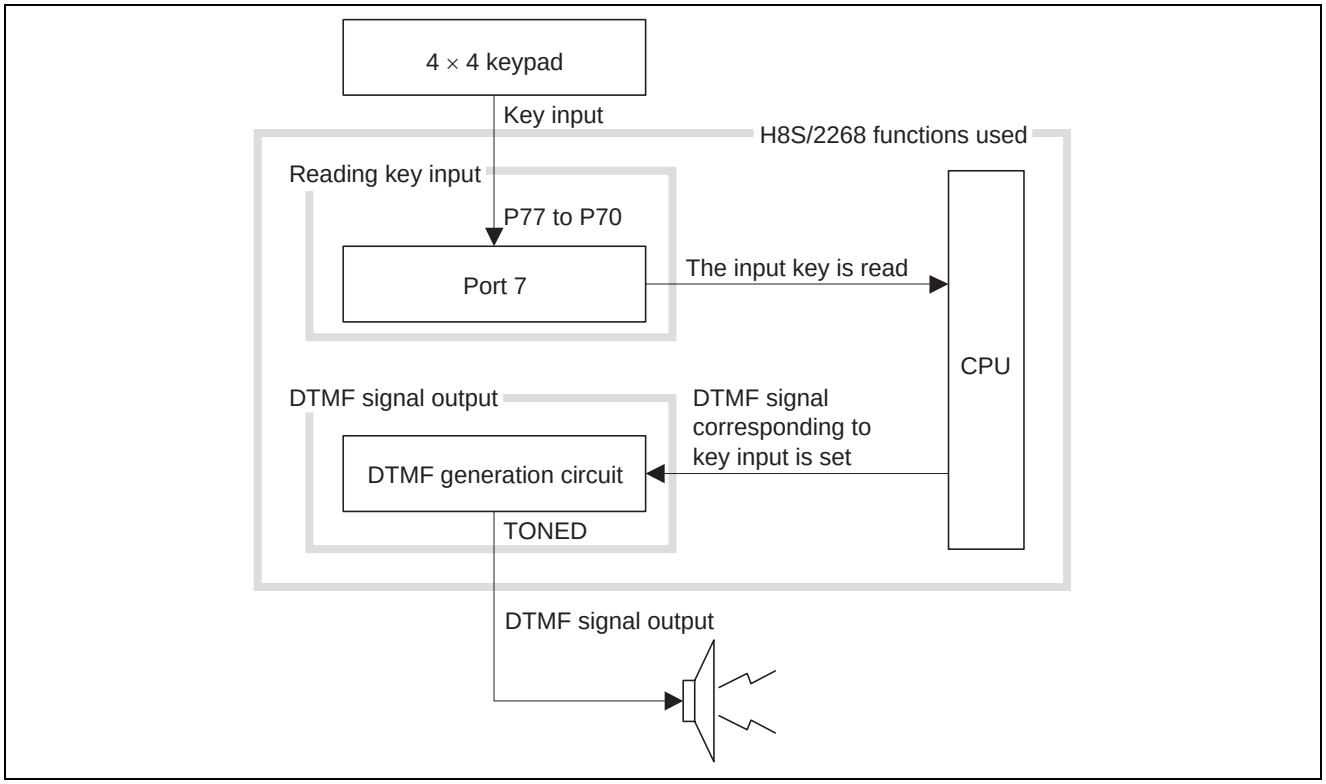


Figure 2 Block Diagram of H8S/2268 Functions Used

(2) Functions of DTMF Generation Circuit

A block diagram of the DTMF generation circuit is shown in figure 3.

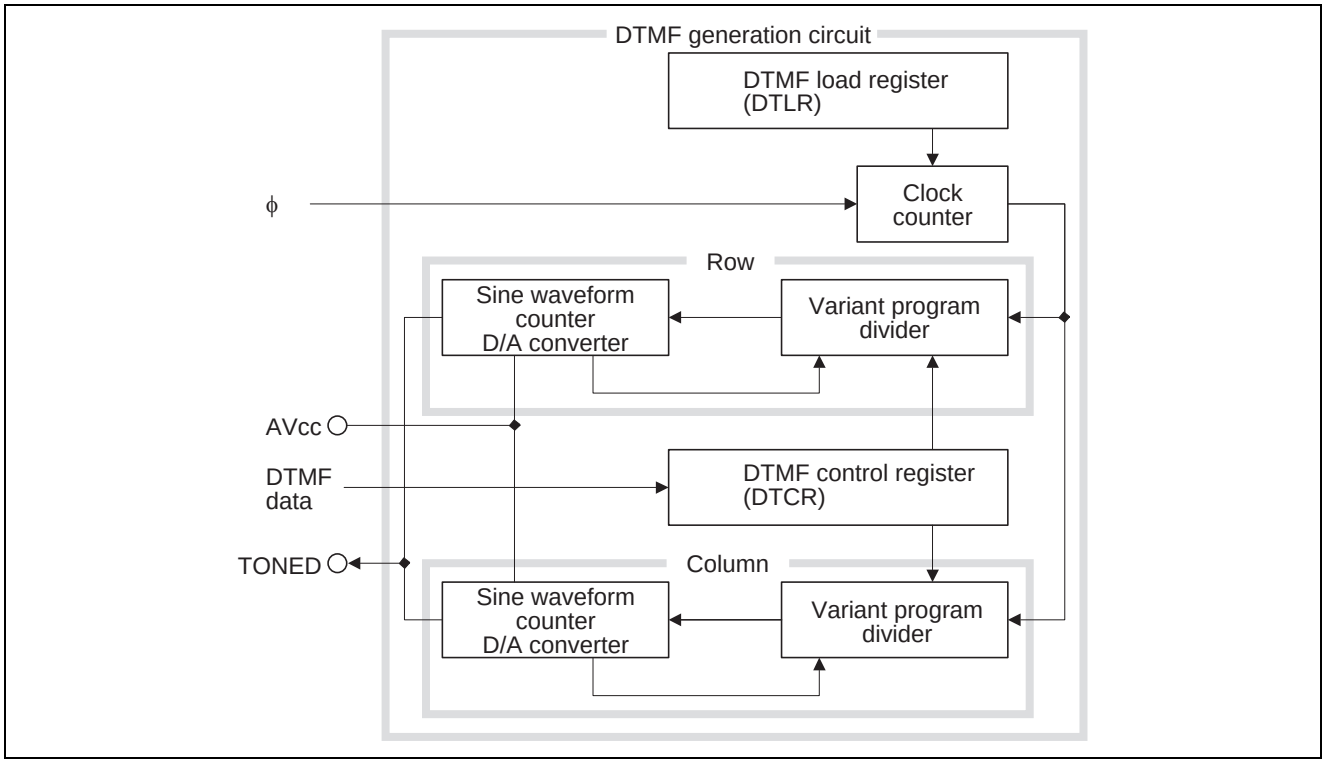


Figure 3 Block Diagram of DTMF Generation Circuit

In this sample task the DTMF generation circuit is used to output DTMF signals. A description of the block diagram of the DTMF generation circuit is given below.

- System clock (ϕ)
  This 10-MHz clock signal is the reference clock used for operation of the CPU and peripheral functions.
- DTMF control register (DTCR)
  Used to control the DTMF generation circuit and DTMF signal output. A DTMF signal is output from the TONED pin when output values are written to DTCR, enabling output.
- DTMF load register (DTLR)
  Bits 5 to 0 of DTLR are used. DTLR specifies the system clock division ratio to produce a 400-kHz clock signal to be supplied to the DTMF generation circuit. In this sample task bits 5 to 0 are set to a value of 011001 (binary) to specify a clock division ratio of 25, since the main clock (ϕ) frequency is 10 MHz.
- DTMF signal output pin (TONED)
  TONED is the output pin for the DTMF signal. A DTMF signal specified in DTCR is output.

(3) Functions of Port 7

A block diagram of the key input circuit using port 7 is shown in figure 4.

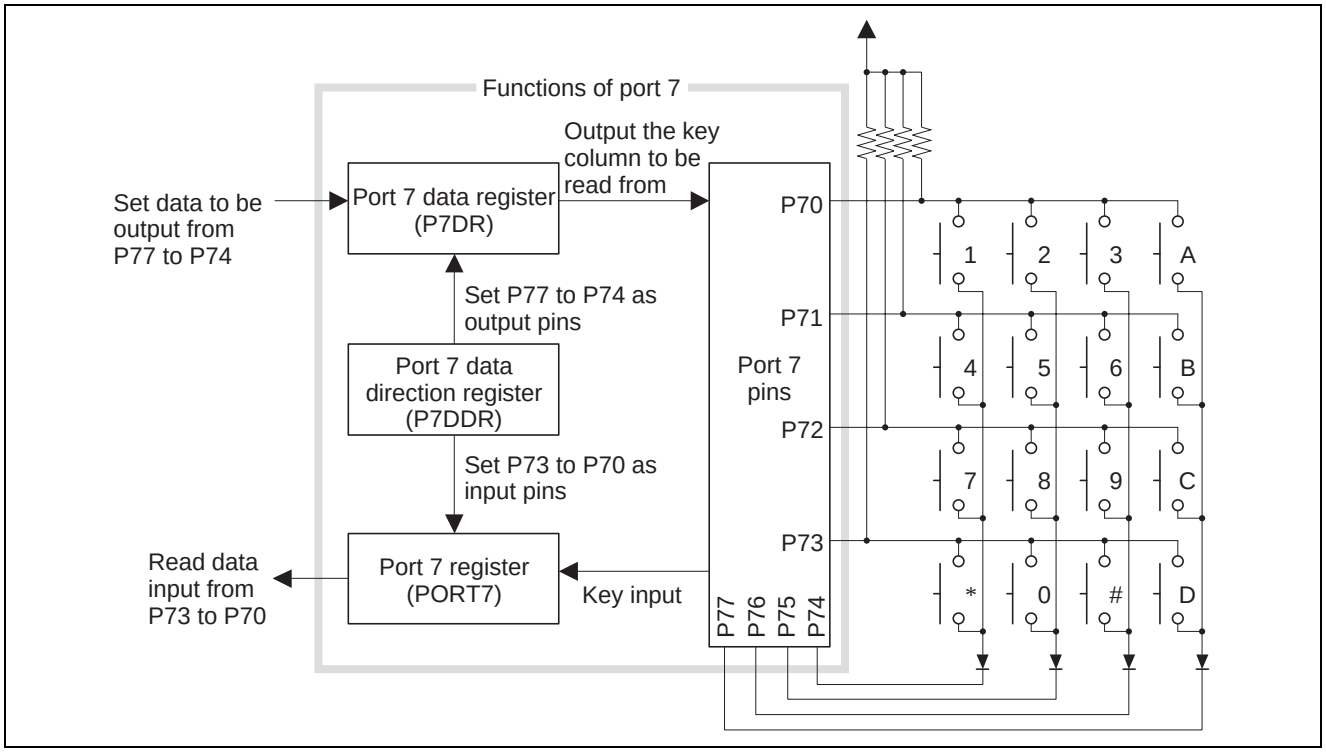


Figure 4 Block Diagram of Key Input Circuit Using Port 7

In this sample task port 7 is used for key input. A description of the block diagram of the key input circuit is given below.

- Port 7 data direction register (P7DDR)
  Specifies input or output settings for port 7 pins. Setting P7DDR to a value of H'F0 sets P77 to P74 as outputs and P73 to P70 as inputs.
- Port 7 data register (P7DR)
  Stores data for output port pins P77 to P74. P73 to P70 reflect the state of the key column set to a low level among P77 to P74.
- Port 7 register (PORT7)
  The lower 4 bits of PORT7 are designated as PORT7L and reflect the values of input port pins P73 to P70. The value stored in PORT7L shows the state of the key column selected by P7DR.

(4) Assignment of Functions

Table 1 shows the assignment of functions in this sample task. Using functions assigned as shown in table 1, DTMF signals are output using the DTMF generation circuit.

Table 1 Assignment of Functions

Elements	Description
PSS	13-bit up-counter with system clock (10 MHz) as input
DTCR	Controls DTMF generation circuit and DTMF signal output
DTLR	Generates 400-kHz clock signal input to DTMF generation circuit
P7DDR	Sets P77 to P74 as output pins and P73 to P70 as input pins
P7DR	Selects the read-in key column
P0RT7L	Stores state of key column selected by P7DR
MSTPCTC	Clears module stop mode of DTMF generation circuit

3. Principles of Operation

(1) Output Waveforms of DTMF Generation Circuit

The DTMF generation circuit of the H8S/2268 outputs from the TONED pin either composite row and column group output waveforms or single sine waveforms (DTMF signals) for the row or column group alone. These signals are generated by a high-precision resistor-ladder-type D/A converter. The output frequency is set in DTCR. The equivalent circuit for TONED pin output is illustrated in figure 5, and a single output waveform for the row group or column group alone is shown in figure 6. Each cycle of the output waveform is divided into 32 parts, achieving low-distortion and stable output.

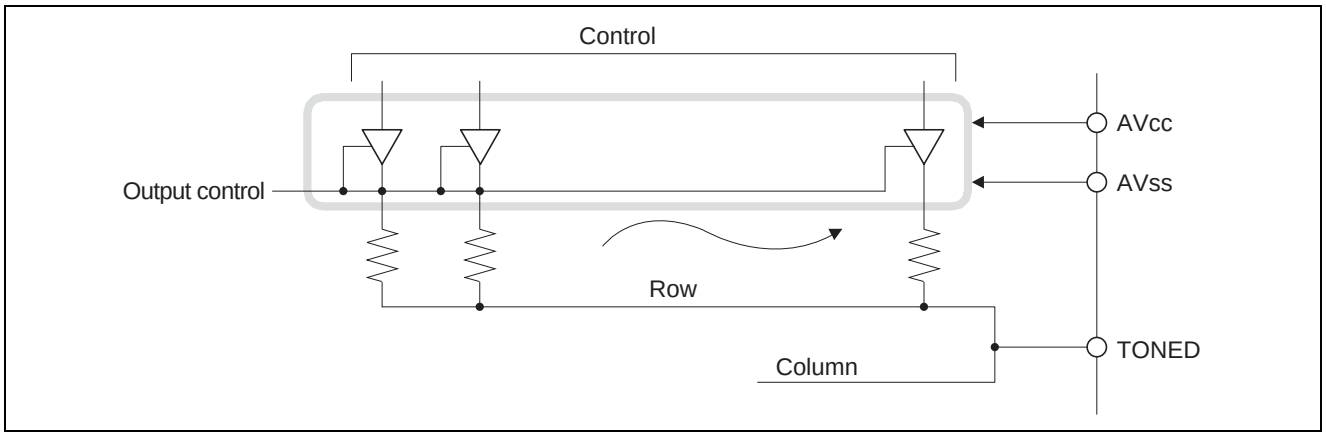


Figure 5 Equivalence Circuit for Output from the TONED Pin

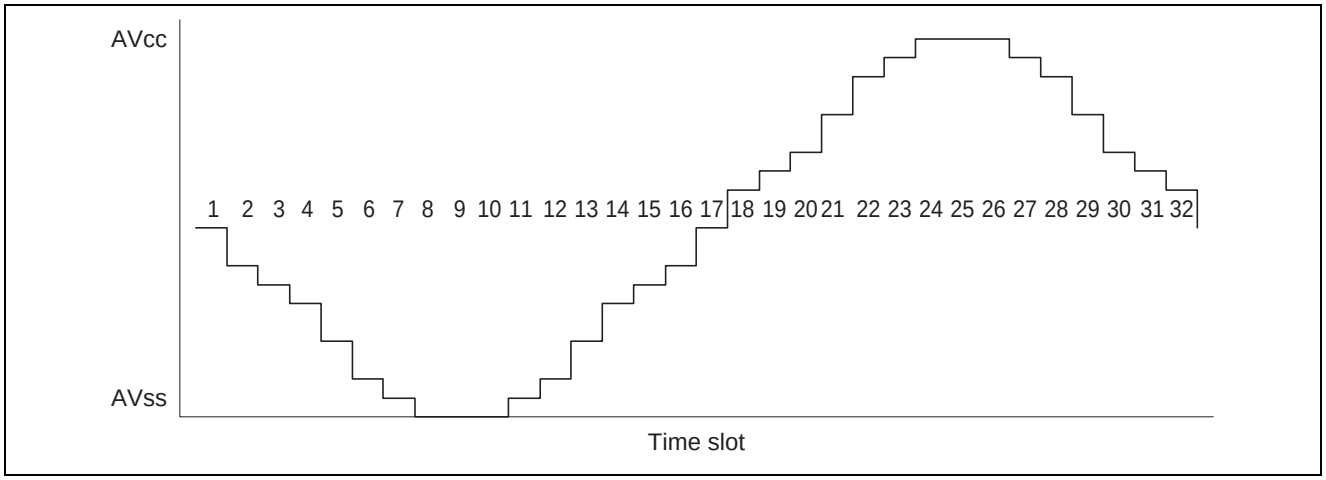


Figure 6 Output Waveform of the TONED Pin (Row Group or Column Group Alone)

(2) Frequency Deviation between Output Signals of DTMF Generation Circuit and Reference Signals

Table 2 Frequency Deviation between Signals Output from DTMF Generation Circuit and Reference Signals

Symbol	Reference Signal [Hz]	DTMF Output Signal [Hz]	Frequency Deviation [%]
R1	697	694.44	–0.37
R2	770	769.23	–0.10
R3	852	851.06	–0.11
R4	941	938.97	–0.22
C1	1209	1212.12	0.26
C2	1336	1333.33	–0.20
C3	1477	1481.48	0.30
C4	1633	1639.34	0.39

4. Description of Software

(1) Modules

Table 3 shows the modules used in this sample task.

Table 3 Modules

Module	Label	Description
Main routine	main	Sets DTMF generation circuit and specifies ports to be used as key input pins

(2) Arguments

No arguments are used in this sample task.

(3) Internal Registers Used

The internal registers used in this sample task are shown below.

Table 4 Internal Registers Used

Register	Bit Name	Description	Address	Set Value
DTCR		DTMF control register	H'FFFC68	—
	DTEN	DTMF generation circuit operation control • DTEN = 0: DTMF generation circuit halted • DTEN = 1: DTMF generation circuit operates	Bit 7	1
	CLOE	Column output control • CLOE = 0: Column DTMF signal output disabled • CLOE = 1: Column DTMF signal output enabled	Bit 5	0
	RWOE	Row output control • RWOE = 0: Row DTMF signal output disabled • RWOE = 1: Row DTMF signal output enabled	Bit 4	0
	CLF1 CLF0	Column DTMF signal output frequency 1 and 0 These bits select the column DTMF signal output frequency. • CLF1, CLF0 = 00: 1,209 Hz (C1) • CLF1, CLF0 = 01: 1,336 Hz (C2) • CLF1, CLF0 = 10: 1,447 Hz (C3) • CLF1, CLF0 = 11: 1,633 Hz (C4)	Bit 3 Bit 2	—
	RWF1 RWF0	Row DTMF signal output frequency 1 and 0 These bits select the row DTMF signal output frequency. • RWF1, RWF0 = 00: 697 Hz (R1) • RWF1, RWF0 = 01: 770 Hz (R2) • RWF1, RWF0 = 10: 852 Hz (R3) • RWF1, RWF0 = 11: 941 Hz (R4)	Bit 1 Bit 0	—
DTLR		• DTMF load register	H'FFFC69	H'D9
	DTL5 to DTL0	Main clock division ratio • DTL5 to DTL0 = 011001 (binary): 400-kHz clock signal generated by division of the 10-MHz main clock frequency by 25	Bit 5 to Bit 0	

Table 4 Internal Registers Used (cont)

Register	Bit Name	Description	Address	Set Value
P7DDR		Port 7 data direction register • P7DDR = H'F0: P77 to P74 set as output ports, P73 to P70 set as input ports	H'FFFF36	H'F0
P7DR		Port 7 data register Stores data for output ports P77 to P74. P73 to P70 reflect the state of the key column set to a low level among P77 to P74 • P7DR = H'E0: P74 key column (1, 4, 7, *) selected • P7DR = H'D0: P75 key column (2, 5, 8, 0) selected • P7DR = H'B0: P76 key column (3, 6, 9, #) selected • P7DR = H'70: P77 key column (A, B, C, D) selected	H'FFFF06	—
P0RT7		• Port 7 register	H'FFFFB6	—
	P0RT7L	• The lower 4 bits of PORT7 are designated as PORT7L and reflect the values of input ports P73 to P70	Bit 3 to Bit 0	
MSTPCRC		• Module stop control register C	H'FFFDEA	H'FB
	MSTPC2	• MSTPC2 = 0: DTMF generation circuit module stop mode is cleared • MSTPC2 = 1: DTMF generation circuit module stop mode is set	Bit 2	0

(4) RAM Usage

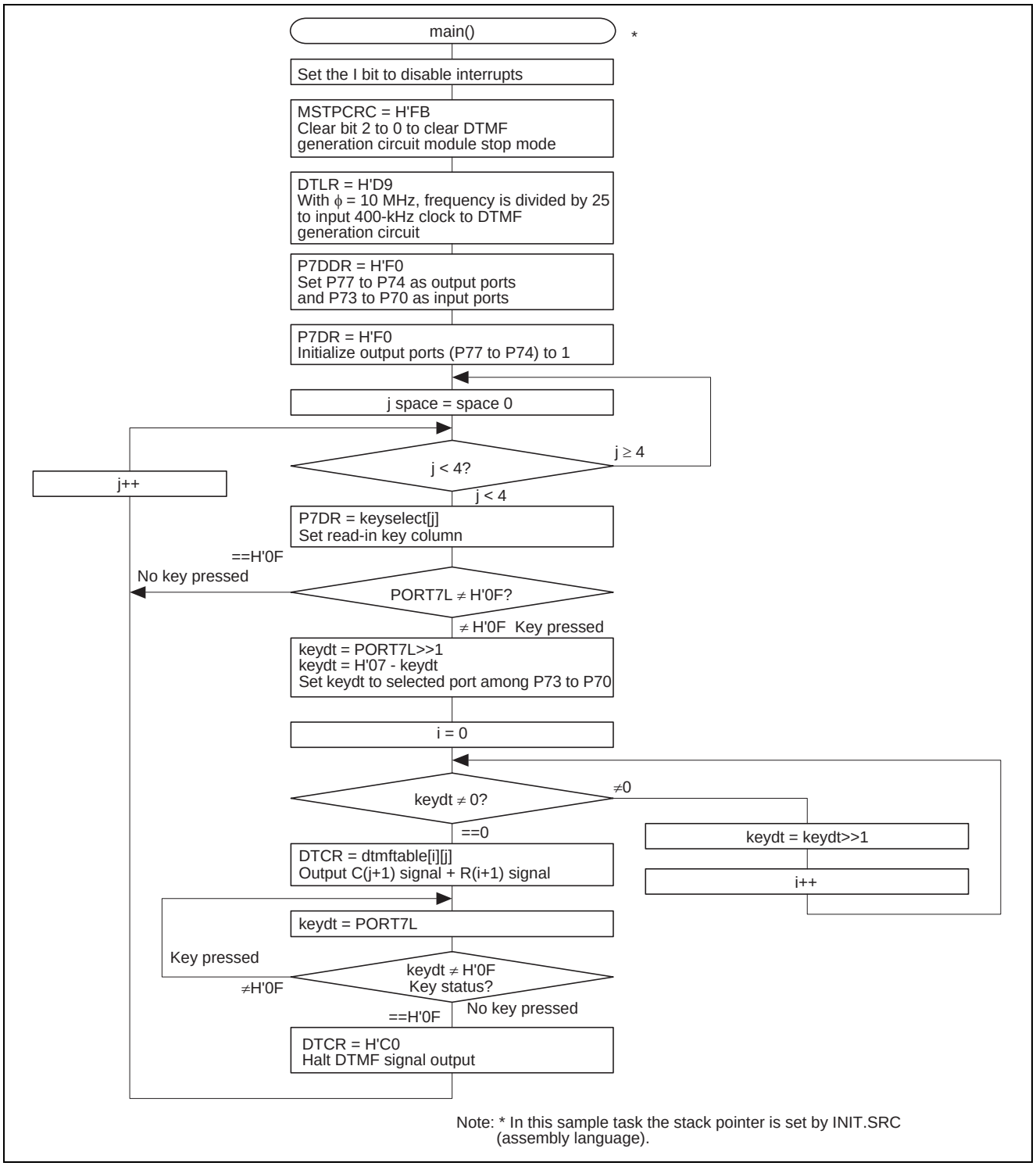
The RAM usage in this sample task is shown in table 5.

Table 5 RAM Usage

Label	Description	Amount of Memory Used	Used in
dtmftable	DTMF output value	16 bytes	main
keyselect	Selects key column for key input	4 bytes	main

5. Flowchart

Main Routin



Note: * In this sample task the stack pointer is set by INIT.SRC (assembly language).

6. Program Listings

INIT. SRC program listing

```
.export _INIT
.import _main
;
.section P,CODE,ALIGN=2
_INIT:
mov.l #h'ffefc0,er7
ldc.b #b'10000000,ccr
ldc.b #0,exr
jmp @_main
;
.end
```

```
/************************************************************************/
/*                                                                      */
/* H8S/2000 Series -H8S/2268-                                           */
/* Application Note                                                     */
/*                                                                      */
/* 'DTMF Waveform Output'                                               */
/*                                                                      */
/* Function                                                             */
/* : DTMF Generation Circuit                                            */
/*                                                                      */
/* External Clock : 10MHz                                               */
/* Internal Clock : 10MHz                                               */
/* Sub Clock : 32.768kHz                                                */
/*                                                                      */
/************************************************************************/
#include <machine.h>
/************************************************************************/
/* Symbol Definition                                                    */
/************************************************************************/
struct BIT {
unsigned char b7:1;                                     /* bit7                     */
unsigned char b6:1;                                     /* bit6                     */
unsigned char b5:1;                                     /* bit5                     */
unsigned char b4:1;                                     /* bit4                     */
unsigned char b3:1;                                     /* bit3                     */
unsigned char b2:1;                                     /* bit2                     */
unsigned char b1:1;                                     /* bit1                     */
unsigned char b0:1;                                     /* bit0                     */
};
struct P4BIT {
unsigned char H:4;                                      /* bit7-bit4                */
unsigned char L:4;                                      /* bit3-bit0                */
};
#define DTCR *(volatile unsigned char *)0xFFFC68        /* DTMF Control Register    */
#define DTCR_BIT (*(struct BIT *)0xFFFC60)              /* DTMF Control Register    */
#define DTEN DTCR_BIT.b7                                /* DTMF generation          */
#define CLOE DTCR_BIT.b5                                /* Column section outputs   */
#define RWOE DTCR_BIT.b4                                /* Column section outputs   */
#define DTLR *(volatile unsigned char *)0xFFFC69        /* DTMF Load Register       */
```

```
#define P7DDR *(volatile unsigned char *)0xFFFE36        /* Port 7 Data Direction Register     */
#define P7DR *(volatile unsigned char *)0xFFFF06         /* Port 7 Data Register               */
#define PORT7 *(volatile unsigned char *)0xFFFFB6        /* Port 7 Register                    */
#define PORT7_BIT (*(struct P4BIT *)0xFFFFB6)            /* Port 7 Register                    */
#define PORT7H PORT7_BIT.H                               /* P77-P74                            */
#define PORT7L PORT7_BIT.L                               /* P73-P70                            */
#define MSTPCRC *(volatile unsigned char *)0xFFFDEA      /* Module Stop Control Registers C    */
/************************************************************/
/* Function define                                          */
/************************************************************/
extern void INIT ( void );                               /* SP Set                             */
void main ( void );
unsigned char dtmftable[4][4] = {                        /* DTMF Waveform Output Table         */
0xF0,0xF4,0xF8,0xFC,                                     /* R1 C1,C2,C3,C4                     */
0xF1,0xF5,0xF9,0xFD,                                     /* R2 C1,C2,C3,C4                     */
0xF2,0xF6,0xFA,0xFE,                                     /* R3 C1,C2,C3,C4                     */
0xF3,0xF7,0xFB,0xFF,                                     /* R4 C1,C2,C3,C4                     */
};
unsigned char keyselect[4] = {
0xE0,
0xD0,
0xB0,
0x70,
};
/************************************************************/
/* Vector Address                                           */
/************************************************************/
#pragma section V1                                       /* VECTOR SECTOIN SET                 */
void (*const VEC_TBL1[])(void) = {                       /* 0x00 - 0x0f                        */
INIT                                                     /* 00 Reset                           */
};
#pragma section                                          /* P                                  */
/************************************************************/
/* Main Program                                             */
/************************************************************/
void main ( void )
{
unsigned char i,j,keydt;
set_imask_ccr(1);                                    /* Interrupt Disable                  */
MSTPCRC = 0xFB;                                      /* module stop mode is cleared        */
DTLR = 0xD9;                                         /* Make 400kHz for DTMF Circuit       */
P7DDR = 0xF0;                                        /* Set P77-4Output, P73-0Input Port   */
P7DR = 0xF0;                                         /* P77-4 Port 1set                    */
while(1){
for(j = 0; j < 4; j++){
P7DR = keyselect[j];                                 /* Set Key Select                     */
if(PORT7L != 0x0F){                                  /* Touch Key?                         */
keydt = PORT7L>>1;                                   /* What Key?                          */
keydt = 0x07 - keydt;
for(i = 0; keydt != 0; i++){
keydt = keydt>>1;
}
DTCR = dtmftable[i][j];                              /* DTMF Data Set                      */
do{
```

```
keydt = PORT7L;
}while(keydt != 0x0F);                          /* Touch Key?                  */
DTCR = 0xC0;                                    /* Stop DTMF                   */
}
}
}
}
```

7. Link Addresses

Section	Address
CV1	H' 000000
P	H' 000100

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.09.05	—	First edition issued

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