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April 1st, 2010
Renesas Electronics Corporation

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H8S Family

15-Phase PWM Output

Introduction

A 15-phase PWM waveform with variable duty cycle is output with the desired cycle.

Target Device

H8S/2339

Contents

1. Specifications

(1) Outputs 15-phase PWM waveforms with variable duty cycles, as shown in figure 1.
(2) In operation at 19.6608 MHz, the period of the output PWM signal can be set to any desired value from about 50.86 ns to 3.33 ms by the value set in pwm_cyc.

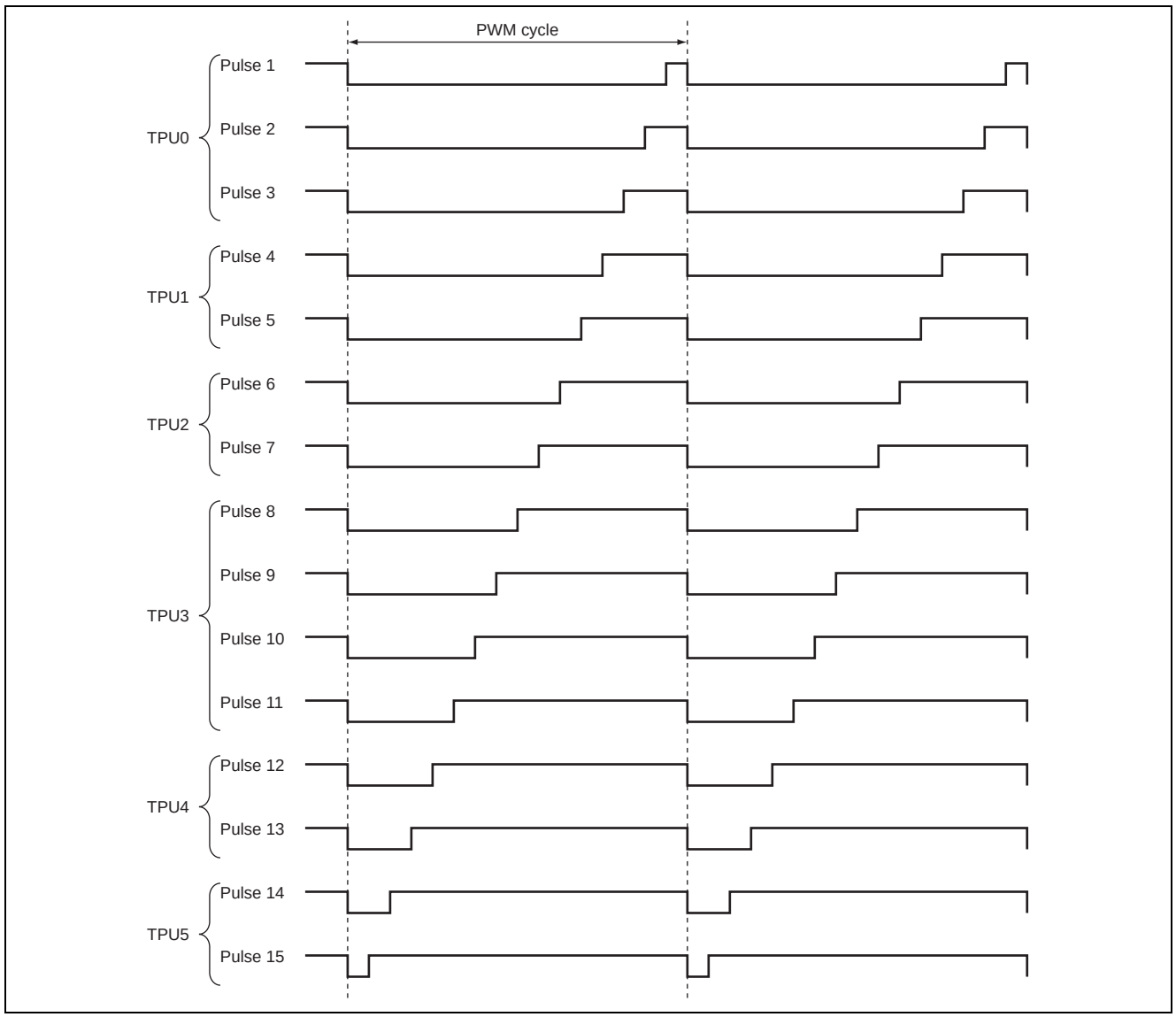


Figure 1 Example of PWM-Waveform Output

2. Description of Module Usage

(1) TPU0 to TPU5 operate in synchronization to produce 15 PWM waveforms with different phases.

(a) Figure 2 is a block diagram of how the TPUs are used in this sample task, which demonstrates how up to 15 PWM waveforms with different phases can be output through synchronized operation of the TPU functions (PWM mode 2).

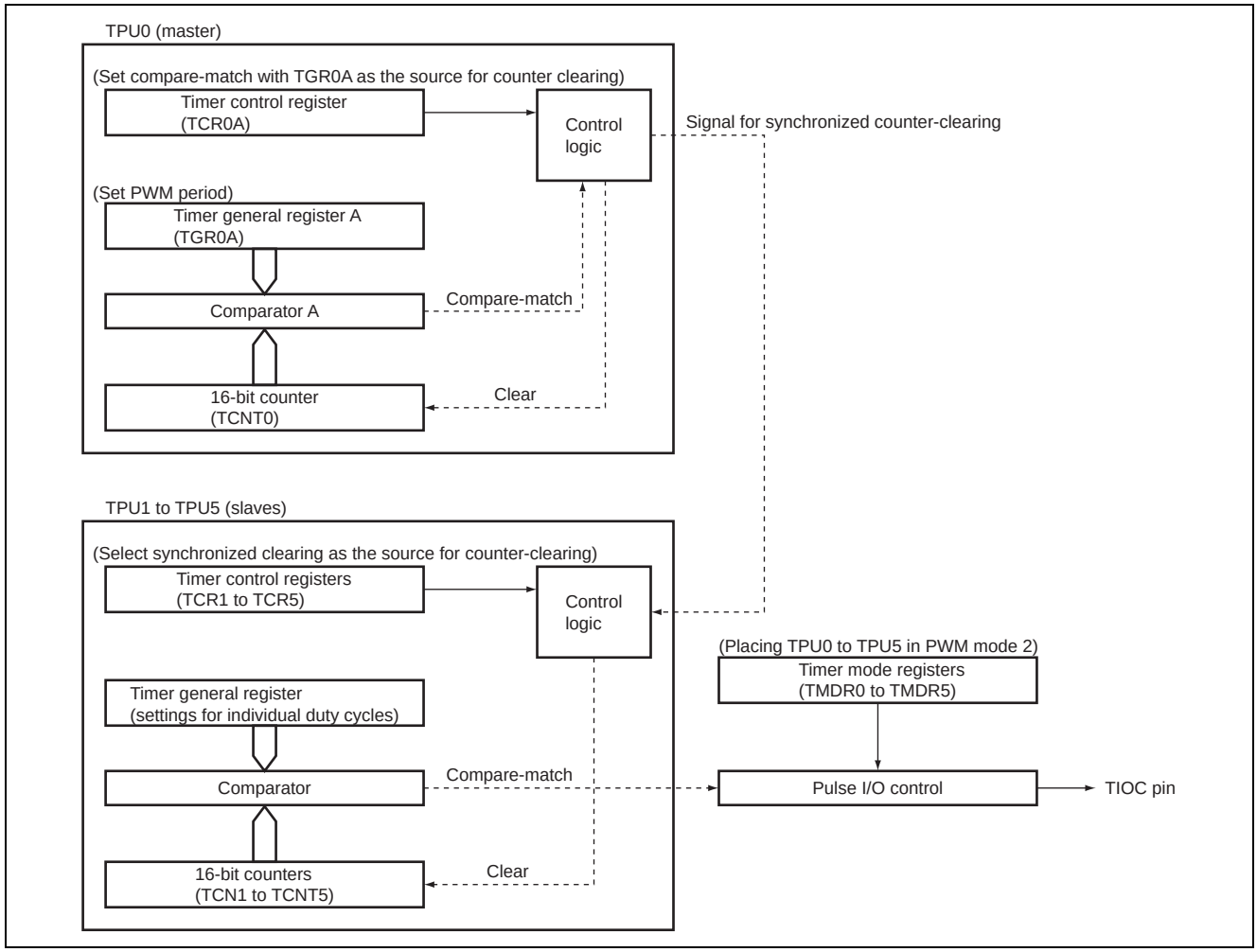
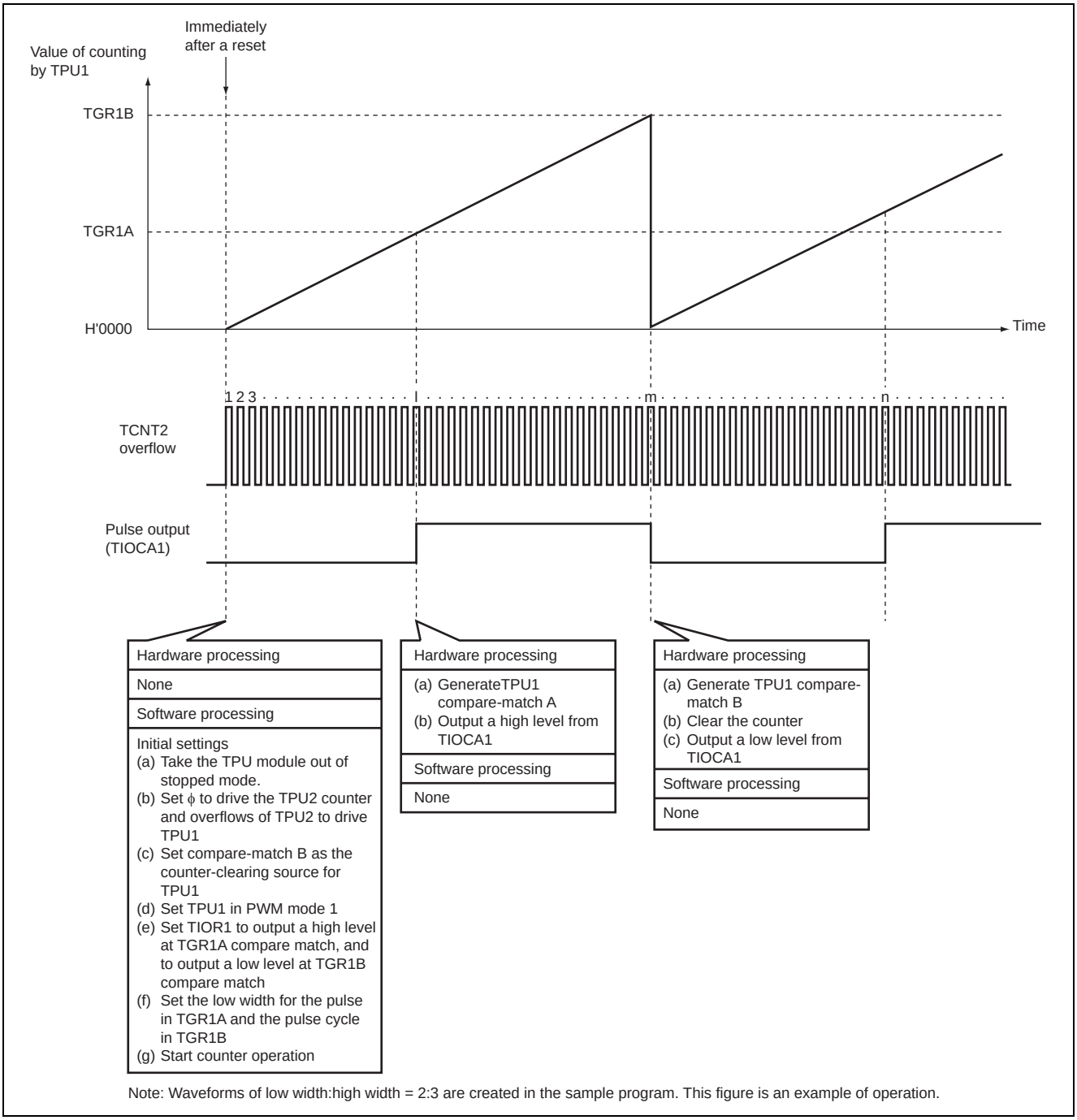


Figure 2 15-Phase PWM Output

3. Principles of Operation

The principle of operation for 15-phase PWM output is shown in figure 3. As the figure shows, the pulse trains are output on the PWM-output pins, TPU0 to TPU5, through a combination of hardware and software processing.



Note: Waveforms of low width:high width = 2:3 are created in the sample program. This figure is an example of operation.

Figure 3 Principle of Operation for 15-Phase PWM Output

4. Software Description

(1) Function

Function	Label	Description
Main routine	pwrn15mn	Settings for simultaneous clearing of channels 0 to 5 and PWM output

(2) Arguments

Label	Description	Data Type	Used in	I/O
pwm[0] to pwm[14]	The timer-counter settings for low pulse width. The following expression governs pulse width. Low pulse width (ns) = timer-counter value x ϕ period (50.86 ns in operation at 19.66 MHz) x frequency divisor for the input clock on each channel	unsigned short	Main routine	Input
pwm_cyc	The timer-counter setting for PWM period. The following expression governs PWM period. PWM period (ns) = timer-counter value x ϕ period (50.86 ns in operation at 19.66 MHz) x frequency divisor for the input clock on each channel	unsigned short	Main routine	Input

(3) Internal Registers

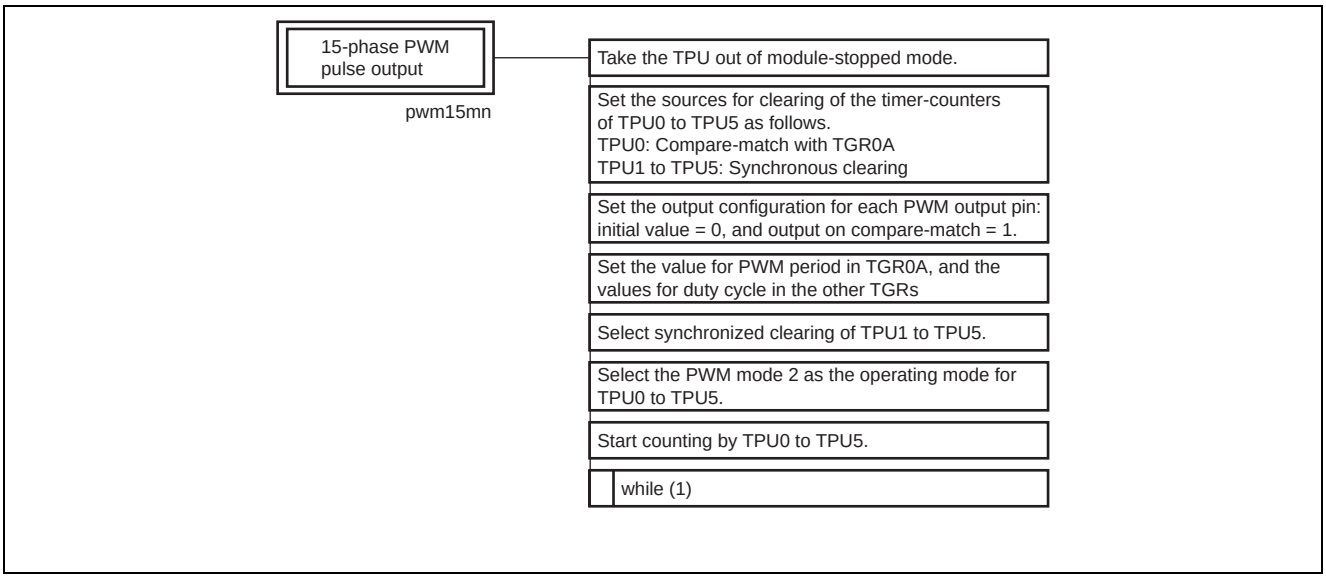
Register	Description	Used in
TSTR	Starts and stops counting by the timer counters of TPU0 to TPU5.	Main routine
TSYR	Selects synchronous operation for the timer counters of TPU0 to TPU5	Main routine
TCR0	Sets compare-match with TGR0A as the source for clearing the timer counters	Main routine
TCR1 to TCR5	Sets synchronous clearing as the source for clearing of the timer counters	Main routine
TIOR0 to TIOR5	Sets output on each of the PWM output pins	Main routine
TMDR0 to TMDR5	Selects PWM mode 2	Main routine
TGR0A	Sets the PWM cycle	Main routine
TGR0B to TGR5B	Sets the timer-counter values at which the levels on the PWM output pins go high	Main routine
MSTPCR	Takes the TPU out of module-stopped mode	Main routine

(4) RAM Usage

Label	Set value of the sample task
pwm[0] to [14]	H'07FF, H'03FF, H'01FF, H'00FF, H'007F, H'003F, H'001F, H'000F, H'000D, H'000B, H'0009, H'0007, H'0005, H'0003, H'0001
pwm_cyc	H'0FFF

5. PAD

(1) Main routine



Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Feb.17.05	—	First edition issued

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