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# H8/38076R

## Measuring Number of Input Pulses Using 16-Bit Event Counter Function of Timer F

## Introduction

The 16-bit event counter function of timer F is used to count the rising edges of pulses input to the timer F event input (TMIF) pin.

## Target Device

H8/38076R

## Contents

# 1.    Specifications

In this sample task timer counter F (TCF) is set to count the rising edges of an external clock input to the timer F event input (TMIF) pin. Timer counter F continues counting up until the rising edge count reaches 1,024.

# 2.    Description of Functions

## 2.1    Functions

When the rising edge count reaches 1,024 the external clock input to TCF is halted and the sample task ends. In this sample task the 16-bit event counter function of timer counter F is used to measure the number of pulses input to the TMIF pin. A block diagram of the 16-bit event counter function of timer F is shown in figure 1. The 16-bit event counter function of timer F is described below.

1.  Timer F Functions
    This 16-bit timer has an output compare function. It can be used for external event counting or as a multifunction timer for a variety of applications, including counter resetting, interrupt request, and toggle output using compare match signals. It can also be used as two independent 8-bit timers (timer FH and timer FL).

- Timer counter F (TCF)
    TCF is a 16-bit readable/writeable up-counter that is incremented by input of an internal or an external clock. Five input clock options are available: the system clock divided by 4, 16, or 32; the subclock divided by 4; or an external clock.
    In this sample task external clock is selected as the TCF input clock.
- Timer control register F (TCRF)
    TCRF is an 8-bit readable/writeable register used for switching between 16-bit mode and 8-bit mode and for selecting among the four internal clocks and an external event.
- Timer control/status register F (TCSRF)
    TCSRF is an 8-bit register used for counter clear selection, overflow flag and compare match flag settings, and controlling the enabling of overflow interrupt requests.

2.  I/O Port Functions
    The following port setting is performed.

- Port mode register 4 (PMR4)
    PMR4 is used to set the P40/SCK31/TMIF pin as a TMIF pin.

3.  Interrupt Controller Functions
    The following registers are used to control interrupts.

- Interrupt enable register 2 (IENR2)
    IENR2 controls timer F interrupts.
- Interrupt request register 2 (IRR2)
    IRR2 is the interrupt request status register for timer F interrupts.
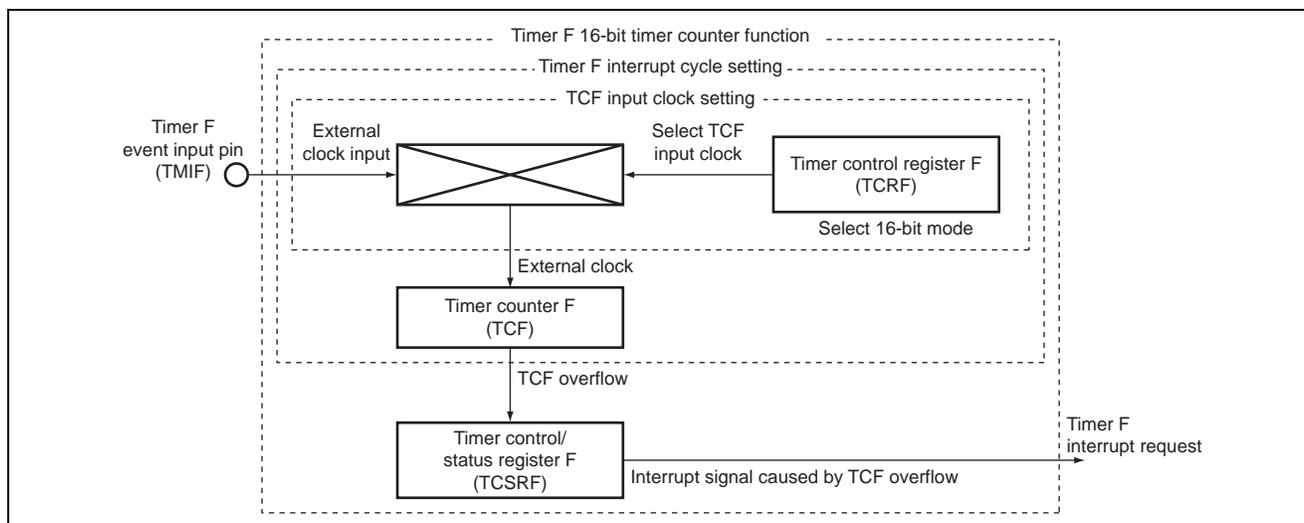
**Figure 1  Block Diagram of 16-Bit Event Counter Function of Timer F**

## 2.2      Assignment of Functions

Table 1 shows the assignment of functions in this sample task. With functions assigned as shown in table 1 the 16-bit event counter function of timer F is used to measure the number of input pulses.

**Table 1  Assignment of Functions**

| Elements | Description |
|----------|-------------|
| TCF | 16-bit counter using external clock input |
| TCRF | Sets TCF to 16-bit mode, selects external clock as TCF input clock |
| TCSRF | Timer F status register, enables TCF overflow interrupts, disables clearing TCF by compare match |
| IENTFH | Enables interrupt requests at timer F overflow |
| IRRTFH | Interrupt flag set by timer F overflow |
| TMIF | Input pin for external event input to TCFL |

## 3. Principles of Operation

The principles of operation of this sample task are illustrated in figure 2. Using the hardware and software processing shown in figure 2 the 16-bit event counter function of timer F is used to measure the number of input pulses.
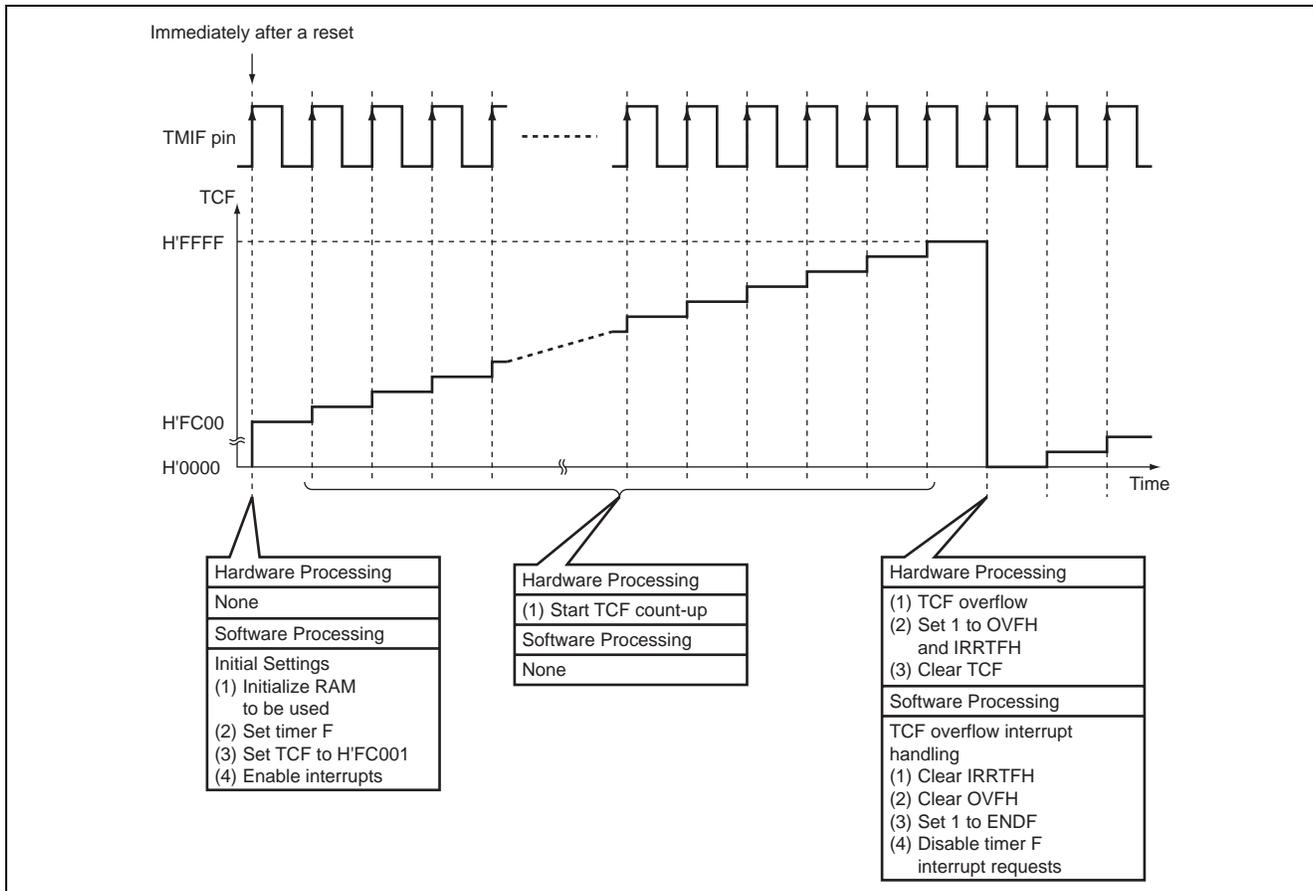


**Figure 2  Principles of Operation**

# 4. Description of Software

## 4.1 Description of Modules

Table 2 shows the modules used in this sample task.

**Table 2 Modules**

| Function Name | Description |
|---|---|
| main | Settings for timer F 16-bit event counter function, selects external clock the TCF input clock source, enables interrupts, ends when TCF input clock rising edge count reaches 1,024 |
| tfint | During timer F overflow interrupt handling, sets 1 to ENDF and disables timer F interrupt requests |

## 4.2 Arguments

No arguments are used in this sample task.

## 4.3 Description of Internal Registers

The internal registers used in this sample task are shown below.

- TCRF          Timer Control Register F          Address: H'FFB6

| Bit | Bit Name | Set Value | R/W | Description |
|---|---|---|---|---|
| 6 | CKSH2 | 0 | W | Clock Select H |
| 5 | CKSH1 | 0 | W | Selects the clock input to TCFH from among internal clock |
| 4 | CKSH0 | 0 | W | sources or TCFL overflow. |
| | | | | 000: 16-bit mode, counting on TCFL overflow signal |
| | | | | 001: 16-bit mode, counting on TCFL overflow signal |
| | | | | 010: 16-bit mode, counting on TCFL overflow signal |
| 2 | CKSL2 | 0 | W | Clock Select L |
| 1 | CKSL1 | 0 | W | Select the clock input to TCFL from among internal clock |
| 0 | CKSL0 | 0 | W | sources or external event input. |
| | | | | 000: Counting on rising or falling edge of an external event (TMIF pin)* |
| | | | | 001: Counting on rising or falling edge of an external event (TMIF pin)* |
| | | | | 010: Counting on rising or falling edge of an external event (TMIF pin)* |

Note: * The TMIFEG bit in IEGR selects which edge of an external event is used for counting.

- TCSRF　　　　　　Timer Control/Status Register F　　　　Address: H'FFB7

| Bit | Bit Name | Set Value | R/W | Description |
|-----|----------|-----------|-----|-------------|
| 7 | OVFH | Undefined | R/W* | Timer Overflow Flag H<br>[Setting condition]<br>- When TCFH overflows from H'FF to H'00<br>[Clearing condition]<br>- When 0 is written to this bit after reading it as 1 |
| 5 | OVIEH | 1 | R/W | Timer Overflow Interrupt Enable H<br>Enables or disables interrupt generation when TCFH overflows.<br>1: TCFH overflow interrupt requests enabled |
| 4 | CCLRH | 0 | R/W | Counter Clear H<br>In 16-bit mode this bit selects whether TCF is cleared when TCF and OCRF match.<br>In 16-bit mode:<br>0: TCF clearing by compare match disabled |

Note:　*　Only 0 can be written to clear the flag.

- TCF　　　　　　　Timer Counter F　　　　　　　　　Address: H'FFB8

| Bit | Bit Name | Set Value | R/W | Description |
|-----|----------|-----------|-----|-------------|
| 15 | Bit 15 | Undefined | R/W | Output Compare Register F |
| 14 | Bit 14 | Undefined | R/W | When CKSH2 in TCRF is set to 0 TCF operates as a 16-bit |
| 13 | Bit 13 | Undefined | R/W | counter. The TCF input clock is selected by bits CKSL2 to |
| 12 | Bit 12 | Undefined | R/W | CKSL0 in TCF. |
| 11 | Bit 11 | Undefined | R/W | TCF can be cleared in the event of a compare match by |
| 10 | Bit 10 | Undefined | R/W | CCLRH in TCSRF. |
| 9 | Bit 9 | Undefined | R/W | When TCF overflows from H'FFFF to H'0000, OVFH in |
| 8 | Bit 8 | Undefined | R/W | TCSRF is set to 1. If the value of OVIEH in TCSRF is 1 at this |
| 7 | Bit 7 | Undefined | R/W | time, IRRTFH in IRR2 is set to 1, and if in addition the value of |
| 6 | Bit 6 | Undefined | R/W | IENTFH in IENR2 is 1, an interrupt request is sent to the CPU. |
| 5 | Bit 5 | Undefined | R/W | |
| 4 | Bit 4 | Undefined | R/W | |
| 3 | Bit 3 | Undefined | R/W | |
| 2 | Bit 2 | Undefined | R/W | |
| 1 | Bit 1 | Undefined | R/W | |
| 0 | Bit 0 | Undefined | R/W | |

- PMR4　　　　　　Port Mode Register 4　　　　　　　Address: H'FFC3

| Bit | Bit Name | Set Value | R/W | Description |
|-----|----------|-----------|-----|-------------|
| 0 | TMIF | 1 | R/W | P40/SCK31/TMIF pin function switch<br>Selects whether pin P40/SCK31/TMIF is used as P40/SCK31 or as TMIF.<br>0: Functions as P40/SCK31 I/O pin<br>1: Functions as TMIF input pin |

- IEGR  Interrupt Edge Select Register  Address: H'FFF2

| Bit | Bit Name | Set Value | R/W | Description |
|---|---|---|---|---|
| 6 | TMIFEG | 1 | R/W | TMIF Edge Select<br>0: Detects the falling edge of the TMIF pin input<br>1: Detects the rising edge of the TMIF pin input |

- IENR2  Interrupt Enable Register 2  Address: H'FFF4

| Bit | Bit Name | Set Value | R/W | Description |
|---|---|---|---|---|
| 3 | IENTFH | 1 | R/W | Timer FH Interrupt Enable<br>Timer FH interrupt requests are enabled when this bit is set to 1.<br>1: Timer FH interrupt requests enabled |

- IRR2  Interrupt Request Register 2  Address: H'FFF7

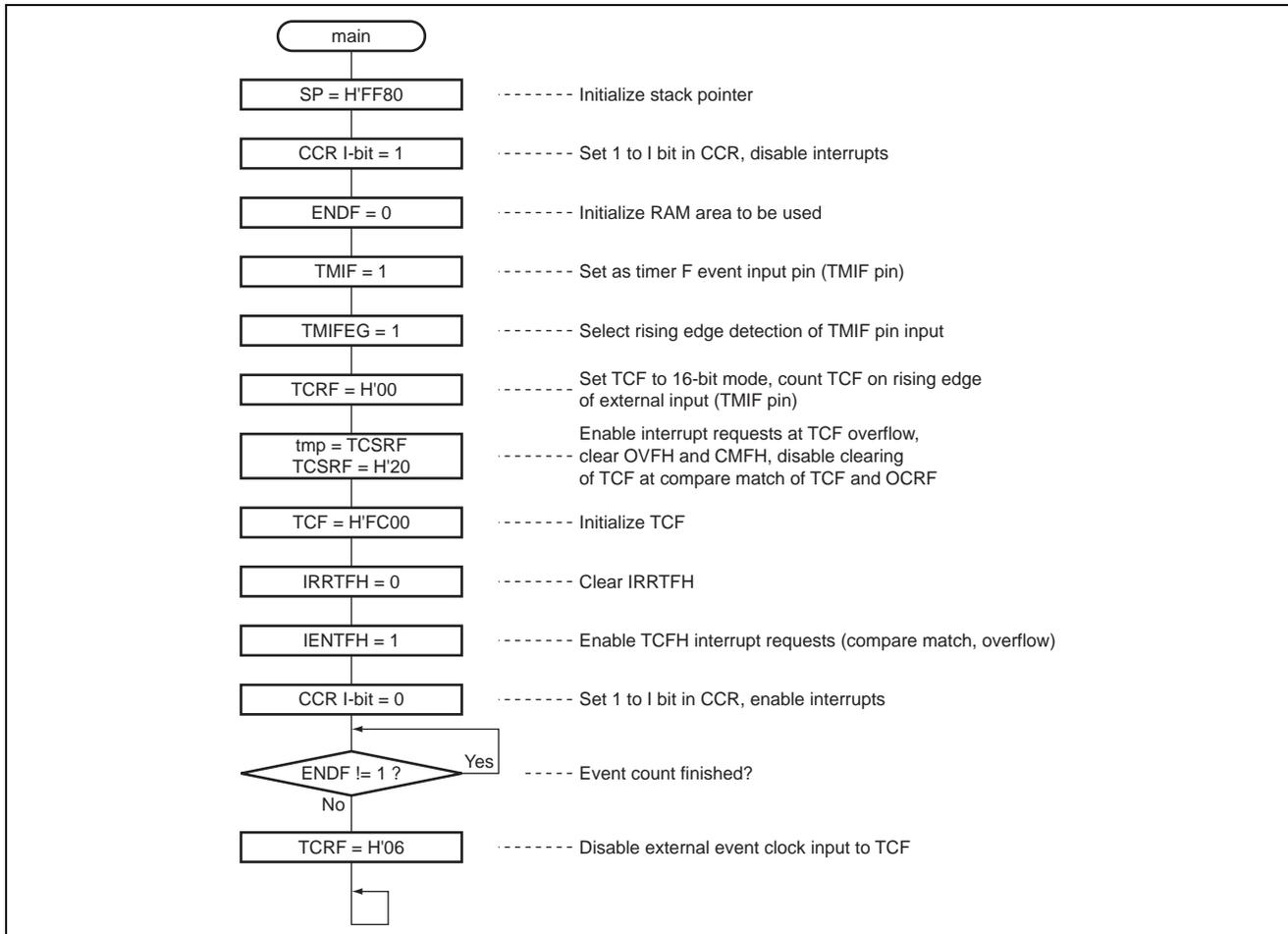| Bit | Bit Name | Set Value | R/W | Description |
|---|---|---|---|---|
| 3 | IRRTFH | Undefined | R/W | Timer FH Interrupt Request Flag<br>[Setting condition]<br>• When timer FH compare match or overflow occurs<br>[Clearing condition]<br>• When 0 is written to this bit |

## 4.4    RAM Usage

The RAM usage in this sample task is shown in table 3.
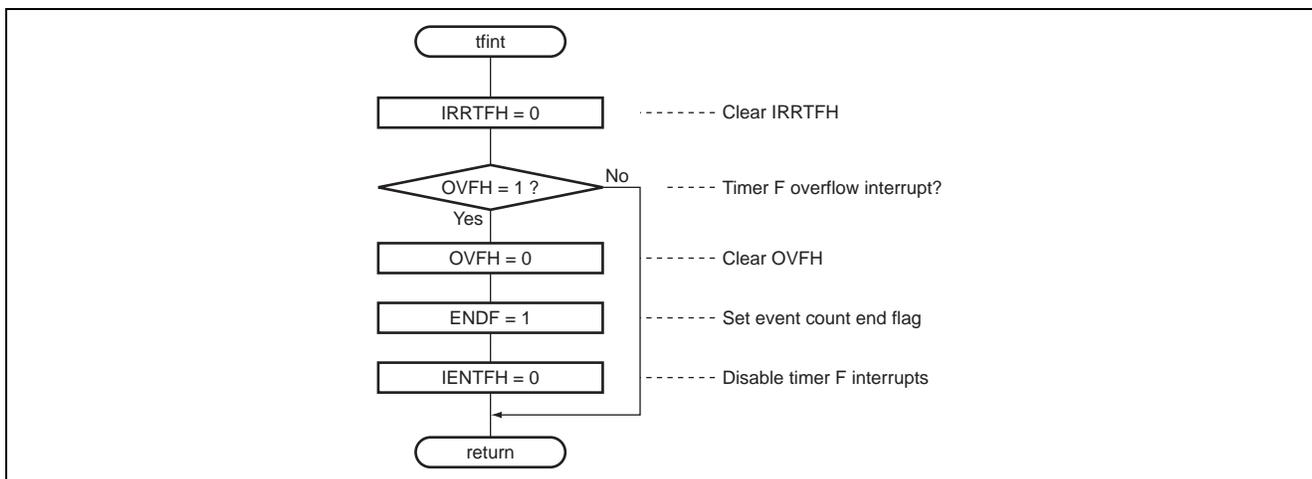
**Table 3  RAM Usage**

| Bit | Bit Name | Description | Amount of Memory Used | Used in |
|---|---|---|---|---|
| 0 | ENDF | Flag indicating that rising edge of input pulse has been detected 1,024 times | 1 bit | main<br>tfint |

## 5. Flowchart

### 5.1 main

```
                    ┌──────────┐
                    │   main   │
                    └────┬─────┘
              ┌──────────────────┐
              │   SP = H'FF80    │ ------- Initialize stack pointer
              └────────┬─────────┘
              ┌──────────────────┐
              │  CCR I-bit = 1   │ ------- Set 1 to I bit in CCR, disable interrupts
              └────────┬─────────┘
              ┌──────────────────┐
              │    ENDF = 0      │ ------- Initialize RAM area to be used
              └────────┬─────────┘
              ┌──────────────────┐
              │    TMIF = 1      │ ------- Set as timer F event input pin (TMIF pin)
              └────────┬─────────┘
              ┌──────────────────┐
              │   TMIFEG = 1     │ ------- Select rising edge detection of TMIF pin input
              └────────┬─────────┘
              ┌──────────────────┐
              │   TCRF = H'00    │ ------- Set TCF to 16-bit mode, count TCF on rising edge
              └────────┬─────────┘           of external input (TMIF pin)
              ┌──────────────────┐           Enable interrupt requests at TCF overflow,
              │   tmp = TCSRF    │ ------- clear OVFH and CMFH, disable clearing
              │  TCSRF = H'20    │           of TCF at compare match of TCF and OCRF
              └────────┬─────────┘
              ┌──────────────────┐
              │   TCF = H'FC00   │ ------- Initialize TCF
              └────────┬─────────┘
              ┌──────────────────┐
              │   IRRTFH = 0     │ ------- Clear IRRTFH
              └────────┬─────────┘
              ┌──────────────────┐
              │   IENTFH = 1     │ ------- Enable TCFH interrupt requests (compare match, overflow)
              └────────┬─────────┘
              ┌──────────────────┐
              │  CCR I-bit = 0   │ ------- Set 1 to I bit in CCR, enable interrupts
              └────────┬─────────┘
                       │◄──────────────┐
                     ◇─┴─◇    Yes      │
                   ◇  ENDF  ◇──────────┤ ----- Event count finished?
                   ◇ != 1 ? ◇          │
                     ◇─┬─◇             │
                       │ No            │
              ┌──────────────────┐     │
              │   TCRF = H'06    │ ----│-- Disable external event clock input to TCF
              └────────┬─────────┘     │
                       └──────►────────┘
                           ┌──┐
                           └──┘
```

### 5.2 tfint

```
                    ┌──────────┐
                    │  tfint   │
                    └────┬─────┘
              ┌──────────────────┐
              │   IRRTFH = 0     │ ------- Clear IRRTFH
              └────────┬─────────┘
                     ◇─┴─◇    No
                   ◇  OVFH  ◇─────────────┐
                   ◇ = 1 ?  ◇             │ ----- Timer F overflow interrupt?
                     ◇─┬─◇               │
                       │ Yes             │
              ┌──────────────────┐       │
              │    OVFH = 0      │ ------│- Clear OVFH
              └────────┬─────────┘       │
              ┌──────────────────┐       │
              │    ENDF = 1      │ ------│- Set event count end flag
              └────────┬─────────┘       │
              ┌──────────────────┐       │
              │   IENTFH = 0     │ ------│- Disable timer F interrupts
              └────────┬─────────┘       │
                       │◄───────────────┘
                    ┌──────────┐
                    │  return  │
                    └──────────┘
```

## 5.3    Link Address Specifications

| Section Name | Address |
|---|---|
| CVECT | H'0000 |
| P | H'0100 |
| B | H'F780 |

## Revision Record

| | | Description | |
|---|---|---|---|
| **Rev.** | **Date** | **Page** | **Summary** |
| 1.00 | Mar.18.05 | — | First edition issued |

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