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H8/38076R

Clock-Synchronous Serial Data Reception (Slave Reception)

Introduction

Serial data received using the clock-synchronous mode of the serial communication interface 3 (SCI3).

Target Device

H8/38076R

Contents

1. Specifications

- Four bytes of 8-bit data are received using the clock-synchronous mode.
- An external clock is used as the transfer clock.
- The data transferred has a data length of 8 bits. It is received with LSB-first, which is beginning with the lowest bit.
- Channel 1 is used for the transfer.
- Figure 1 shows a connection diagram for serial data reception (master reception) in clock-synchronous mode.

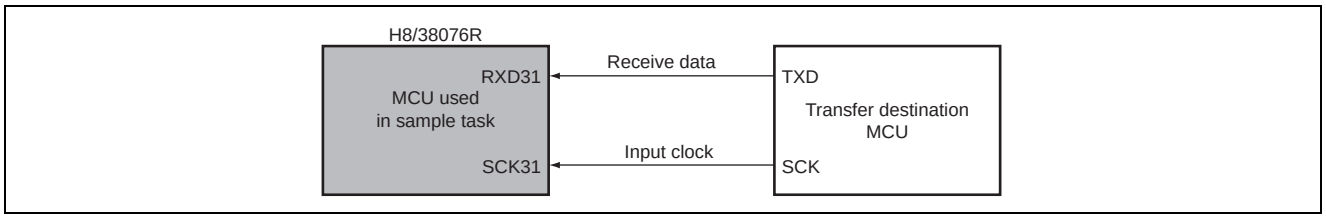


Figure 1 Serial Data Reception (Master Reception) in Clock-Synchronous Mode

2. Functions Used

2.1 Functions

In this sample task serial data is received using the clock-synchronous mode of the serial communication interface 3 (SCI3). A block diagram of the serial communication interface 3 is shown in figure 2, and the functions used in this sample task are described below.

1. System Clock (ϕ)
   This 10-MHz oscillation clock is the reference clock for operation of the CPU and peripheral functions.

2. SCI3 Clock-Synchronous Mode
   In the clock-synchronous mode, data is transmitted and received in synchronization with clock pulses. A single character of transmit data comprises 8 bits of data, starting from the LSB. When transmitting the data using the SCI3, output data is retained from one falling edge of the synchronization clock pulse to the next. When receiving the SCI3 receives data in synchronization with the rising edge of the clock pulse. After the MSB (most significant bit) is output the communication line holds the MSB output state. In clock-synchronous mode no parity or multiprocessor bit is added. Inside the SCI3 the transmitter and receiver are independent units, enabling full-duplex communication by using a common clock. Both the transmitter and the receiver also have a double-buffered structure, so the next data can be written while transmission is in progress and the preceding data can be read while reception is in progress, enabling continuous data transfer.

- Receive shift register 3 (RSR3)
  RSR3 is a shift register that receives serial data input from the RXD31 or RXD32 pin and converts it into parallel data. When one frame of data has been received, it is transferred automatically to RDR3. RSR3 cannot be directly accessed by the CPU.

- Receive data register 3 (RDR3)
  RDR3 is an 8-bit register that stores receive data. When one frame of data has been received, it is transferred from RSR3 to RDR3, enabling RSR3 to receive the next frame of data. RSR3 and RDR3 have a double-buffered structure, so continuous reception is possible. Read RDR3 only once, after confirming that the receive data register full (RDRF) bit in serial status register 3 (SSR3) is set to 1. RDR3 cannot be written by the CPU. The initial value of RDR3 is H'00.
  RDR3 is initialized to H'00 by a reset or in standby mode, watch mode, or module standby mode.

- Serial mode register 3 (SMR3)
  SMR3 is a register for selecting the serial communication format and the clock source for the internal baud rate generator. In this sample task the clock-synchronous mode is selected.

- Serial control register 3 (SCR3)
  SCR3 is a register that controls transmission and reception and interrupts, and selects the clock source. An external clock is used as the clock source in this sample task, so the SCK31 pin functions as a clock input pin. No interrupts are used in this sample task because data transfer is performed using polling.

- Serial status register 3 (SSR3)
  SSR3 consists of status flags and multiprocessor bits for transmission and reception. In this sample task the RDRF bit is polled and the receive data is read in after the preceding frame has been transferred from RSR to RDR3.

- Bit rate register 3 (BRR3)
  BRR3 sets the bit rate. It is not used in this sample task because an external clock is employed.

- Serial port control register (SPCR)
  SPCR switches the functions of the TXD32 and TXD31 pins and controls data inversion of the transmit and receive pins. In this sample task data is input to the RXD31 pin unmodified (without inversion).

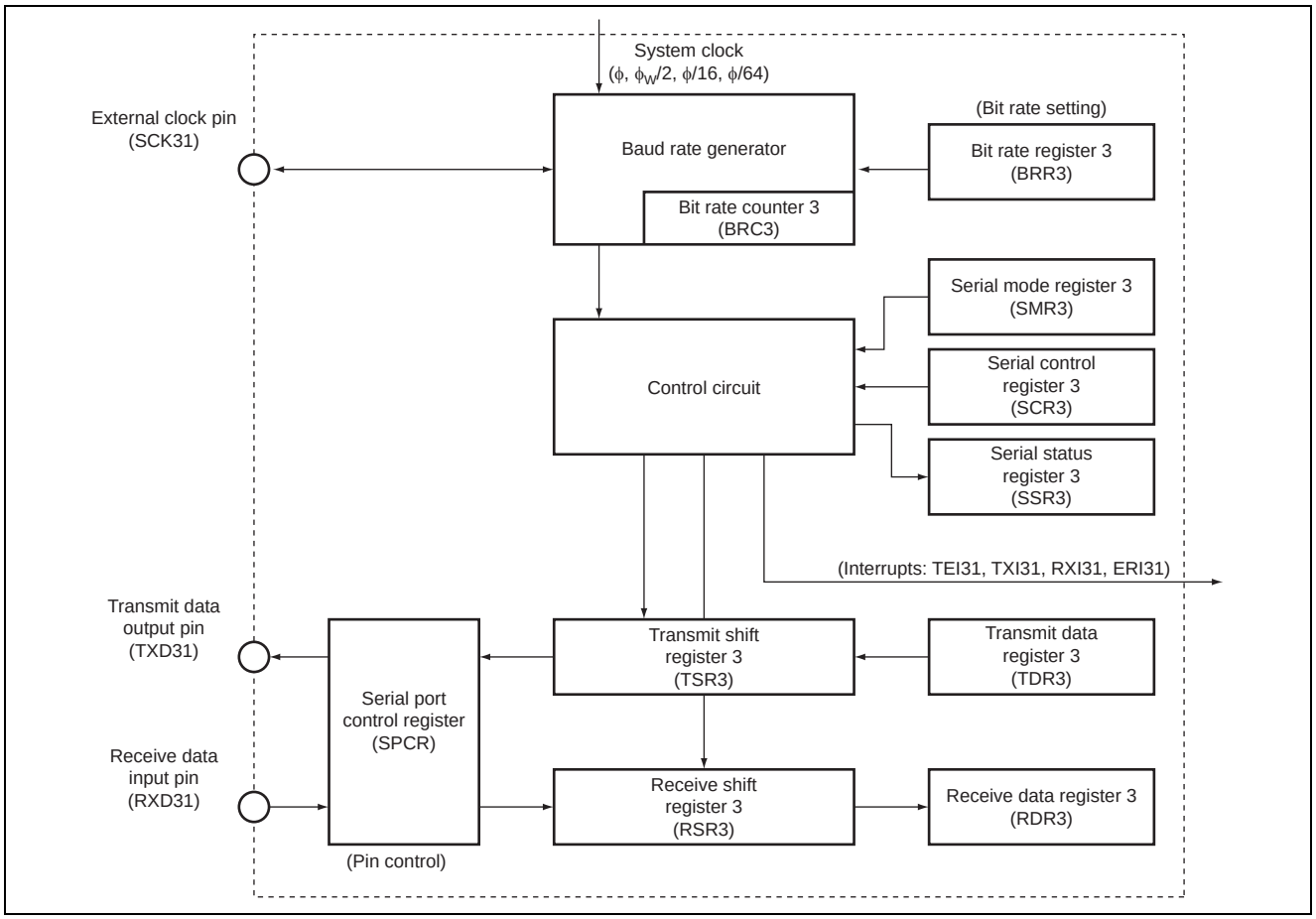


Figure 2 Block Diagram of SCI3

2.2 Assignment of Functions

Table 1 shows the assignment of functions in this sample task. Serial data reception in the clock-synchronous mode is performed using functions assigned as shown in table 1.

Table 1 Assignment of Functions

Elements	Description
RDR3	8-bit register for storing receive data
SMR3	Sets clock-synchronous mode
SCR3	Enables reception, sets external clock as clock source
SSR3	Status flag showing the operating status of the SCI3
SPCR	Specifies that data is input to the RXD31 pin unmodified
SCK31	Clock input pin of SCI3
RXD31	Receive data output pin of SCI3

3. Principles of Operation

The principles of operation for this sample task are illustrated in figure 3. Serial data in the clock-synchronous mode is received using the hardware and software processings shown below.

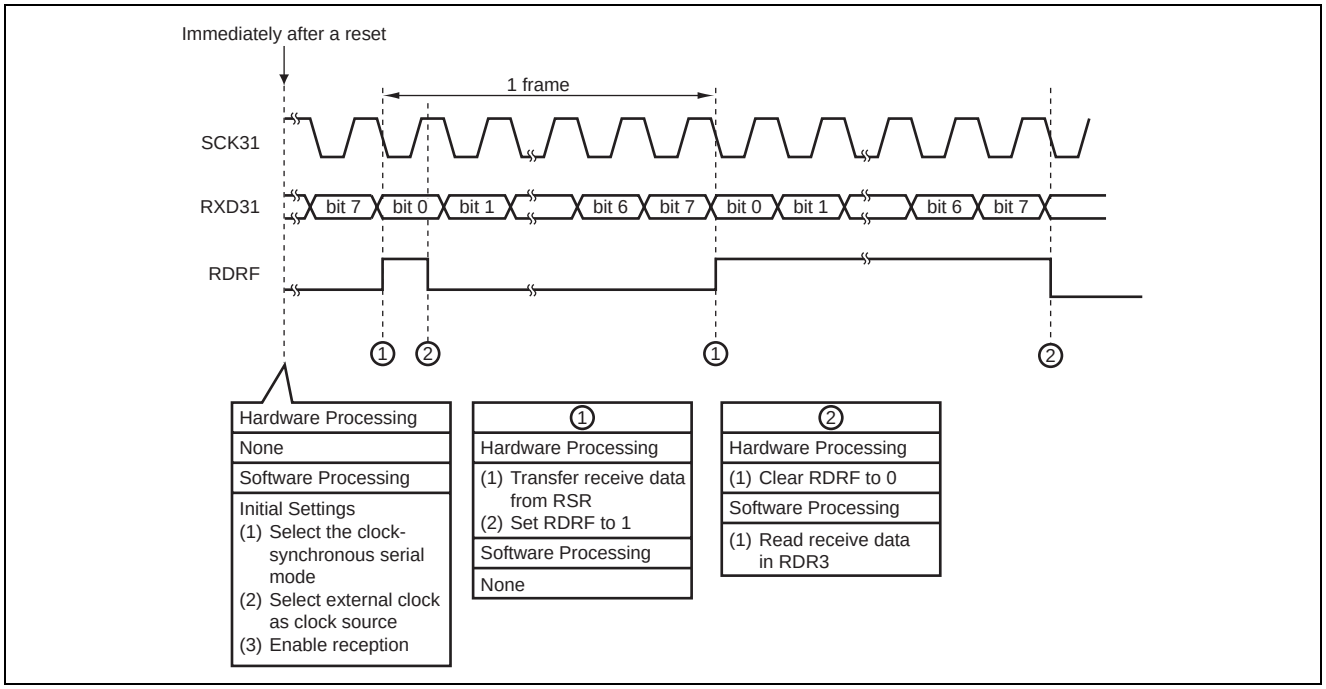


Figure 3 Principles of Operation for Serial Data Reception in the Clock-Synchronous Mode

4. Description of Software

In this sample task serial data is received in the clock-synchronous mode. The functions used are listed below.

4.1 Description of Functions

Table 2 List of Functions

Function Name	Description
main	Controls serial data reception in the clock-synchronous mode
init_sci3	Initializes the SCI3
rcv_sci3	Receives serial data in the clock-synchronous mode
stop_sci3	Ends the clock-synchronous mode

4.2 Description of Constants

The constants used in this sample task are listed in table 3.

Table 3 Constants

Label Name	Constant Value	Description	Used in
DATA_NUM	4	Receive data size	main

4.3 RAM Usage

Table 4 shows the RAM used in this sample task.

Table 4 RAM Usage

Label Name	Description	Memory Consumption	Used in
r_buf[4]	Receive data storage buffer	1 byte	main

4.4 Modules

4.4.1 main() Function

1. Module Specifications

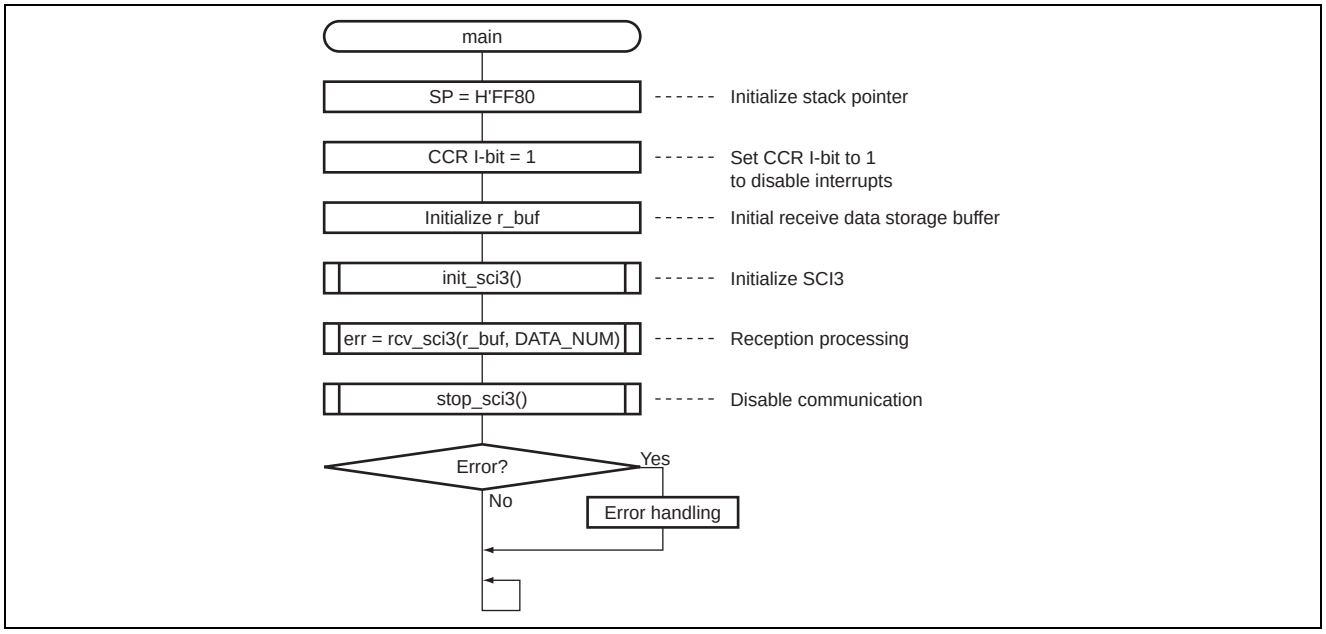
- Controls serial data reception in the clock-synchronous mode

Table 5 Module Specifications

Item	Type	Variable	Description
Arguments	None	None	None

2. Internal Registers Used
   None

3. Flowchart



4.4.2 init_sci3 Function

1. Module Specifications

- Initializes the clock-synchronous mode

Table 6 Module Specifications

Item	Type	Variable	Description
Arguments	None	None	None

2. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- SPCR Serial Port Control Register Address: H'FF91

Bit	Bit Name	Set Value	R/W	Description
0	SCINV0	0	R/W	RXD31 Pin Input Data Inversion Switch Selects whether data input to the RXD31 pin is inverted or not. 0: RXD31 input data not inverted 1: RXD31 input data inverted

- SMR3 Serial Mode Register 3 Address: H'FF98

Bit	Bit Name	Set Value	R/W	Description
7	COM	1	R/W	Communication Mode 0: Asynchronous mode 1: Clock synchronous mode
6	CHR	0	R/W	Character Length In the clock-synchronous mode the data length is fixed at 8 bits regardless of the CHR bit setting.

- SCR3 Serial Control Register 3 Address: H'FF9A

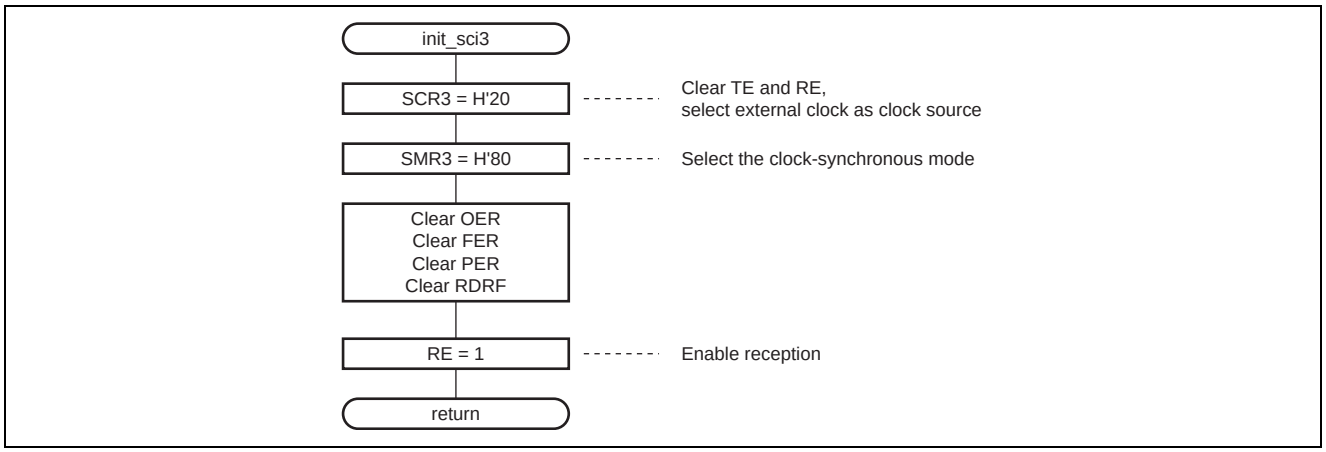
Bit	Bit Name	Set Value	R/W	Description
4	RE	1	R/W	Receive Enable Reception is enabled when this bit is set to 1. In this state serial data reception is started when serial clock input is detected in clock-synchronous mode. Be sure to carry out SMR3 settings to decide the reception format before setting the RE bit to 1. Note that the RDRF, FER, PER, and OER flags in SSR3 are not affected when the RE bit is cleared to 0, and retain their previous state.
1	CKE1	1	R/W	Clock Enable 0 and 1
0	CKE0	0	R/W	Selects the clock source. Clock-synchronous mode 10: External clock (SCK31 or SCK32 pin functions as clock input)

- SSR3 Serial Status Register 3 Address: H'FF9C

Bit	Bit Name	Set Value	R/W	Description
6	RDRF	0	R/(W)*	Receive Data Register Full Indicates whether or not receive data is stored in RDR3. [Setting condition] • When reception ends normally and receive data is transferred from RSR3 to RDR3 [Clearing conditions] • When 0 is written to RDRF after it was read as 1 • When data is read from RDR3 If an error is detected during reception, or if the RE bit in SCR3 has been cleared to 0, RDR3 and the RDRF bit are not affected and retain their previous state. Note that if data reception is completed while bit RDRF is still set to 1, an overrun error (OER) will occur and the receive data will be lost.
5	OER	0	R/(W)*	Overrun Error [Setting condition] • When an overrun error occurs during reception [Clearing condition] • When 0 is written to OER after it was read as 1 When the RE bit in SCR3 is cleared to 0, the OER bit is not affected and retains its previous state. When an overrun error occurs, RDR3 retains the receive data it held before the overrun error occurred, and data received after the error is lost. Reception cannot be continued with the OER bit set to 1, and in the clock-synchronous mode, transmission cannot be continued either.
4	FER	0	R/(W)*	Framing Error [Setting condition] • When a framing error occurs during reception [Clearing condition] • When 0 is written to FER after it was read as 1 In the clock-synchronous mode neither transmission nor reception is possible when the FER bit is set to 1. In this sample task FER is only cleared when SCI3 is initialized.
3	PER	0	R/(W)*	Parity Error [Setting condition] • When a parity error is generated during reception [Clearing condition] • When 0 is written to PER after it was read as 1 In the clock-synchronous mode neither transmission nor reception is possible when the PER bit is set to 1. In this sample task PER is only cleared when SCI3 is initialized.

Note: * Only 0 can be written to clear the flag.

3. Flowchart


init_sci3
SCR3 = H'20
Clear TE and RE,
select external clock as clock source
SMR3 = H'80
Select the clock-synchronous mode
Clear OER
Clear FER
Clear PER
Clear RDRF
RE = 1
Enable reception
return

4.4.3 rcv_sci3() Function

1. Module Specifications

- Receives serial data in the clock-synchronous mode

Table 7 Module Specifications

Item	Type	Variable	Description
Arguments	unsigned char *	r_ptr	Receive data pointer
	unsigned char	cnt	Reception count
Return value	unsigned char	err	Indicates whether or not an error has been generated

2. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- SSR3 Serial Status Register 3 Address: H'FF9C

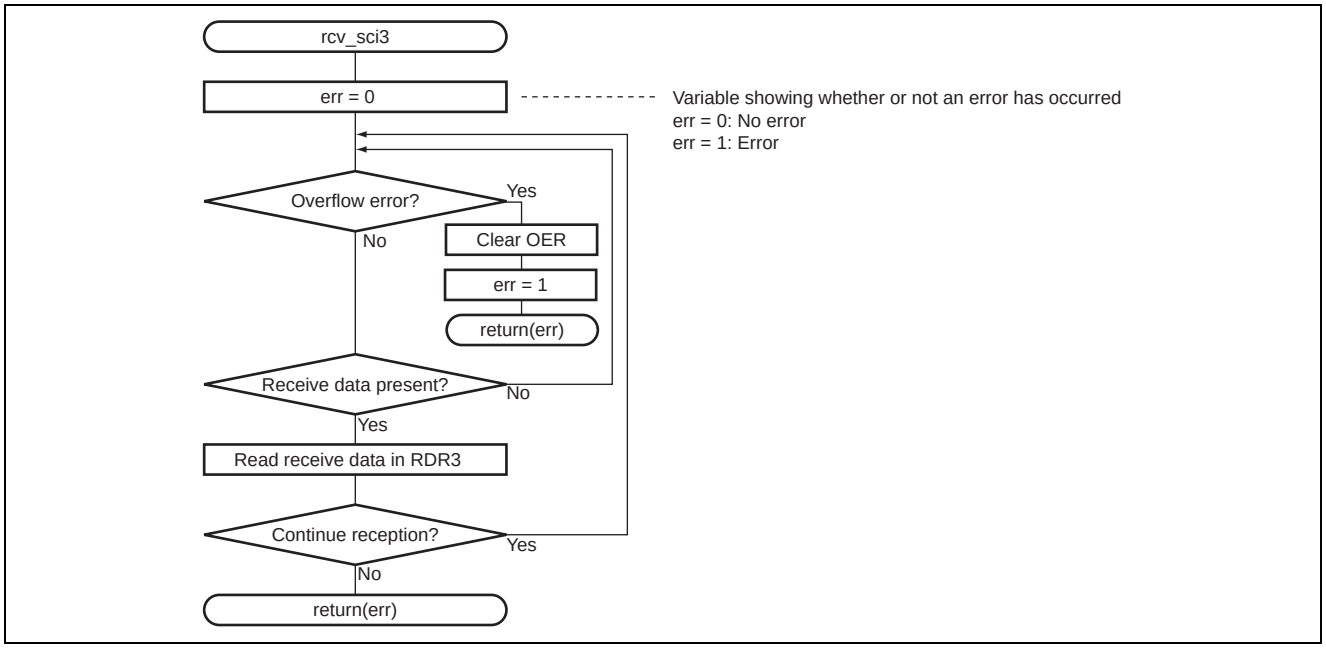
Bit	Bit Name	Set Value	R/W	Description
6	RDRF	Undefined	R/(W)*	Receive Data Register Full Indicates whether or not receive data is stored in RDR3. [Setting condition] • When reception ends normally and receive data is transferred from RSR3 to RDR3 [Clearing conditions] • When 0 is written to RDRF after it was read as 1 • When receive data is read from RDR3 If an error is detected during reception, or if the RE bit in SCR3 has been cleared to 0, RDR3 and the RDRF bit are not affected and retain their previous state. Note that if data reception is completed while bit RDRF is still set to 1, an overrun error (OER) will occur and the receive data will be lost.
5	OER	Undefined	R/(W)*	Overrun error [Setting condition] • When an overrun error occurs during reception [Clearing condition] • When 0 is written to OER after it was read as 1 When the RE bit in SCR3 is cleared to 0, the OER bit is not affected and retains its previous state. When an overrun error occurs, RDR3 retains the receive data it held before the overrun error occurred, and data received after the error is lost. Reception cannot be continued with the OER bit set to 1, and in clock-synchronous mode, transmission cannot be continued either.

Note: * Only 0 can be written to clear the flag.

- RDR3 Receive Data Register 3 Address: H'FF9D

Bit	Bit Name	Set Value	R/W	Description
7	Bit 7	Undefined	R	RDR3 is an 8-bit register that stores receive data. When one frame of data has been received, it is transferred from RSR3 to this register, enabling RSR3 to receive the next frame of data. RSR3 and RDR3 have a double-buffered structure, so continuous reception is possible. Read RDR3 only once, after confirming that the RDRF bit in SSR3 is set to 1. RDR3 cannot be written by the CPU. The initial value of RDR3 is H'00. RDR3 is initialized to H'00 by a reset or in the standby mode, watch mode, or module standby mode.
6	Bit 6	Undefined	R	
5	Bit 5	Undefined	R	
4	Bit 4	Undefined	R	
3	Bit 3	Undefined	R	
2	Bit 2	Undefined	R	
1	Bit 1	Undefined	R	
0	Bit 0	Undefined	R	

3. Flowchart



4.4.4 stop_sci3() Function

1. Module Specifications

- Ends the clock-synchronous mode

Table 8 Module Specifications

Item	Type	Variable	Description
Arguments	None	None	None

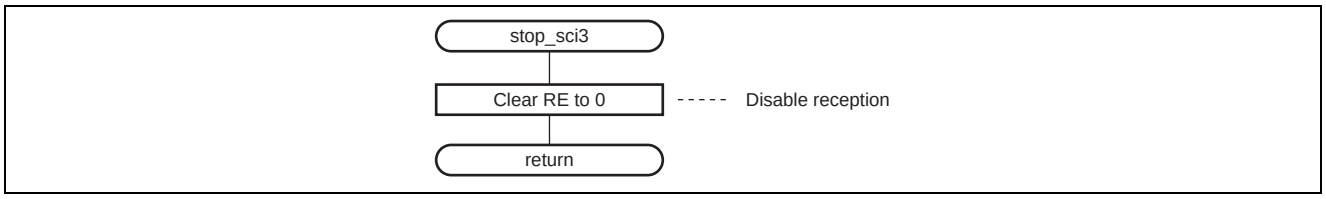
2. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- SCR3 Serial Control Register 3 Address: H'FF9A

Bit	Bit Name	Set Value	R/W	Description
4	RE	0	R/W	Receive Enable Reception is enabled when this bit is set to 1. In this state serial data reception is started when serial clock input is detected in clock-synchronous mode. Be sure to carry out SMR3 settings to decide the reception format before setting the RE bit to 1. Note that the RDRF, FER, PER, and OER flags in SSR3 are not affected when the RE bit is cleared to 0, and retain their previous state.

3. Flowchart



4.5 Link Address Specifications

Section Name	Address
CVECT	H'0000
P	H'0100
B	H'F780

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Mar.18.05	—	First edition issued

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