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H8/300H SLP Series

Pulse Cycle Measurement Using TPU Input Capture Function

Introduction

The input capture function of the 16-bit timer pulse unit (TPU) is used to measure the time (cycle) from the rising edge of a pulse input from an input capture input pin (TIOCA1) to the next rising edge.

Target Device

H8/38076R

Contents

1. Specifications

- The input capture function of the 16-bit timer pulse unit (TPU) is used to measure the cycle of a pulse input from an input capture input pin (TIOCA1).
- In this sample task, internal clock ϕ/256 is set as the timer counter_1 (TCNT_1) input clock. At ϕ = 10 MHz operation, the resolution is 25.6 µs and the measurable cycle is 1.67 s. The TCNT_1 count value from the rising edge of a TIOCA1 input pulse to the next rising edge is stored in RAM.
- An example of pulse cycle measurement by means of the input capture function is shown in figure 1.

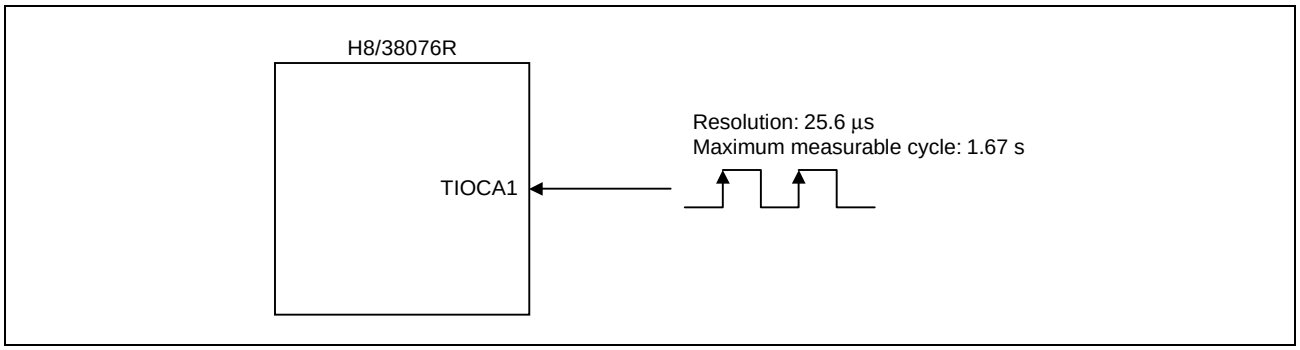


Figure 1 Example of Pulse Cycle Measurement Using TPU Input Capture Function

2. Functions Used

2.1 TPU Input Capture Function

In this sample task, the input capture function of the TPU is used to measure the cycle of a pulse input to an input capture input pin (TIOCA1). A block diagram of the input capture function of the TPU is shown in figure 2. The block diagram of the input capture function of the TPU is explained below.

- Timer control register_1 (TCR_1)

  Selects timer counter_1 (TCNT_1) counter clearing source, the input clock edge, and the clock source.
- Timer mode register_1 (TMDR_1)

  Sets the operating mode of channel 1.
- Timer I/O control register_1 (TIOR_1)

  Controls timer general register A_1 (TGRA_1).
- Timer interrupt enable register_1 (TIER_1)

  Enables or disables TPU_1 interrupt requests.
- Timer status register_1 (TSR_1)

  Indicates the state of TPU_1.
- Timer counter_1 (TCNT_1)

  A 16-bit readable/writable counter that counts using the rising edge of internal clock ϕ/256
- Timer general register A_1 (TGRA_1)

  A 16-bit readable/writable input capture register

- Timer start register (TSTR)

  Controls operation/stopping of timer counter_1 (TCNT_1).

- An example of input capture input cycle calculation is shown below. (In this sample task, the TCNT_1 count value is stored in RAM.)

  (ϕ = 10 MHz, TCNT_1 input clock = ϕ/256)

  TIOCA1 pin input pulse cycle = TCNT_1 count value × TCNT_1 input clock cycle
  = TCNT_1 count value × 25.6 µs

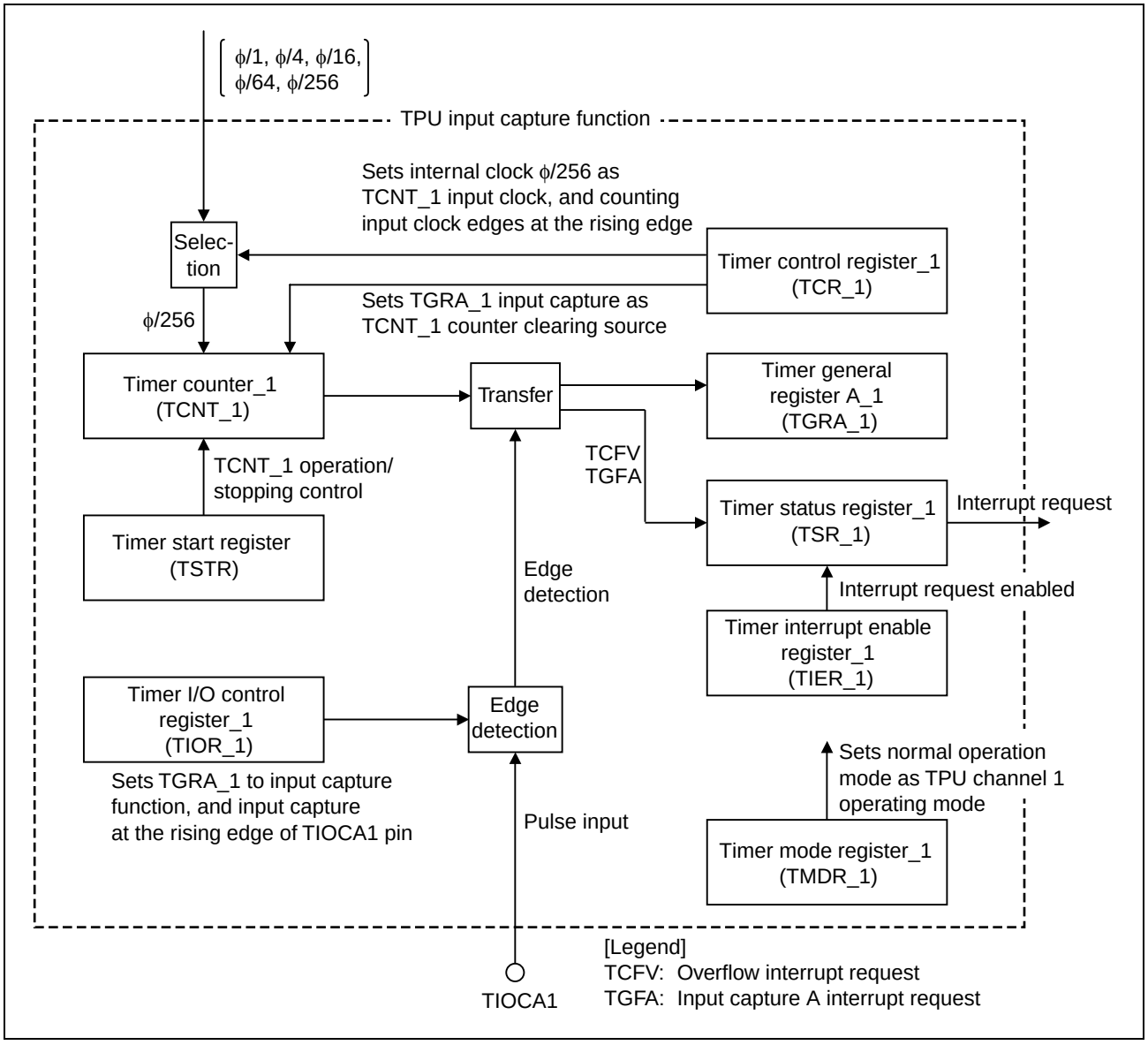


Figure 2 Block Diagram of TPU Input Capture Function

2.2 Assignment of Functions

Table 1 shows the assignment of functions in this sample task. Using functions assigned as shown in table 1, the cycle of a pulse input from an input capture input pin (TIOCA1) is measured by means of the TPU input capture function.

Table 1 Assignment of Functions

Elements	Description
TCR_1	Sets TGRA_1 compare match as TCNT_1 counter clearing source, rising edge as input clock edge, and internal clock ϕ/256 as clock source
TMDR_1	Sets normal operation mode as TPU channel 1 operating mode
TIOR_1	Sets input capture register as TGRA_1 function, and input capture at the rising edge as TIOCA1 pin function
TIER_1	Enables TCFV and TGFA interrupts
TSR_1	TCFV, TGFA interrupt request flags
TCNT_1	16-bit counter using internal clock ϕ/256 as clock source
TGRA_1	16-bit input capture register
TSTR	Sets TCNT_1 count operation
TIOCA1	TGRA_1 input capture input pin

3. Principles of Operation

The principles of operation of this sample task are illustrated in figure 3. Using the hardware and software processing shown in figure 3, pulse cycles are measured using the input capture function of the TPU.

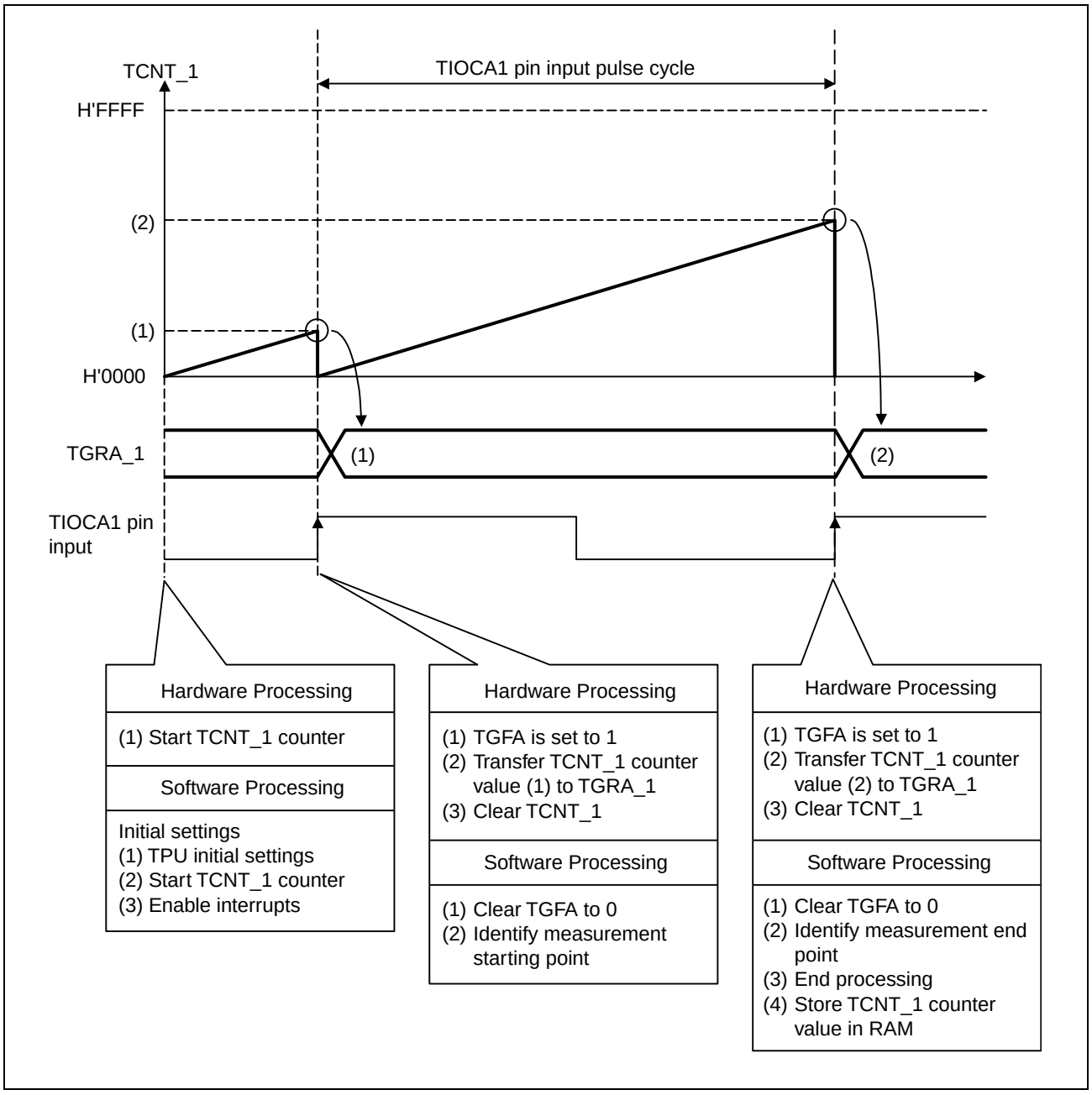


Figure 3 Principles of Operation

4. Description of Software

4.1 Modules

Table 2 shows the modules used in this sample task.

Table 2 Modules

Function Name	Description
main	TPU initial settings, TCNT_1 count operation start, interrupt enabling, storing TCNT_1 value in RAM at end of measurement, end processing
int_tgi1a	TGRA_1 input capture A interrupt processing, measurement starting point/end point identification
int_tci1v	TCNT_1 overflow interrupt processing

4.2 Arguments

No arguments are used in this sample task.

4.3 Internal Registers Used

The internal registers used in this sample task are shown below.

- TSTR Timer start register Address: H'F030

Bit	Bit Name	Set Value	R/W	Description
1	CST1	1	R/W	Counter start 1 Selects TCNT_1 operation or stopping. CST1 = 1: TCNT_1 performs count operation

- TCR_1 Timer control register_1 Address: H'F040

Bit	Bit Name	Set Value	R/W	Description
6	CCLR1	0	R/W	Counter clear 1, 0
5	CCLR0	1	R/W	Select the TCNT_1 counter clearing source. CCLR1 = 0, CCLR0 = 1: TCNT_1 cleared by TGRA_1 input capture
4	CKEG1	0	R/W	Clock edge 1, 0
3	CKEG0	0	R/W	Select the TCNT_1 input clock edge. CKEG1 = 0, CKEG0 = 0: Counts at the rising edge
2	TPSC2	1	R/W	Timer prescaler 2, 1, 0
1	TPSC1	1	R/W	Select the TCNT_1 clock source.
0	TPSC0	0	R/W	TPSC2 = 1, TPSC1 = 1, TPSC0 = 0: Counts on internal clock ϕ/256

- TMDR_1 Timer mode register_1 Address: H'F041

Bit	Bit Name	Set Value	R/W	Description
1	MD1	0	R/W	Mode 1, 0
0	MD0	0	R/W	Select the TPU_1 operating mode. MD1 = 0, MD0 = 0: TPU_1 set to normal operation mode

- TIOR_1 Timer I/O control register_1 Address: H'F042

Bit	Bit Name	Set Value	R/W	Description
3	IOA3	1	R/W	I/O control A3 to A0
2	IOA2	0	R/W	Select the function of TGRA_1.
1	IOA1	0	R/W	IOA3 = 1, IOA2 = 0, IOA1 = 0, IOA0 = 0: TGRA_1 function is input capture register, TIOCA1 pin function is input capture at the rising edge
0	IOA0	0	R/W	

- TIER_1 Timer interrupt enable register_1 Address: H'F044

Bit	Bit Name	Set Value	R/W	Description
4	TCIEV	1	R/W	Overflow interrupt enable Enables or disables TCFV flag interrupt request (TCI1V) when TCFV flag is set to 1 in TSR_1. TCIEV = 1: TCFV flag interrupt request (TCI1V) enabled
0	TGIEA	1	R/W	TGR interrupt enable A Enables or disables TGFA flag interrupt request (TGI1A) when TGFA flag is set to 1 in TSR. TGIEA = 1: TGFA flag interrupt request (TGI1A) enabled

- TSR_1 Timer status register_1 Address: H'F045

Bit	Bit Name	Set Value	R/W	Description
4	TCFV	0	R/(W)*	Overflow flag Status flag indicating occurrence of TCNT_1 overflow [Setting condition] When TCNT_1 value overflows (H'FFFF → H'0000) [Clearing condition] When 0 is written to TCFV after TCFV is read while set to 1
0	TGFA	0	R/(W)*	Input capture/output compare flag A Status flag indicating occurrence of TGRA_1 input capture or compare match [Setting conditions] • When TCNT_1 = TGRA_1 while TGRA_1 is functioning as output compare register • When TCNT_1 value is transferred to TGRA_1 in response to input capture signal when TGRA_1 is functioning as input capture register [Clearing condition] • When 0 is written to TGFA after TGFA is read while set to 1

Note: * Only 0 can be written to clear the flag.

- TCNT_1 Timer counter_1 Address: H'F046

Bit	Bit Name	Set Value	R/W	Description
15	Bit 15	0	R/W	Timer counter_1 16-bit readable/writable counter. TCNT_1 is initialized to H'0000 at a reset. TCNT_1 cannot be accessed in 8-bit units, and must always be accessed in 16-bit units.
14	Bit 14	0	R/W	
13	Bit 13	0	R/W	
12	Bit 12	0	R/W	
11	Bit 11	0	R/W	
10	Bit 10	0	R/W	
9	Bit 9	0	R/W	
8	Bit 8	0	R/W	
7	Bit 7	0	R/W	
6	Bit 6	0	R/W	
5	Bit 5	0	R/W	
4	Bit 4	0	R/W	
3	Bit 3	0	R/W	
2	Bit 2	0	R/W	
1	Bit 1	0	R/W	
0	Bit 0	0	R/W	

- TGRA_1 Timer general register A_1 Address: H'F048

Bit	Bit Name	Set Value	R/W	Description
15	Bit 15	—	R/W	Timer general register A_1
14	Bit 14	—	R/W	A 16-bit readable/writable register, functioning as either output compare or input capture register. TGRA_1 is initialized to H'FFFF at a reset. TGRA_1 cannot be accessed in 8-bit units, and must always be accessed in 16-bit units.
13	Bit 13	—	R/W	
12	Bit 12	—	R/W	
11	Bit 11	—	R/W	
10	Bit 10	—	R/W	
9	Bit 9	—	R/W	
8	Bit 8	—	R/W	
7	Bit 7	—	R/W	
6	Bit 6	—	R/W	
5	Bit 5	—	R/W	
4	Bit 4	—	R/W	
3	Bit 3	—	R/W	
2	Bit 2	—	R/W	
1	Bit 1	—	R/W	
0	Bit 0	—	R/W	

4.4 Constants Used

No constants are used in this sample task.

4.5 RAM Usage

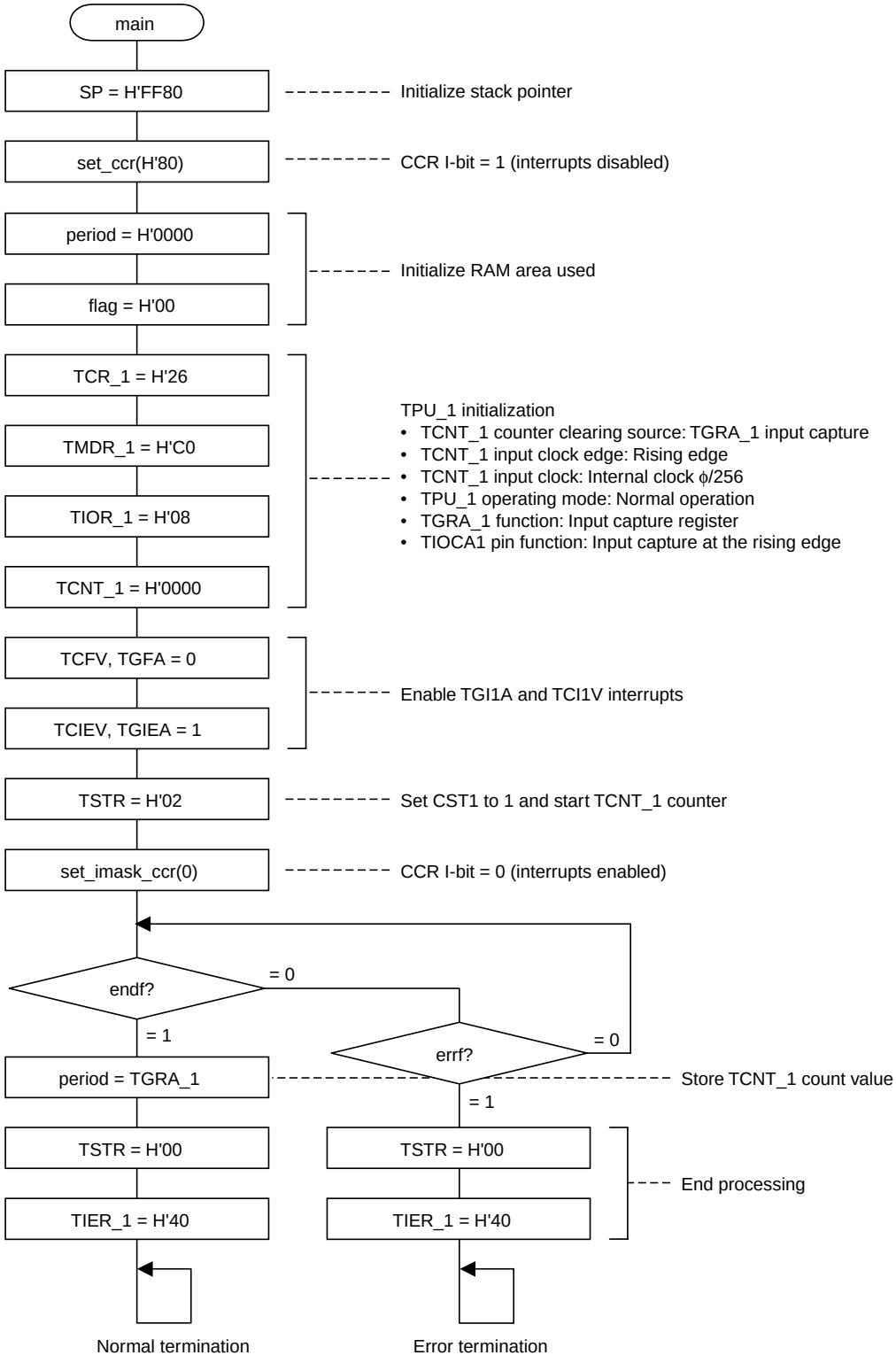
Table 3 describes RAM usage in this sample task.

Table 3 RAM Usage

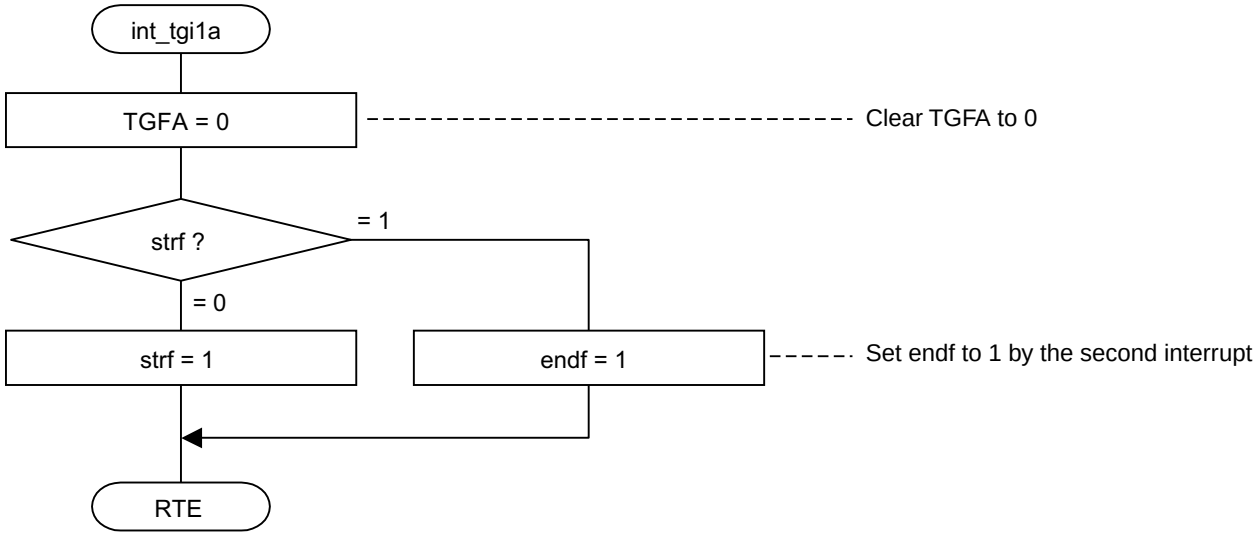
Label		Description	Amount of Memory Used	Used in
period		Stores TCNT_1 value from rising edge of TIOCA1 pin input pulse to next rising edge.	1 word	main
flag	endf	Flag indicating end of measurement	1 bit	main, int_tgi1a
	strf	Flag indicating start of measurement	1 bit	int_tci1v
	errf	Flag indicating that TCNT_1 has overflowed	1 bit	main, int_tci1v

5. Flowcharts

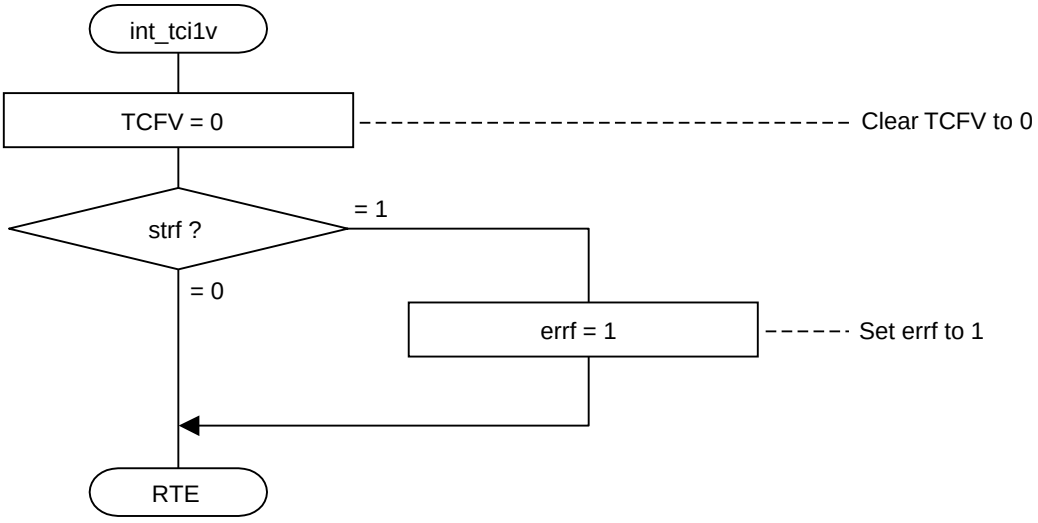
5.1 main



5.2 int_tgi1a



5.3 int_tci1v



- Link Address Specifications

Section Name	Address
CV1	H'0000
CV2	H'003A
CV3	H'003E
P	H'0100
B	H'F780

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Sep.16.04	—	First edition issued

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