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H8/300H SLP Series

Pulse Cycle Measurement Using TPU Cascaded Operation Function

Introduction

Two 16-bit timer counter channels of the 16-bit timer pulse unit (TPU) are connected and operated as a 32-bit timer counter, and the time (cycle) from the rising edge of a pulse input simultaneously to input capture input pins (TIOCA1, TIOCA2) to the next rising edge is measured.

Target Device

H8/38076R

Contents

1. Specifications

- The cascaded operation function of the 16-bit timer pulse unit (TPU) is used to measure the time (cycle) from the rising edge of a pulse input simultaneously to the TGRA_1 input capture input pin (TIOCA1) and TGRA_2 input capture input pin (TIOCA2) to the next rising edge.
- Cascaded operation is a function for connecting two 16-bit counter channels and operating them as a 32-bit counter.
- By inputting a rising edge simultaneously to the TIOCA1 pin and TIOCA2 pin, a 32-bit counter value is transferred, the upper 16 bits being transferred to timer general register A_1 (TGRA_1) and the lower 16 bits to timer general register A_2 (TGRA_2).
- In this sample task, internal clock ϕ is set as the input clock of the 32-bit timer counter. At ϕ = 10 MHz operation, the resolution is 100 ns and the measurable cycle is 429.49 s. The captured 32-bit counter value is stored in RAM.
- An example of pulse cycle measurement by means of the TPU cascaded operation function is shown in figure 1.

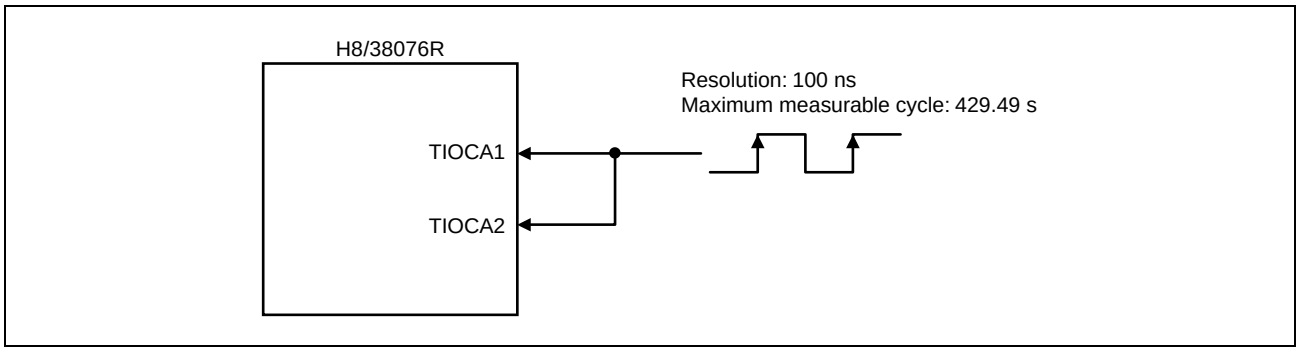


Figure 1 Example of Pulse Cycle Measurement Using TPU Cascaded Operation Function

2. Functions Used

2.1 TPU Cascaded Operation Function

In this sample task, the cascaded operation function of the TPU is used to measure the cycle of a pulse input simultaneously to the TIOCA1 pin and TIOCA2 pin. A block diagram of the cascaded operation function of the TPU is shown in figure 2. The block diagram of the cascaded operation function of the TPU is explained below.

- System clock (ϕ)

  10-MHz clock used as the reference clock for operating the CPU and peripheral function modules
- Timer control register_1 (TCR_1), timer control register_2 (TCR_2)

  These registers select timer counter_1 (TCNT_1), timer counter_2 (TCNT_2) counter clearing source. input clock edge, and clock source.
- Timer mode register_1 (TMDR_1), timer mode register_2 (TMDR_2)

  These registers set the operating modes of channels 1 and 2.
- Timer I/O control register_1 (TIOR_1), timer I/O control register_2 (TIOR_2)

  These registers control timer general register A_1 (TGRA_1) and timer general register A_2 (TGRA_2).
- Timer interrupt enable register_1 (TIER_1)

  Enables or disables of channel 1 interrupt requests.

- Timer status register_1 (TSR_1)

  Indicates the state of channel 1.

- Timer counter_1 (TCNT_1)

  A 16-bit readable/writable counter that operates as the upper 16 bits of a 32-bit timer counter. Counts on overflow of TCNT_2.

- Timer counter_2 (TCNT_2)

  A 16-bit readable/writable counter that operates as the lower 16 bits of a 32-bit timer counter. Counts at the rising edge of internal clock ϕ.

- Timer general register A_1 (TGRA_1)

  A 16-bit readable/writable input capture register that stores the upper 16-bit counter value (TCNT_1 counter value) of the 32-bit timer counter at the rising edge of a pulse input to the TIOCA1 pin

- Timer general register A_2 (TGRA_2)

  A 16-bit readable/writable input capture register that stores the lower 16-bit counter value (TCNT_2 counter value) of the 32-bit timer counter at the rising edge of a pulse input to the TIOCA2 pin

- Timer start register (TSTR)

  Controls operation/stopping of timer counter_1 (TCNT_1) and timer counter_2 (TCNT_2).

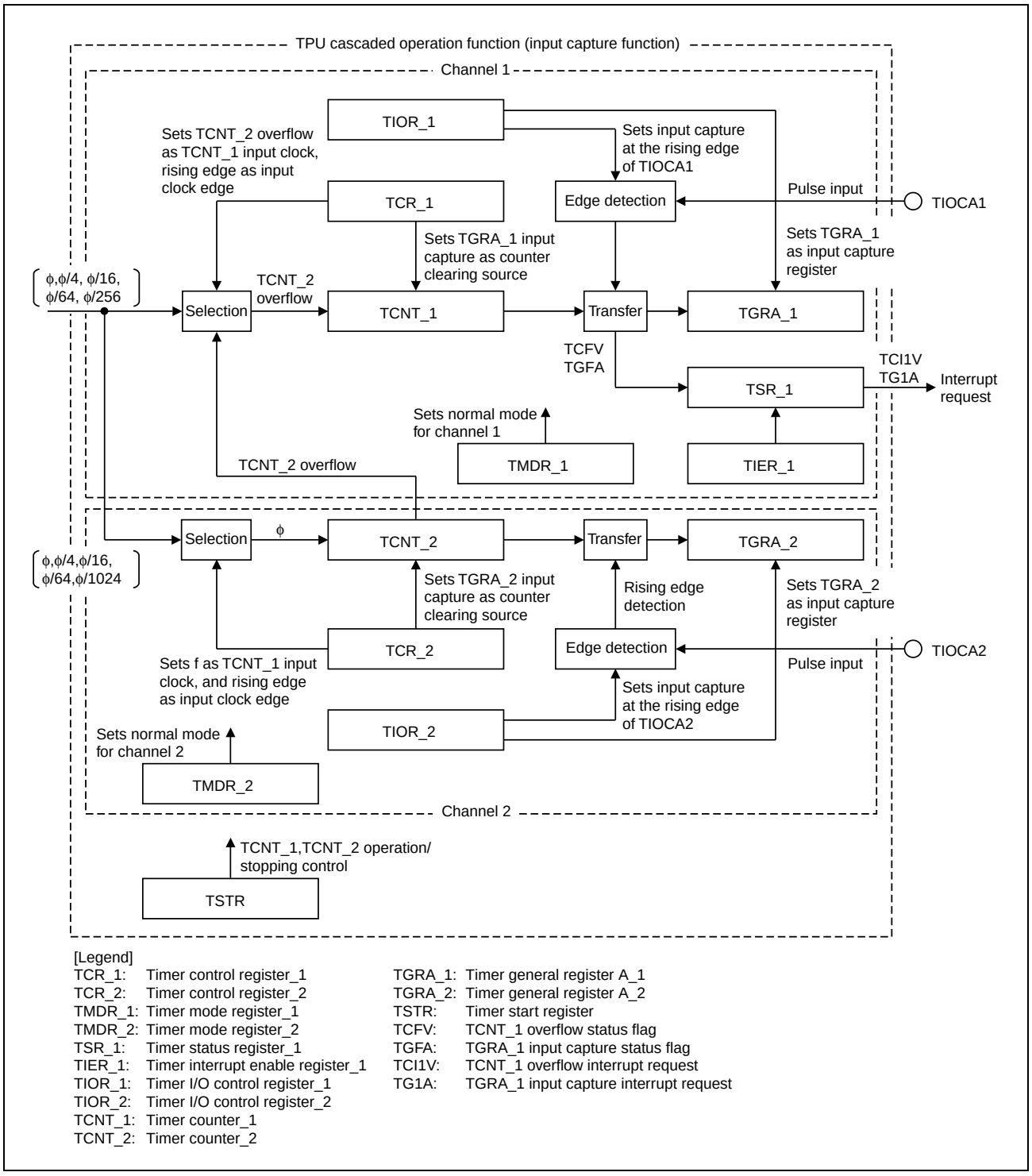
- An example of input capture input cycle calculation is shown below. (In this sample task, the count value of the 32-bit timer counter is stored in RAM.)

  (ϕ = 10 MHz, 32-bit timer counter input clock = ϕ)

  TIOCA1, TIOCA2 pin input pulse cycle

  = 32-bit timer counter value × 32-bit timer counter input clock

  = ([TCNT_1 (upper 16 bits)][TCNT_1 (lower 16 bits)]) × 100 ns



[Legend]

TCR_1:	Timer control register_1	TGRA_1:	Timer general register A_1
TCR_2:	Timer control register_2	TGRA_2:	Timer general register A_2
TMDR_1:	Timer mode register_1	TSTR:	Timer start register
TMDR_2:	Timer mode register_2	TCFV:	TCNT_1 overflow status flag
TSR_1:	Timer status register_1	TGFA:	TGRA_1 input capture status flag
TIER_1:	Timer interrupt enable register_1	TCI1V:	TCNT_1 overflow interrupt request
TIOR_1:	Timer I/O control register_1	TG1A:	TGRA_1 input capture interrupt request
TIOR_2:	Timer I/O control register_2		
TCNT_1:	Timer counter_1		
TCNT_2:	Timer counter_2		

Figure 2 Block Diagram of Cascaded Operation Function

2.2 Assignment of Functions

Table 1 shows the assignment of functions in this sample task. Using functions assigned as shown in table 1, pulse cycles are measured by using the cascaded operation function of the TPU.

Table 1 Assignment of Functions

Elements	Description
TCR_1	Sets TGRA_1 input capture as TCNT_1 counter clearing source, rising edge as TCNT_1 input clock edge, and TCNT_2 overflow as TCNT_1 counter clock
TCR_2	Sets TGRA_2 input capture as TCNT_2 counter clearing source, rising edge as TCNT_2 input clock edge, and internal clock ϕ as TCNT_2 counter clock
TMDR_1	Sets normal mode as channel 1 operating mode
TMDR_2	Sets normal mode as channel 2 operating mode
TIOR_1	Sets input capture register as TGRA_1 function, and input capture at the rising edge as TIOCA1 pin function
TIOR_2	Sets input capture register as TGRA_2 function, and input capture at the rising edge as TIOCA2 pin function
TIER_1	Enables TCNT_1 overflow interrupt request and TGRA_1 input capture interrupt request
TSR_1	Indicates TCNT_1 overflow and TGRA_1 input capture status
TCNT_1	Upper 16 bits of 32-bit timer counter
TCNT_2	Lower 16 bits of 32-bit timer counter
TGRA_1	Input capture register that stores upper 16 bits of 32-bit timer counter
TGRA_2	Input capture register that stores lower 16 bits of 32-bit timer counter
TSTR	Controls operation/stopping of TCNT_1 and TCNT_2
TIOCA1	TGRA_1 input capture input pin, used to input cycle measurement pulse
TIOCA2	TGRA_2 input capture input pin, used to input cycle measurement pulse

3. Principles of Operation

The principles of operation of this sample task are illustrated in figure 3. Using the hardware and software processing shown in figure 3, PWM output is performed by means of the TPU synchronous operation function.

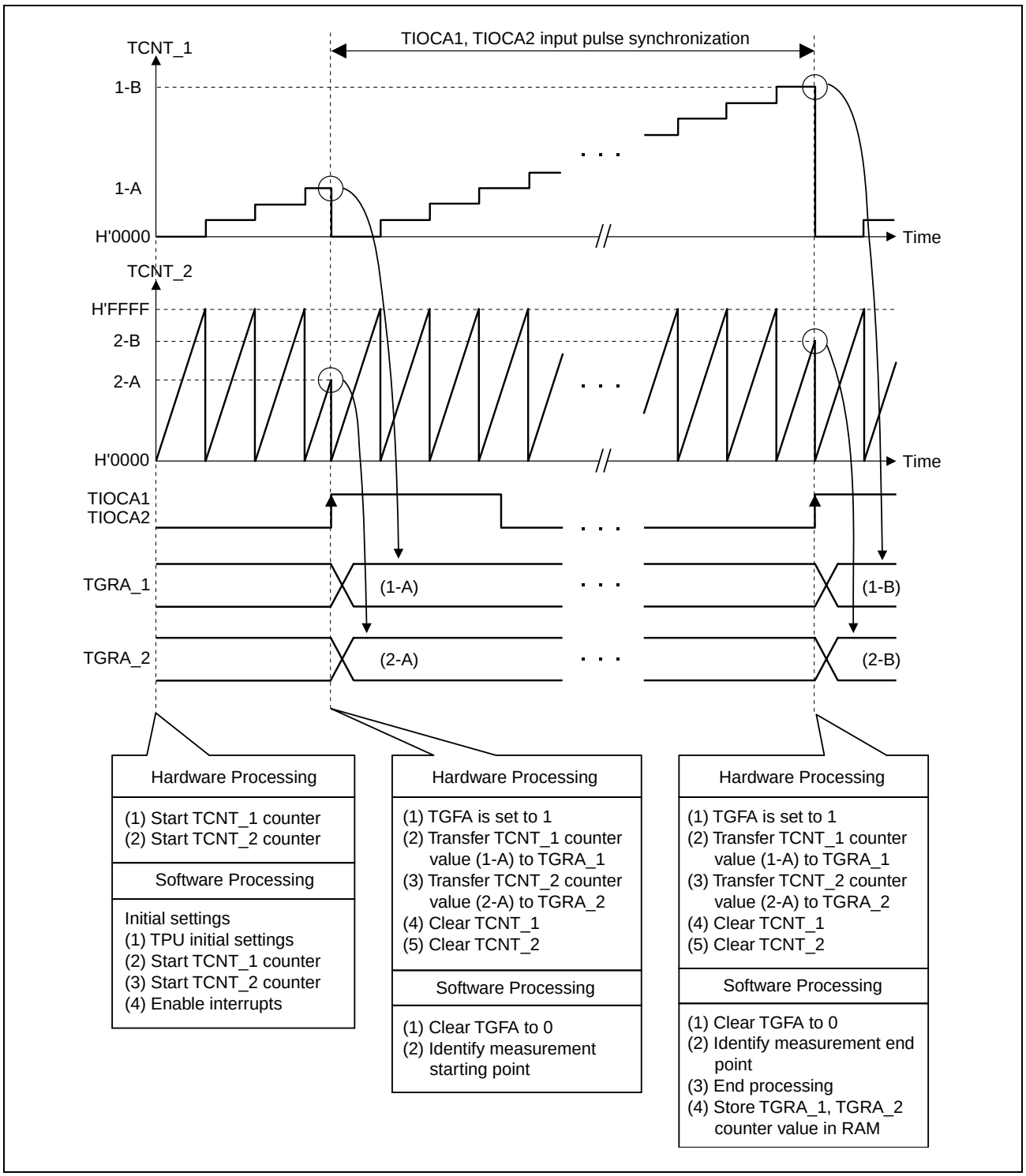


Figure 3 Principles of Operation

4. Description of Software

4.1 Modules

Table 2 shows the modules used in this sample task.

Table 2 Modules

Function Name	Description
main	TPU initial settings, TCNT_1 and TCNT_2 count operation start, interrupt enabling, storing 32-bit timer counter value in RAM at end of measurement, end processing
int_tg1a	TGRA_1 input capture A interrupt processing, measurement starting point/end point identification
int_tci1v	TCNT_1 overflow interrupt processing, measurement error identification

4.2 Arguments

No arguments are used in this sample task.

4.3 Internal Registers Used

The internal registers used in this sample task are shown below.

- TSTR Timer start register Address: H'F030

Bit	Bit Name	Set Value	R/W	Description
2	CST2	1	R/W	Counter start 2 Selects TCNT_2 operation or stopping. CST2 = 1: TCNT_2 performs count operation
1	CST1	1	R/W	Counter start 1 Selects TCNT_1 operation or stopping. CST1 = 1: TCNT_1 performs count operation

- TCR_1 Timer control register_1 Address: H'F040

Bit	Bit Name	Set Value	R/W	Description
6	CCLR1	0	R/W	Counter clear 1, 0
5	CCLR0	1	R/W	Select the TCNT_1 counter clearing source. CCLR1 = 0, CCLR0 = 1: TCNT_1 cleared by TGRA_1 input capture
4	CKEG1	0	R/W	Clock edge 1, 0
3	CKEG0	0	R/W	Select the TCNT_1 input clock edge. CKEG1 = 0, CKEG0 = 0: Counts at the rising edge
2	TPSC2	1	R/W	Timer prescaler 2, 1, 0
1	TPSC1	1	R/W	Select the TCNT_1 clock source.
0	TPSC0	1	R/W	TPSC2 = 1, TPSC1 = 1, TPSC0 = 1: Counts on TCNT_2 overflow

- TMDR_1 Timer mode register_1 Address: H'F041

Bit	Bit Name	Set Value	R/W	Description
1	MD1	0	R/W	Mode 1, 0
0	MD0	0	R/W	Select the TPU_1 operating mode. MD1 = 0, MD0 = 0: TPU_1 set to normal operation mode

- TIOR_1 Timer I/O control register_1 Address: H'F042

Bit	Bit Name	Set Value	R/W	Description
3	IOA3	1	R/W	I/O control A3 to A0
2	IOA2	0	R/W	Select the function of TGRA_1.
1	IOA1	0	R/W	IOA3 = 1, IOA2 = 0, IOA1 = 0, IOA0 = 0: TGRA_1 function is input capture register, input capture at the rising edge of TIOCA1 pin
0	IOA0	0	R/W	

- TIER_1 Timer interrupt enable register_1 Address: H'F044

Bit	Bit Name	Set Value	R/W	Description
4	TCIEV	1	R/W	Overflow interrupt enable Enables or disables TCFV flag interrupt request (TCIV) when TCFV flag is set to 1 in TSR_1. TCIEV = 1: TCFV flag interrupt request (TCIV) enabled
0	TGIEA	1	R/W	TGR interrupt enable A Enables or disables TGFA flag interrupt request (TGIA) when TGFA flag is set to 1 in TSR_1. TGIEA = 1: TGFA flag interrupt request (TGIA) enabled

- TSR_1 Timer status register_1 Address: H'F045

Bit	Bit Name	Set Value	R/W	Description
4	TCFV	0	R/(W)*	Overflow flag Status flag indicating occurrence of TCNT_1 overflow [Setting condition] When TCNT_1 value overflows (H'FFFF → H'0000) [Clearing condition] When 0 is written to TCFV after TCFV is read while set to 1
0	TGFA	0	R/(W)*	Input capture flag A Status flag indicating occurrence of TGRA_1 input capture [Setting condition] When TCNT_1 value is transferred to TGRA_1 in response to input capture signal [Clearing condition] When 0 is written to TGFA after TGFA is read while set to 1

Note: * Only 0 can be written to clear the flag.

- TCNT_1 Timer counter_1 Address: H'F046

Bit	Bit Name	Set Value	R/W	Description
15	Bit 15	0	R/W	Timer counter_1
14	Bit 14	0	R/W	16-bit readable/writable counter. TCNT_1 is initialized to H'0000 at a reset. TCNT_1 cannot be accessed in 8-bit units, and must always be accessed in 16-bit units.
13	Bit 13	0	R/W	
12	Bit 12	0	R/W	In cascaded operation, TCNT_1 functions as the upper 16 bits of the 32-bit timer counter.
11	Bit 11	0	R/W	
10	Bit 10	0	R/W	
9	Bit 9	0	R/W	
8	Bit 8	0	R/W	
7	Bit 7	0	R/W	
6	Bit 6	0	R/W	
5	Bit 5	0	R/W	
4	Bit 4	0	R/W	
3	Bit 3	0	R/W	
2	Bit 2	0	R/W	
1	Bit 1	0	R/W	
0	Bit 0	0	R/W	

- TGRA_1 Timer general register A_1 Address: H'F048

Bit	Bit Name	Set Value	R/W	Description
15	Bit 15	—	R/W	Timer general register A_1
14	Bit 14	—	R/W	A 16-bit readable/writable register, functioning as either output compare or input capture register. TGRA_1 is initialized to H'FFFF at a reset. TGRA_1 cannot be accessed in 8-bit units, and must always be accessed in 16-bit units.
13	Bit 13	—	R/W	
12	Bit 12	—	R/W	
11	Bit 11	—	R/W	In cascaded operation, TGRA_1 stores the upper 16 bits (TCNT_1 value) of the 32-bit timer counter at the rising edge of a pulse input to the TIOCA1 pin
10	Bit 10	—	R/W	
9	Bit 9	—	R/W	
8	Bit 8	—	R/W	
7	Bit 7	—	R/W	
6	Bit 6	—	R/W	
5	Bit 5	—	R/W	
4	Bit 4	—	R/W	
3	Bit 3	—	R/W	
2	Bit 2	—	R/W	
1	Bit 1	—	R/W	
0	Bit 0	—	R/W	

- TCR_2 Timer control register_2 Address: H'F050

Bit	Bit Name	Set Value	R/W	Description
6	CCLR1	0	R/W	Counter clear 1, 0
5	CCLR0	1	R/W	Select the TCNT_2 counter clearing source. CCLR1 = 0, CCLR0 = 1: TCNT_2 cleared by TGRA_2 input capture
4	CKEG1	0	R/W	Clock edge 1, 0
3	CKEG0	0	R/W	Select the TCNT_2 input clock edge. CKEG1 = 0, CKEG0 = 0: Counts at the rising edge
2	TPSC2	0	R/W	Timer prescaler 2, 1, 0
1	TPSC1	0	R/W	Select the TCNT_2 clock source.
0	TPSC0	0	R/W	TPSC2 = 0, TPSC1 = 0, TPSC0 = 0: Counts on internal clock ϕ

- TMDR_2 Timer mode register_2 Address: H'F051

Bit	Bit Name	Set Value	R/W	Description
1	MD1	0	R/W	Mode 1, 0
0	MD0	0	R/W	Select the TPU_2 operating mode. MD1 = 0, MD0 = 0: TPU_2 set to normal operation mode

- TIOR_2 Timer I/O control register_2 Address: H'F052

Bit	Bit Name	Set Value	R/W	Description
3	IOA3	1	R/W	I/O control A3 to A0
2	IOA2	x	R/W	Select the function of TGRA_2.
1	IOA1	0	R/W	IOA3 = 1, IOA2 = x, IOA1 = 0, IOA0 = 0: TGRA_2 function is input capture register, input capture at the rising edge of TIOCA2 pin
0	IOA0	0	R/W	

x: Don't care

- TCNT_2 Timer counter_2 Address: H'F056

Bit	Bit Name	Set Value	R/W	Description
15	Bit 15	0	R/W	Timer counter_2
14	Bit 14	0	R/W	16-bit readable/writable counter. TCNT_2 is initialized to H'0000 at a reset. TCNT_2 cannot be accessed in 8-bit units, and must always be accessed in 16-bit units.
13	Bit 13	0	R/W	
12	Bit 12	0	R/W	In cascaded operation, TCNT_2 functions as the lower 16 bits of the 32-bit timer counter.
11	Bit 11	0	R/W	
10	Bit 10	0	R/W	
9	Bit 9	0	R/W	
8	Bit 8	0	R/W	
7	Bit 7	0	R/W	
6	Bit 6	0	R/W	
5	Bit 5	0	R/W	
4	Bit 4	0	R/W	
3	Bit 3	0	R/W	
2	Bit 2	0	R/W	
1	Bit 1	0	R/W	
0	Bit 0	0	R/W	

- TGRA_2 Timer general register A_2 Address: H'F058

Bit	Bit Name	Set Value	R/W	Description
15	Bit 15	—	R/W	Timer general register A_2
14	Bit 14	—	R/W	A 16-bit readable/writable register, functioning as either output compare or input capture register. TGRA_2 is initialized to H'FFFF at a reset. TGRA_2 cannot be accessed in 8-bit units, and must always be accessed in 16-bit units.
13	Bit 13	—	R/W	
12	Bit 12	—	R/W	
11	Bit 11	—	R/W	In cascaded operation, TGRA_2 stores the lower 16-bit (TCNT_2) value of the 32-bit timer counter at the rising edge of a pulse input to the TIOCA2 pin.
10	Bit 10	—	R/W	
9	Bit 9	—	R/W	
8	Bit 8	—	R/W	
7	Bit 7	—	R/W	
6	Bit 6	—	R/W	
5	Bit 5	—	R/W	
4	Bit 4	—	R/W	
3	Bit 3	—	R/W	
2	Bit 2	—	R/W	
1	Bit 1	—	R/W	
0	Bit 0	—	R/W	

4.4 Constants Used

No constants are used in this sample task.

4.5 RAM Usage

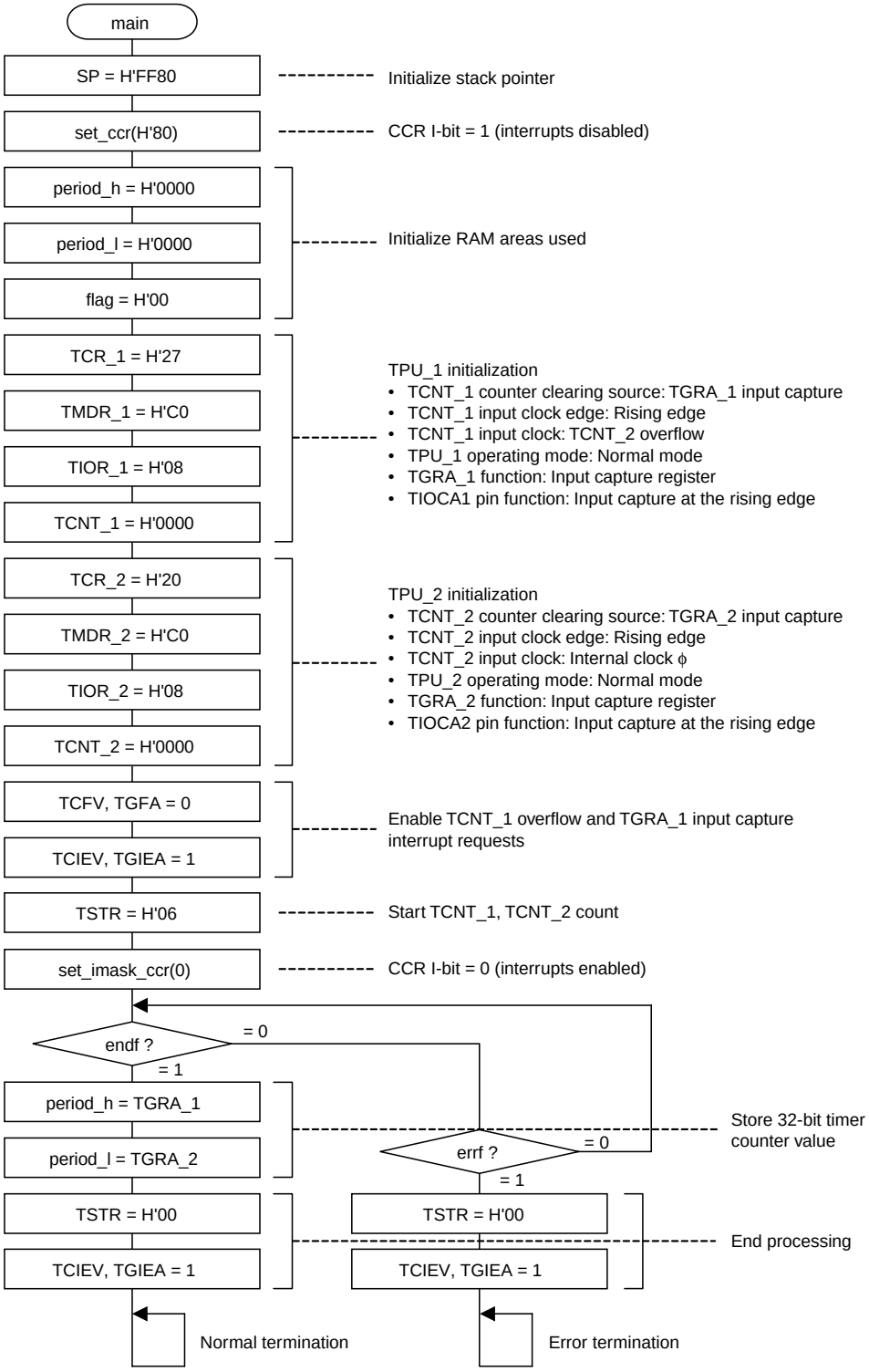
Table 3 describes RAM usage in this sample task.

Table 3 RAM Usage

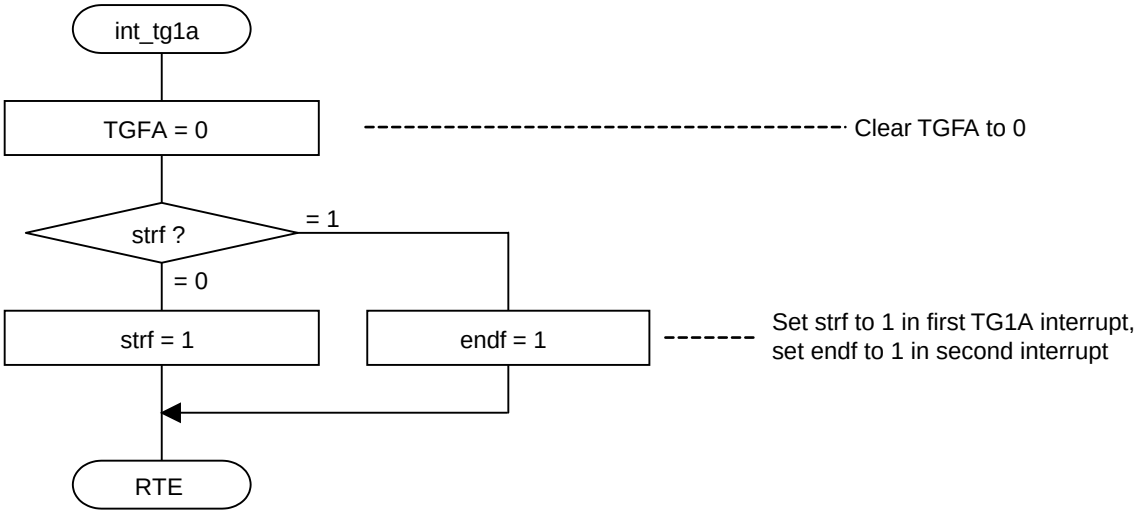
Label		Description	Amount of Memory Used	Used in
period_h		Stores upper 16 bits of 32-bit timer counter value from rising edge of TIOCA1 pin, TIOCA2 pin input pulse to next rising edge.	1 word	main
period_l		Stores lower 16 bits of 32-bit timer counter value from rising edge of TIOCA1 pin, TIOCA2 pin input pulse to next rising edge.	1 word	main
flag	endf	Flag indicating end of measurement	1 bit	main, int_tg1a
	strf	Flag indicating start of measurement	1 bit	int_tg1a, int_tci1v
	errf	Flag indicating that TCNT_1 has overflowed	1 bit	main, int_tci1v

5. Flowcharts

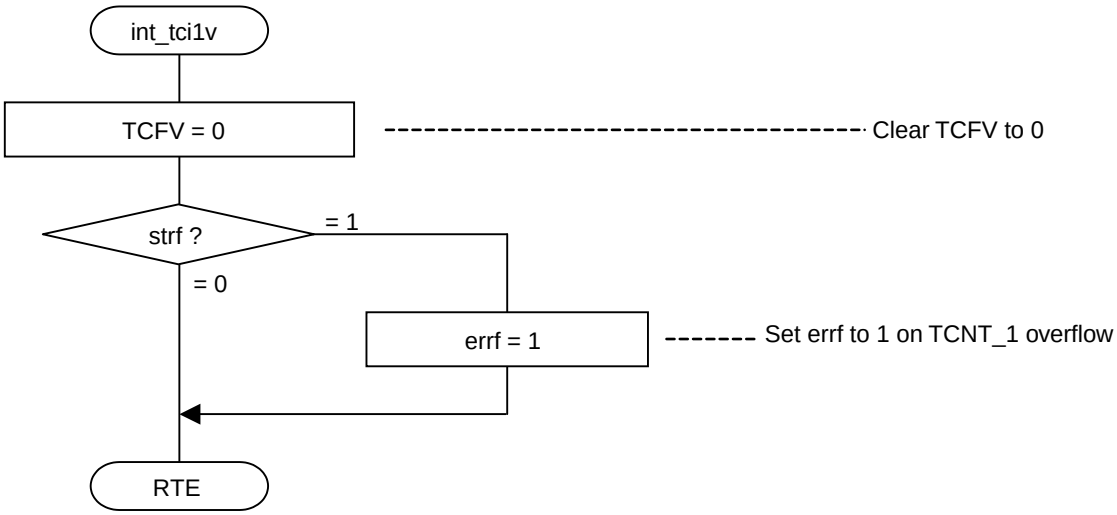
5.1 main



5.2 int_tg1a



5.3 int_tci1v



- Link Address Specifications

Section Name	Address
CV1	H'0000
CV2	H'003A
CV3	H'003E
P	H'0100
B	H'F780

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Sep.16.04	—	First edition issued

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