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April 1st, 2010
Renesas Electronics Corporation

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H8/300H SLP Series

Duty Pulse Output Using AEC Event Counter PWM Output Function

Introduction

Duty pulses are output using the event counter PWM output function of the asynchronous event counter (AEC).

Target Device

H8/38076R

Contents

1. Specifications

Duty pulses are output using the event counter PWM output function of the AEC, as shown in figure 1.

- A standard PWM waveform is output from the PWM1 output pin by means of the AEC event counter PWM function.
- This sample task outputs duty pulses with a pulse cycle of 12 ms, pulse high width of 9 ms, and duty cycle of 75%.

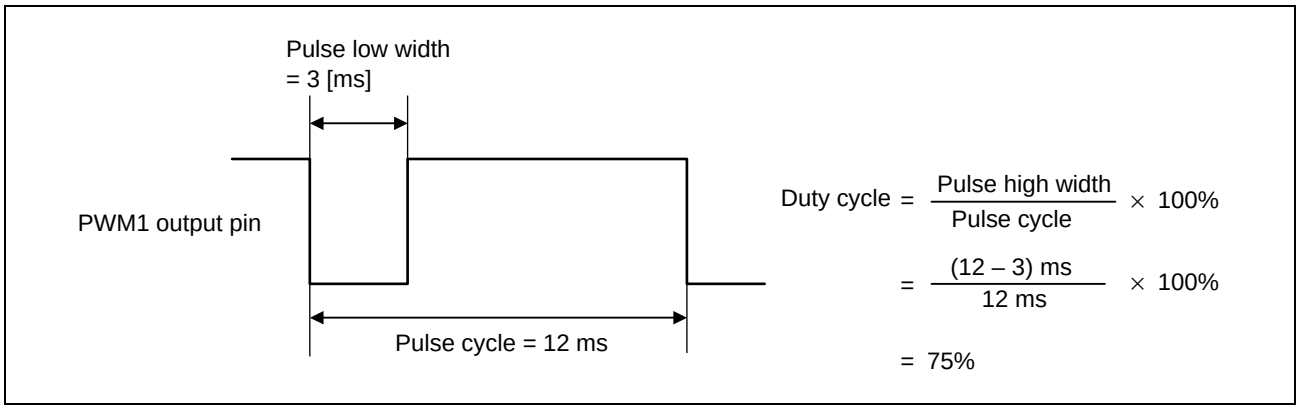


Figure 1 Duty Pulse Output Using Event Counter PWM Output Function of AEC

2. Functions Used

2.1 Functions

In this sample task, duty pulses are output using the event counter PWM output function of the AEC. A block diagram of the AEC is shown in figure 2. The block diagram of the event counter PWM output function of the AEC is explained below.

- System clock (ϕ)

  The reference clock for operating the CPU and peripheral functions (in this sample task, 10 MHz)
- Prescaler S (PSS)

  A 13-bit counter with ϕ as input, incremented every cycle
- Event counter PWM compare register (ECPWCR)

  ECPWCR sets the one conversion period of the event counter PWM waveform.
- Event counter PWM data register (ECPWDR)

  ECPWDR controls data of the event counter PWM waveform generator.
- Input pin edge select register (AEGSR)

  AEGSR enables or stops event counter PWM operation.
- Event counter control register (ECCR)

  ECCR controls counter input clock and IRQAEC/IECPWM.
- Event counter PWM output (IECPWM)

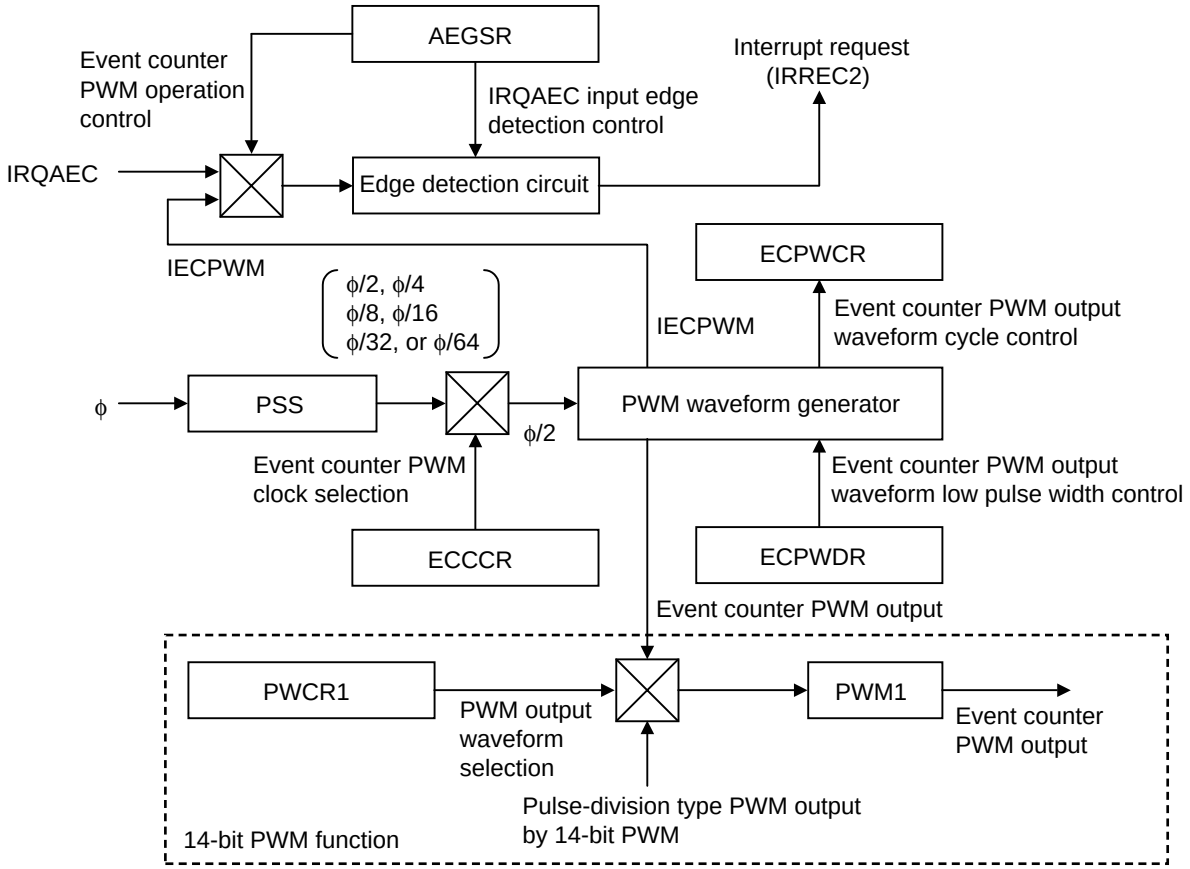
  IECPWM operates as an interrupt source. Interrupt enabling is controlled by IENEC2 in IENR1. When an IECPWM interrupt is generated, IRR1 interrupt request flag IRREC2 is set to 1. If IENEC2 is at this time, an interrupt request is issued to the CPU.
- Event input enable (IRQAEC)

  Interrupt input pin that enables event input. Not used in this sample task.
- PWM1 control register (PWCR1)

  Selects whether a PWM waveform output from the PWM1 output pin is a pulse division PWM waveform or AEC event counter PWM output.
- PWM1 output pin (PWM1)

  In this sample task, PWM1 outputs an AEC event counter PWM waveform.
- Port mode register 9 (PMR9)

  Sets the P90/PWM1 pin to PWM1 output.



[Legend]

ECPWCR:	Event counter PWM compare register	IRQAEC:	Event input enable
ECPWDR:	Event counter PWM data register	PWCR1:	PWM1 control register 1
AEGSR:	Input pin edge select register	PWM1:	PWM1 output pin
ECCR:	Event counter control register	IRREC2:	IRQAEC interrupt request
IECPWM:	Event counter PWM output		

Figure 2 Block Diagram of AEC Event Counter PWM Output Function

2.2 Assignment of Functions

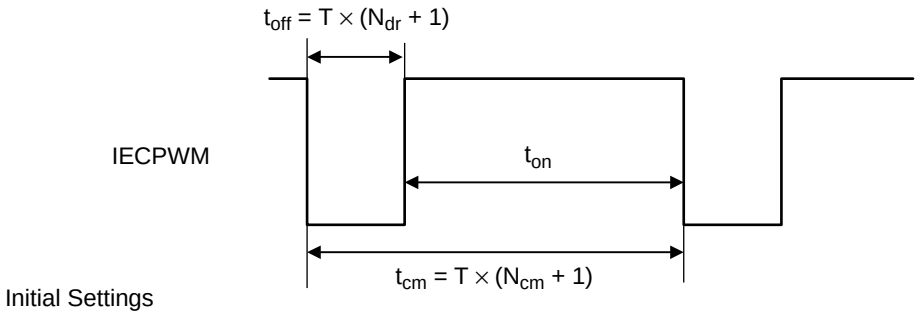
Table 1 shows the assignment of functions in this sample task. Using functions assigned as shown in table 1, duty pulses are output by using the AEC event counter PWM output function.

Table 1 Assignment of Functions

Elements	Description
ECPWCR	Sets event counter PWM output waveform conversion cycle to 12 ms.
ECPWDR	Sets IECPWM low-level periods to 3 ms.
ECCR	Selects ϕ/2 as event counter PWM clock.
AEGSR	Enables event counter PWM operation.
PWCR1	Sets standard PWM waveform as the waveform to be output from the PWM1 pin.
PWM1	Outputs event counter PWM waveform.
PMR9	Sets P90/PWM1 pin to be output from the PWM1 pin.

3. Principles of Operation

The principles of operation of this sample task are illustrated below. By means of the hardware and software processing shown in figure 3, duty pulses are output using the PWM function of the AEC.



Initial Settings

Hardware Processing
None
Software Processing
(1) Event counter PWM setting (2) PWM1 output pin setting (3) Enable interrupts

t_{on}: IECPWM high-level time
t_{off}: IECPWM low-level time
t_{cm}: One conversion period
T: Event counter PWM input clock cycle
N_{dr}: ECPWDR value
N_{cm}: ECPWCR value

Figure 3 Principles of Operation

4. Description of Software

4.1 Modules

Table 2 shows the modules used in this sample task.

Table 2 Modules

Function Name	Description
main	Event counter PWM setting, PWM1 output pin setting, enable interrupt

4.2 Arguments

No arguments are used in this sample task.

4.3 Internal Registers Used

The internal registers used in this sample task are shown below.

- ECPWCR Event counter PWM compare register Address: H'FF8C

  Function: ECPWCR sets one event counter PWM waveform conversion period.

  Set value: H'EA59

  R/W: R/W

- ECPWDR Event counter PWM data register Address: H'FF8E

  Function: ECPWDR controls event counter PWM waveform data.

  Set value: H'3A97

  R/W: W

- AEGSR Input pin edge select register Address: H'FF92

Bit	Bit Name	Set Value	R/W	Description
1	ECPWME	1	R/W	Event counter PWM enable Controls operation of event counter PWM and selection of IRQAEC. 0: AEC PWM halted, IRQAEC selected 1: AEC PWM enabled, IRQAEC not selected

- ECCR Event counter control register Address: H'FF94

Bit	Bit Name	Set Value	R/W	Description
3	PWCK2	0	R/W	Event counter PWM clock select
2	PWCK1	0	R/W	Selects event counter PWM clock.
1	PWCK0	0	R/W	000: ϕ/2 001: ϕ/4 010: ϕ/8 011: ϕ/16 1x0: ϕ/32 1x1: ϕ/64

Note: x: Don't care

- PMR9 Port mode register 9 Address: H'FFC8

Bit	Bit Name	Set Value	R/W	Description
0	PWM1	1	R/W	P90/PWM1 pin switching Sets whether P90/PWM1 pin is to be used as P90 I/O pin or as PWM1 output pin. 0: P90 I/O pin 1: PWM1 output pin

- PWCR1 PWM1 control register Address: H'FFD0

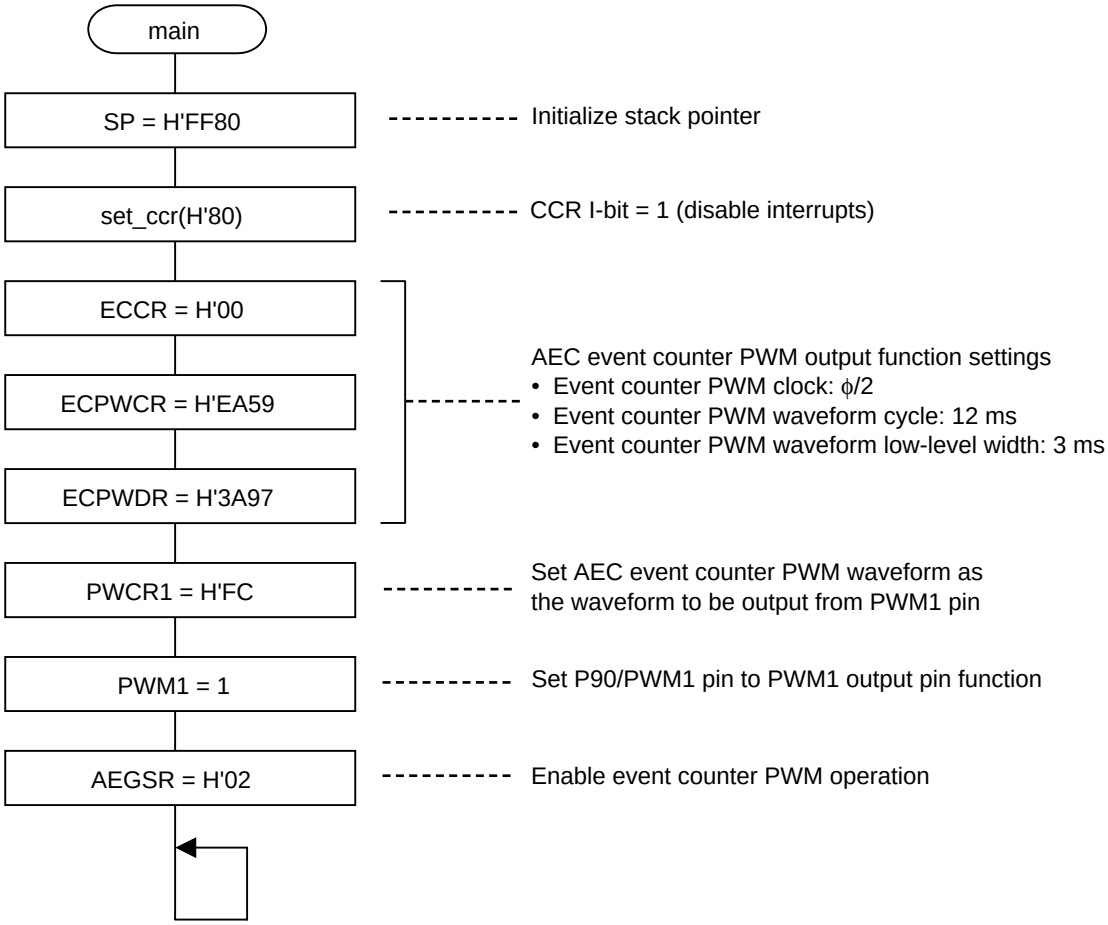
Bit	Bit Name	Set Value	R/W	Description
2	PWCR1n	1	W	PWM output waveform select Selects standard PWM waveform or pulse-division type PWM waveform. 0: Pulse-division type PWM waveform is output 1: Standard PWM waveform is output

4.4 RAM Usage

No RAM is used in this sample task.

5. Flowcharts

5.1 main



- Link Address Specifications

Section Name	Address
CV1	H'0000
P	H'0100

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Sep.16.04	—	First edition issued

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