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April 1st, 2010
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H8/300H SLP Series

Cyclic Operation Using TPU Compare Match Function

Introduction

The compare match function of the 16-bit timer pulse unit (TPU) is used to turn an LED connected to a port on and off at approximately 0.5 second intervals.

Target Device

H8/38076R

Contents

1. Specifications

- The compare match function of the 16-bit timer pulse unit (TPU) is used to turn an LED connected to a port on and off at approximately 0.5 second intervals.
- In this sample task, internal clock ϕ/256 is set as the timer counter_1 (TCNT_1) input clock, and the value of timer general register_1 (TGRA_1) is set to H'4C4A (19530). At ϕ = 10 MHz operation, a compare match is generated every 0.4999936 seconds, and on/off control of an LED connected to a port (P93) is performed by compare match interrupt processing.
- An example of cyclic operation by means of the TPU output compare function is shown in figure 1.

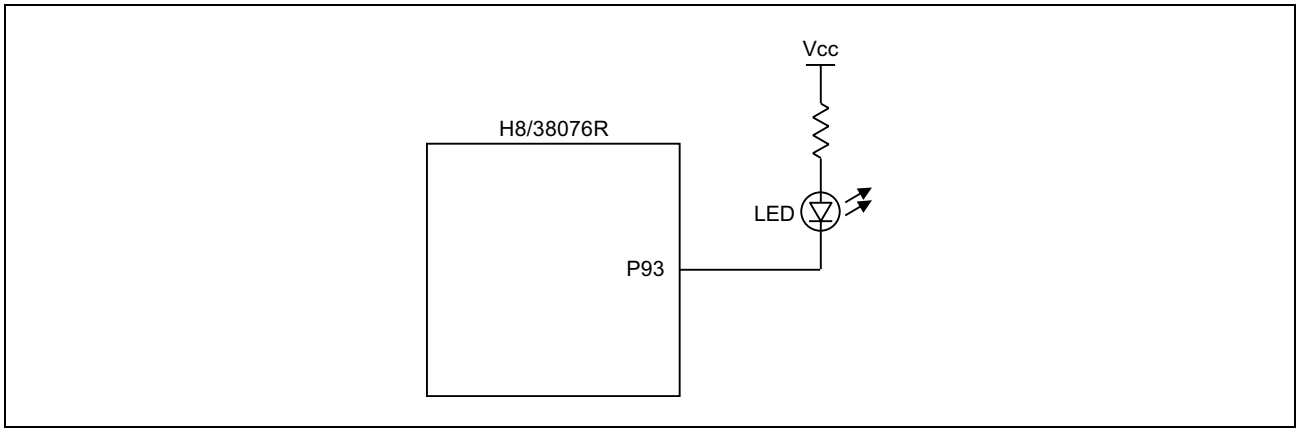


Figure 1 Example of Cyclic Operation Using TPU Compare Match Function

2. Functions Used

2.1 TPU Compare Match Function

In this sample task, the compare match function of the TPU is used to turn an LED connected to P93 on and off at approximately 0.5 second intervals. A block diagram of the compare match function of the TPU is shown in figure 2. The block diagram of the compare match function of the TPU is explained below.

- Timer control register_1 (TCR_1)

  Selects timer counter_1 (TCNT_1) counter clearing source, the input clock edge, and the clock source.
- Timer mode register_1 (TMDR_1)

  Sets the operating mode of channel 1.
- Timer interrupt enable register_1 (TIER_1)

  Enables or disables TPU_1 interrupt requests.
- Timer status register_1 (TSR_1)

  Indicates the state of TPU_1.
- Timer counter_1 (TCNT_1)

  A 16-bit readable/writable counter that counts using the rising edge of internal clock ϕ/256.
- Timer general register A_1 (TGRA_1)

  A 16-bit readable/writable input capture register.

- Timer start register (TSTR)

  Controls operation/stopping of timer counter_1 (TCNT_1).

- An example of compare match cycle calculation is shown below.

  (ϕ = 10 MHz, TCNT_1 input clock = ϕ/256, TGRA_1 set value = H'4C4A = 19530)

$$\text{Compare match cycle} = \frac{\text{TGRA\_1 set value} + 1}{\text{TCNT\_1 input clock}} = \frac{19530 + 1}{10\ \text{MHz} / 256} = 0.4999936\ \text{s}$$

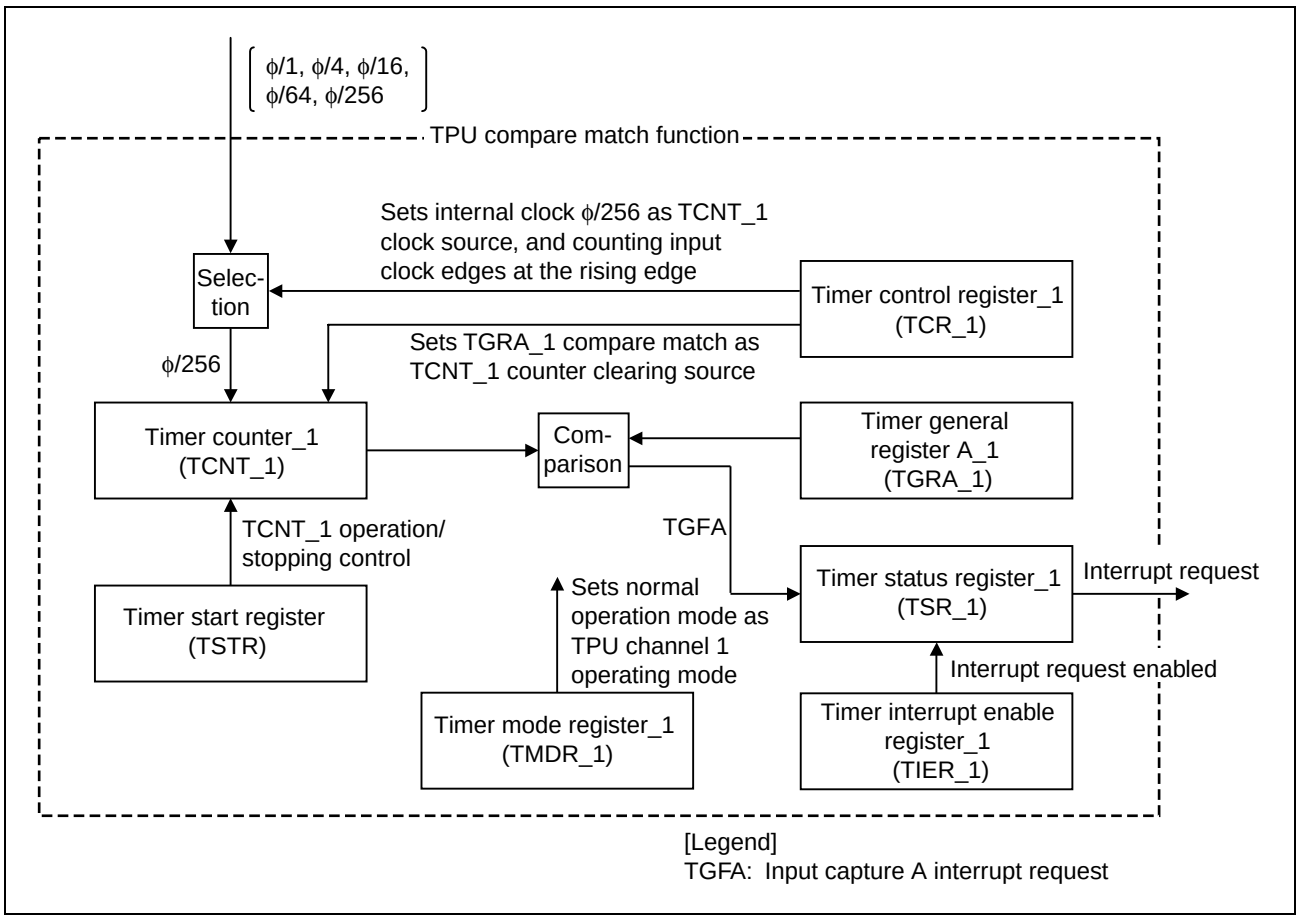


Figure 2 Block Diagram of TPU Compare Match Function

2.2 Assignment of Functions

Table 1 shows the assignment of functions in this sample task. Using functions assigned as shown in table 1, an LED connected to P93 is turned on and off at approximately 0.5 s intervals by means of the TPU compare match function.

Table 1 Assignment of Functions

Elements	Description
TCR_1	Sets TGRA_1 compare match as TCNT_1 counter clearing source, rising edge as input clock edge, and internal clock φ/256 as clock source
TMDR_1	Sets normal operation mode as TPU channel 1 operating mode
TIER_1	Enables TGFA interrupt
TSR_1	TGFA interrupt request flag
TCNT_1	16-bit counter using internal clock φ/256 as clock source
TGRA_1	16-bit compare match register
TSTR	Sets TCNT_1 count operation

3. Principles of Operation

The principles of operation of this sample task are illustrated in figure 3. Using the hardware and software processing shown in figure 3, an LED connected to P93 is turned on and off at approximately 0.5 s intervals by means of the compare match function of the TPU.

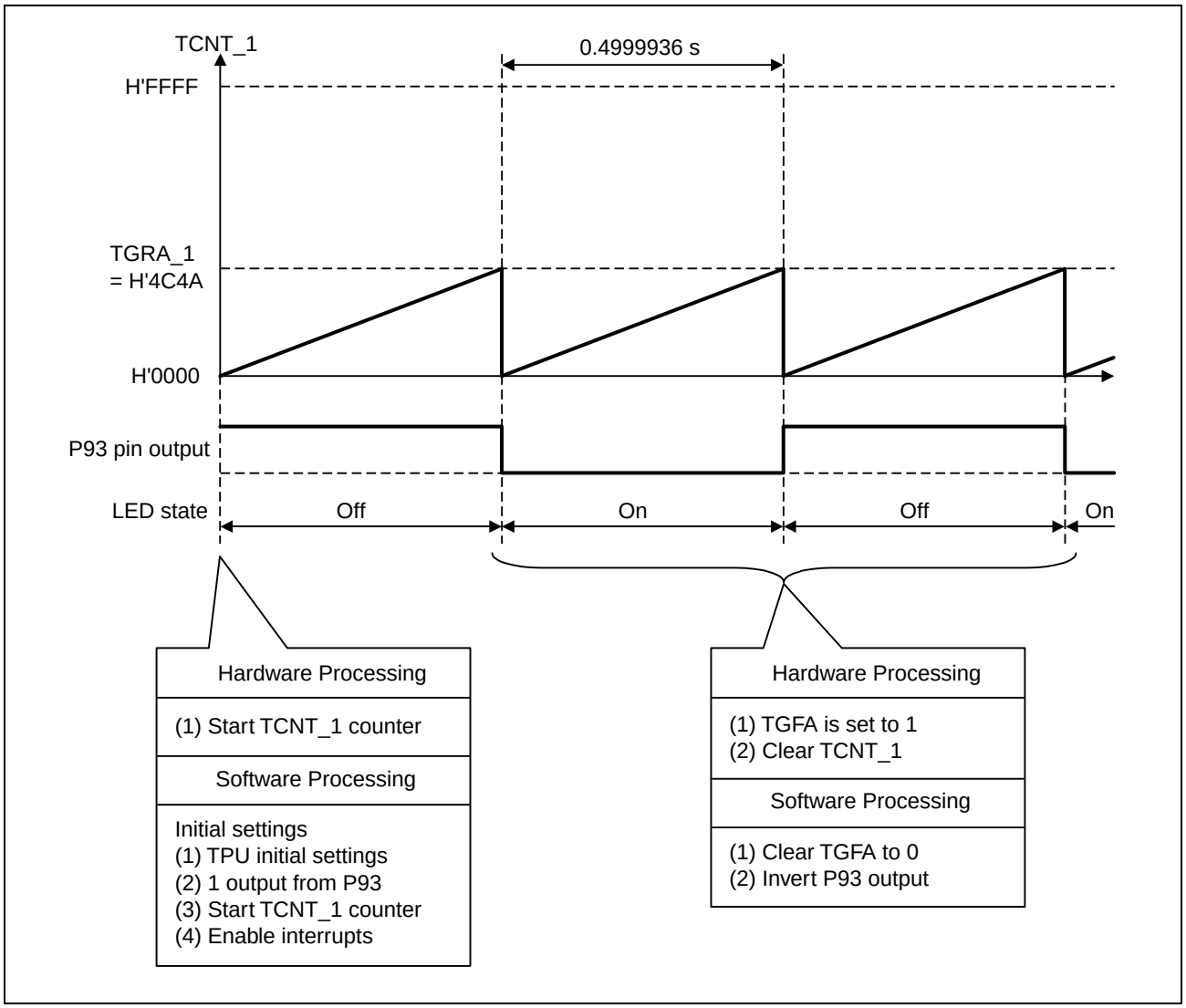


Figure 3 Principles of Operation

4. Description of Software

4.1 Modules

Table 2 shows the modules used in this sample task.

Table 2 Modules

Function Name	Description
main	TPU initial settings, P93 initial setting, interrupt enabling, TCNT_1 count operation start
int_tgi1a	TGRA_1 input capture A interrupt processing, inversion of P93 output

4.2 Arguments

No arguments are used in this sample task.

4.3 Internal Registers Used

The internal registers used in this sample task are shown below.

- TSTR Timer start register Address: H'F030

Bit	Bit Name	Set Value	R/W	Description
1	CST1	1	R/W	Counter start 1 Selects TCNT_1 operation or stopping. CST1 = 1: TCNT_1 performs count operation

- TCR_1 Timer control register_1 Address: H'F040

Bit	Bit Name	Set Value	R/W	Description
6	CCLR1	0	R/W	Counter clear 1, 0
5	CCLR0	1	R/W	Select the TCNT_1 counter clearing source. CCLR1 = 0, CCLR0 = 1: TCNT_1 cleared by TGRA_1 compare match
4	CKEG1	0	R/W	Clock edge 1, 0
3	CKEG0	0	R/W	Select the TCNT_1 input clock edge. CKEG1 = 0, CKEG0 = 0: Counts at the rising edge
2	TPSC2	1	R/W	Timer prescaler 2, 1, 0
1	TPSC1	1	R/W	Select the TCNT_1 clock source.
0	TPSC0	0	R/W	TPSC2 = 1, TPSC1 = 1, TPSC0 = 0: Counts on internal clock ϕ/256

- TMDR_1 Timer mode register_1 Address: H'F041

Bit	Bit Name	Set Value	R/W	Description
1	MD1	0	R/W	Mode 1, 0
0	MD0	0	R/W	Select the TPU_1 operating mode. MD1 = 0, MD0 = 0: TPU_1 set to normal operation mode

- TIER_1 Timer interrupt enable register_1 Address: H'F044

Bit	Bit Name	Set Value	R/W	Description
0	TGIEA	1	R/W	TGR interrupt enable A Enables or disables TGFA flag interrupt request (TGI1A) when TGFA flag is set to 1 in TSR. TGIEA = 1: TGFA flag interrupt request (TGI1A) enabled

- TSR_1 Timer status register_1 Address: H'F045

Bit	Bit Name	Set Value	R/W	Description
0	TGFA	0	R/(W)*	Input capture/output compare flag A Status flag indicating occurrence TGRA_1 input capture or compare match [Setting conditions] • When TCNT_1 = TGRA_1 while TGRA_1 is functioning as output compare register • When TCNT_1 value is transferred to TGRA_1 in response to input capture signal when TGRA_1 is functioning as input capture register [Clearing condition] • When 0 is written to TGFA after TGFA is read while set to 1

Note: * Only 0 can be written to clear the flag.

- TCNT_1 Timer counter_1 Address: H'F046

Bit	Bit Name	Set Value	R/W	Description
15	Bit 15	0	R/W	Timer counter_1 16-bit readable/writable counter. TCNT_1 is initialized to H'0000 at a reset. TCNT_1 cannot be accessed in 8-bit units, and must always be accessed in 16-bit units.
14	Bit 14	0	R/W	
13	Bit 13	0	R/W	
12	Bit 12	0	R/W	
11	Bit 11	0	R/W	
10	Bit 10	0	R/W	
9	Bit 9	0	R/W	
8	Bit 8	0	R/W	
7	Bit 7	0	R/W	
6	Bit 6	0	R/W	
5	Bit 5	0	R/W	
4	Bit 4	0	R/W	
3	Bit 3	0	R/W	
2	Bit 2	0	R/W	
1	Bit 1	0	R/W	
0	Bit 0	0	R/W	

- TGRA_1 Timer general register A_1 Address: H'F048

Bit	Bit Name	Set Value	R/W	Description
15	Bit 15	0	R/W	Timer general register A_1
14	Bit 14	1	R/W	A 16-bit readable/writable register, functioning as either output compare or input capture register. TGRA_1 is initialized to H'FFFF at a reset. TGRA_1 cannot be accessed in 8-bit units, and must always be accessed in 16-bit units.
13	Bit 13	0	R/W	
12	Bit 12	0	R/W	
11	Bit 11	1	R/W	Note: Set value: H'4C4A
10	Bit 10	1	R/W	
9	Bit 9	0	R/W	
8	Bit 8	0	R/W	
7	Bit 7	0	R/W	
6	Bit 6	1	R/W	
5	Bit 5	0	R/W	
4	Bit 4	0	R/W	
3	Bit 3	1	R/W	
2	Bit 2	0	R/W	
1	Bit 1	1	R/W	
0	Bit 0	0	R/W	

- PDR9 Port data register 9 Address: H'FFDC

Bit	Bit Name	Set Value	R/W	Description
3	P93	1	R/W	P93 data register If P93 is read while PCR9 bits are set to 1, the values stored in PDR9 are read, regardless of the actual pin states. If P93 is read while PCR9 bits are cleared to 0, the pin states are read.

- PCR9 Port control register 9 Address: H'FFEC

Bit	Bit Name	Set Value	R/W	Description
3	PCR93	1	W	P93 control register Controls P93 input/output. P93 is an output pin when PCR93 is set to 1, and an input pin when PCR93 is cleared to 0. PCR9 is a write-only register, and will always return a value of 1 if read.

4.4 Constants Used

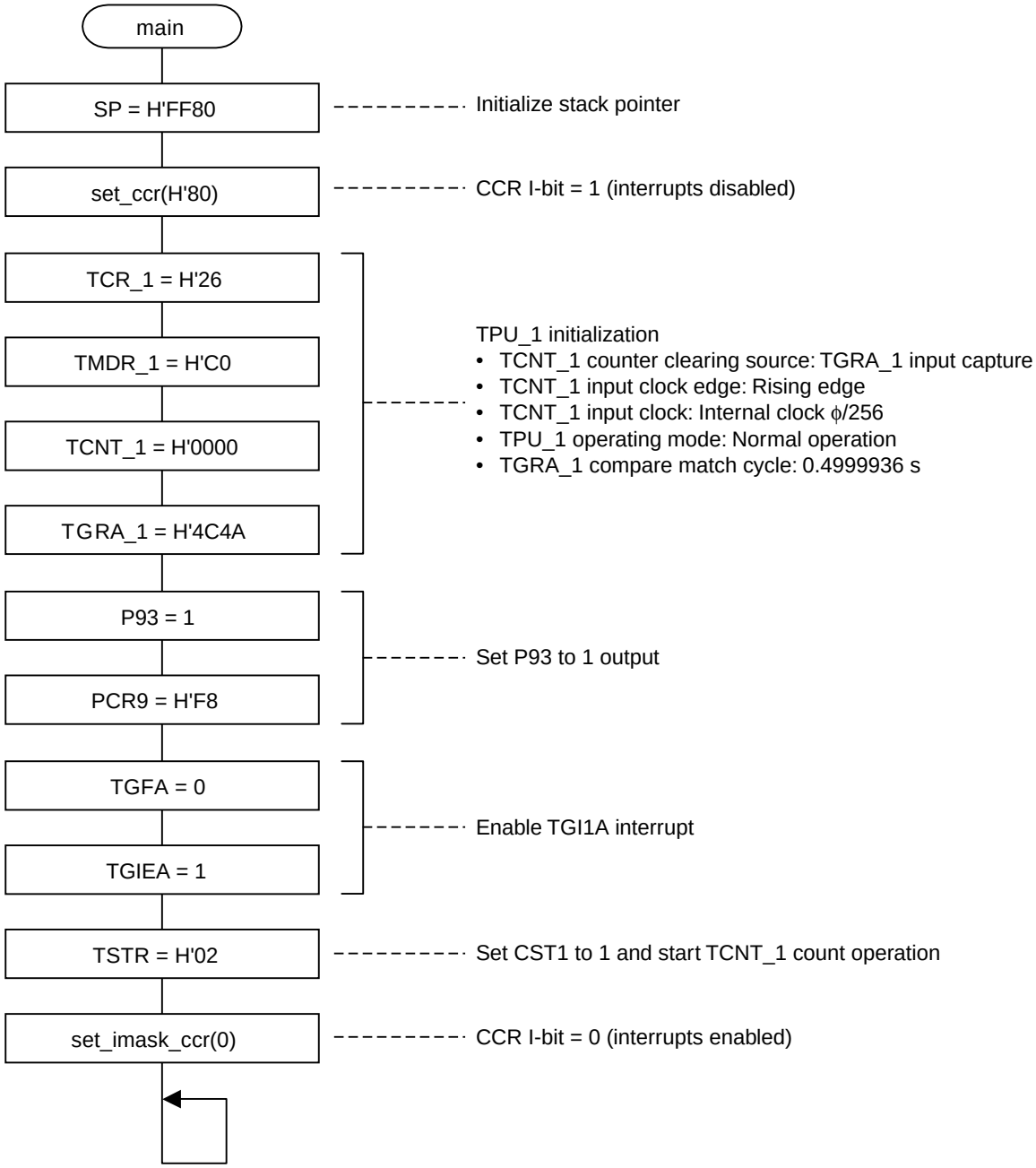
No constants are used in this sample task.

4.5 RAM Usage

No RAM is used in this sample task.

5. Flowcharts

5.1 main



5.2 int_tgi1a

- Link Address Specifications

Section Name	Address
CV1	H'0000
CV2	H'003A
P	H'0100

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Sep.16.04	—	First edition issued

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